



# STGD10NC60H

N-channel 10A - 600V - DPAK  
Very fast PowerMESH™ IGBT

## Features

Type	V <sub>CE(S)</sub>	V <sub>CE(sat)</sub> (Max)@ 25°C	I <sub>C</sub> @100°C
STGD10NC60H	600V	< 2.5V	10A

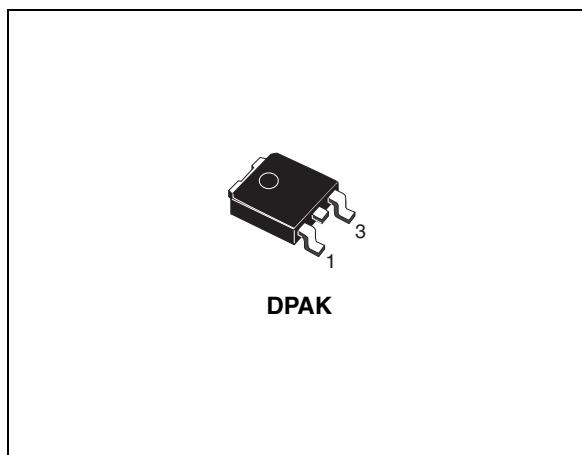
- Low on-voltage drop (V<sub>cesat</sub>)
- Low C<sub>RES</sub> / C<sub>IES</sub> ratio (no cross-conduction susceptibility)

## Description

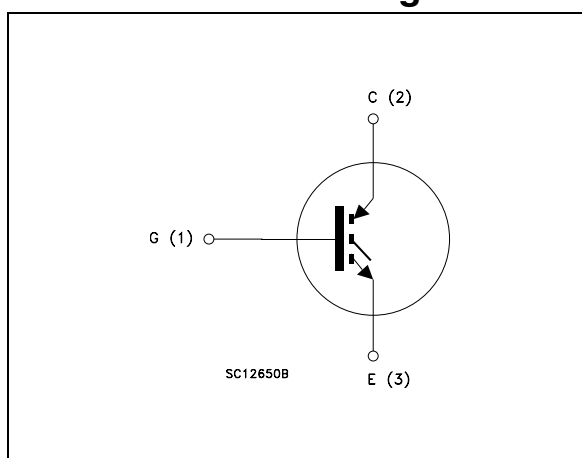
Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix "H" identifies a family optimized for high frequency applications in order to achieve very high switching performances (reduced t<sub>fall</sub>) maintaining a low voltage drop.

## Applications

- High frequency motor controls
- SMPS and PFC in both hard switch and resonant topologies
- Motor drivers



## Internal schematic diagram



## Order code

Part number	Marking	Package	Packaging
STGD10NC60H	GD10NC60H	DPAK	Tape & reel

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CES}$	Collector-emitter voltage ( $V_{GS} = 0$ )	600	V
$I_C^{(1)}$	Collector current (continuous) at $T_C = 25^\circ\text{C}$	20	A
$I_C^{(1)}$	Collector current (continuous) at $T_C = 100^\circ\text{C}$	10	A
$I_{CL}^{(2)}$	Collector current (pulsed)	40	A
$V_{GE}$	Gate-emitter voltage	$\pm 20$	V
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	60	W
$T_j$	Operating junction temperature	- 55 to 150	$^\circ\text{C}$

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C, I_C)}$$

2.  $V_{clamp}=480\text{V}$ ,  $T_j=150^\circ\text{C}$ ,  $R_G=10\Omega$ ,  $V_{GE}=15\text{V}$

**Table 2. Thermal resistance**

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	2.08	$^\circ\text{C/W}$
Rthj-amb	Thermal resistance junction-ambient max	62.5	$^\circ\text{C/W}$

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 3. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	$I_C = 1\text{mA}$ , $V_{GE} = 0$	600			V
$I_{CES}$	Collector cut-off current ( $V_{GE} = 0$ )	$V_{CE} = \text{Max rating}$ , $T_C = 25^{\circ}\text{C}$ $V_{CE} = \text{Max rating}$ , $T_C = 125^{\circ}\text{C}$			150 1	$\mu\text{A}$ mA
$I_{GES}$	Gate-emitter leakage current ( $V_{CE} = 0$ )	$V_{GE} = \pm 20\text{V}$ , $V_{CE} = 0$			$\pm 100$	nA
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}$ , $I_C = 250\ \mu\text{A}$	3.75		5.75	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{V}$ , $I_C = 5\text{A}$ $V_{GE} = 15\text{V}$ , $I_C = 5\text{A}$ , $T_C = 125^{\circ}\text{C}$		1.9 1.7	2.5	V V
$g_{fs}$	Forward transconductance	$V_{CE} = 15\text{V}$ , $I_C = 5\text{A}$		3.5		S

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{ies}$	Input capacitance	$V_{CE} = 25\text{V}$ , $f = 1\text{MHz}$ , $V_{GE} = 0$		365		pF
$C_{oes}$	Output capacitance			43		pF
$C_{res}$	Reverse transfer capacitance			8.3		pF
$Q_g$	Total gate charge	$V_{CE} = 390\text{V}$ , $I_C = 5\text{A}$ ,		19.2		nC
$Q_{ge}$	Gate-emitter charge	$V_{GE} = 15\text{V}$ ,		4.5		nC
$Q_{gc}$	Gate-collector charge	(see Figure 16)		7		nC

**Table 5. Switching on/off (inductive load)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$ $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	$V_{CC} = 390V, I_C = 5A$ $R_G = 10\Omega, V_{GE} = 15V,$ <i>Figure 15. Figure 17.</i>		14.2 5 1000		ns ns A/ $\mu$ s
$t_{d(on)}$ $t_r$ $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	$V_{CC} = 390V, I_C = 5A$ $R_G = 10\Omega, V_{GE} = 15V,$ $T_j = 125^\circ C$ <i>Figure 15. Figure 17.</i>		14 5 920		ns ns A/ $\mu$ s
$t_r(V_{off})$ $t_{d(off)}$ $t_f$	Off voltage rise time Turn-off delay time Current fall time	$V_{CC} = 390V, I_C = 5A,$ $R_{GE} = 10\Omega, V_{GE} = 15V,$ <i>Figure 15. Figure 17.</i>		27 72 85		ns ns ns
$t_r(V_{off})$ $t_{d(off)}$ $t_f$	Off voltage rise time Turn-off delay time Current fall time	$V_{CC} = 390V, I_C = 5A,$ $R_{GE} = 10\Omega, V_{GE} = 15V,$ $T_j = 125^\circ C$ <i>Figure 15. Figure 17.</i>		50 108 139		ns ns ns

**Table 6. Switching energy (inductive load)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{on}$ $E_{off}^{(1)}$ $E_{ts}$	Turn-on switching losses Turn-off switching losses Total switching losses	$V_{CC} = 390V, I_C = 5A$ $R_G = 10\Omega, V_{GE} = 15V, T_j = 25^\circ C$ <i>(see Figure 17)</i>		31.8 95 126.8		$\mu$ J $\mu$ J $\mu$ J
$E_{on}$ $E_{off}^{(1)}$ $E_{ts}$	Turn-on switching losses Turn-off switching Losses Total switching losses	$V_{CC} = 390V, I_C = 5A$ $R_G = 10\Omega, V_{GE} = 15V,$ $T_j = 125^\circ C$ <i>(see Figure 17)</i>		61.8 173 234.8		$\mu$ J $\mu$ J $\mu$ J

1. Turn-off losses include also the tail of the collector current

## 2.1 Electrical characteristics (curves)

Figure 1. Output characteristics

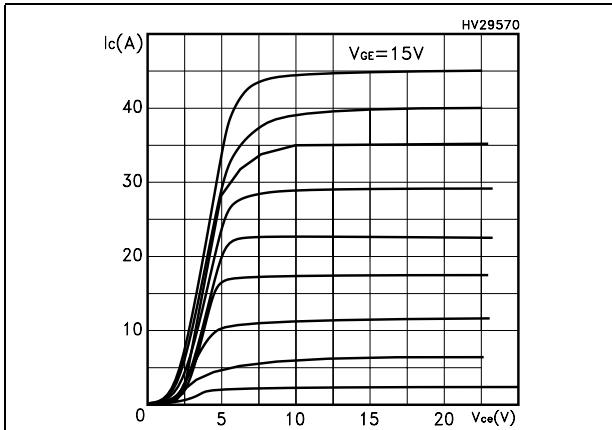


Figure 2. Transfer characteristics

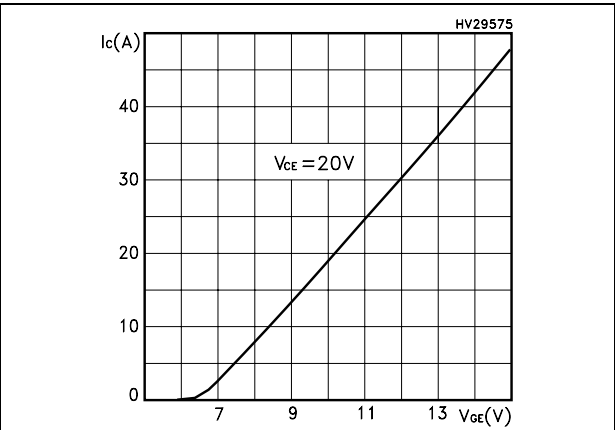


Figure 3. Transconductance

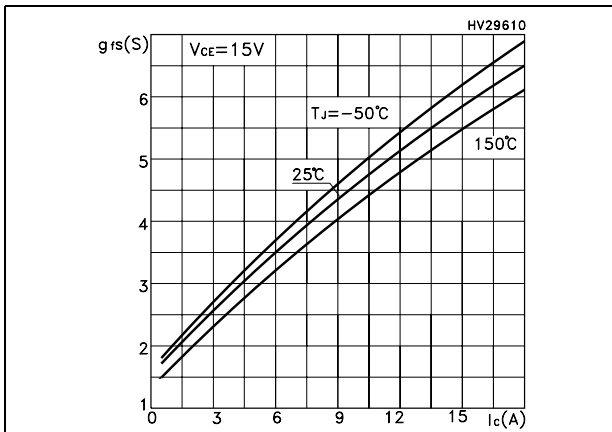


Figure 4. Collector-emitter on voltage vs temperature

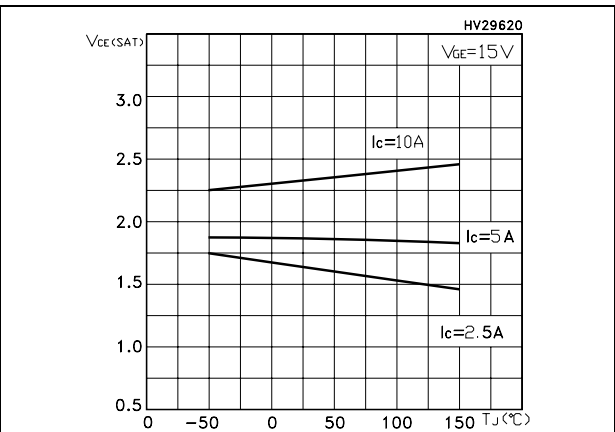


Figure 5. Gate charge vs gate-source voltage

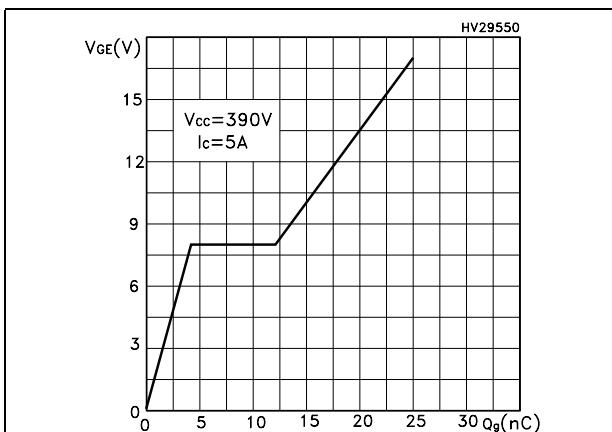


Figure 6. Capacitance variations

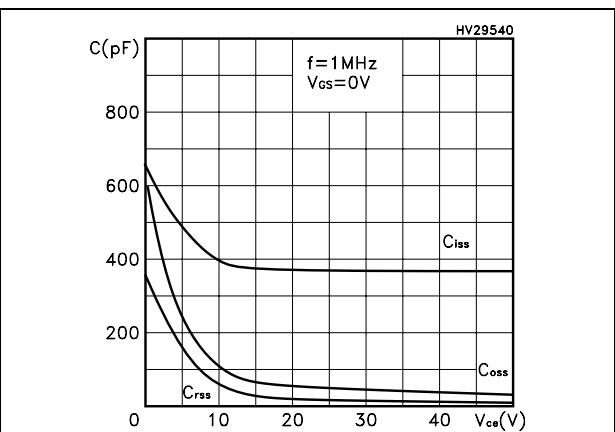


Figure 7. Normalized gate threshold voltage vs temperature

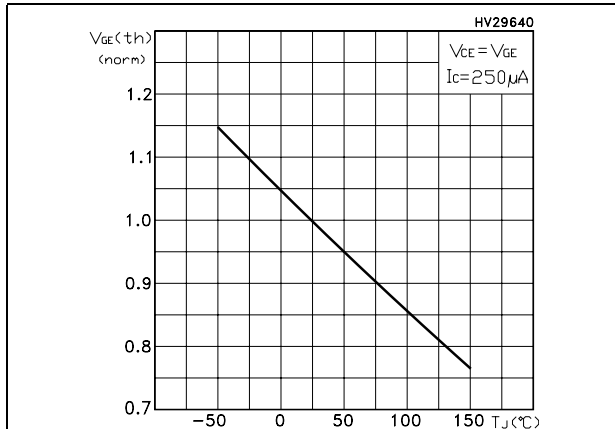


Figure 8. Collector-emitter on voltage vs collector current

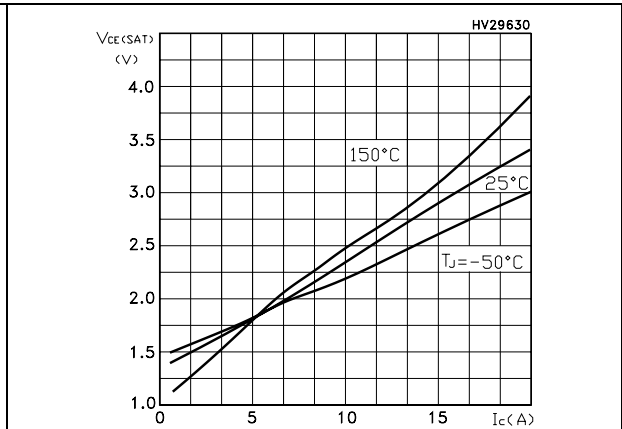


Figure 9. Normalized breakdown voltage vs temperature

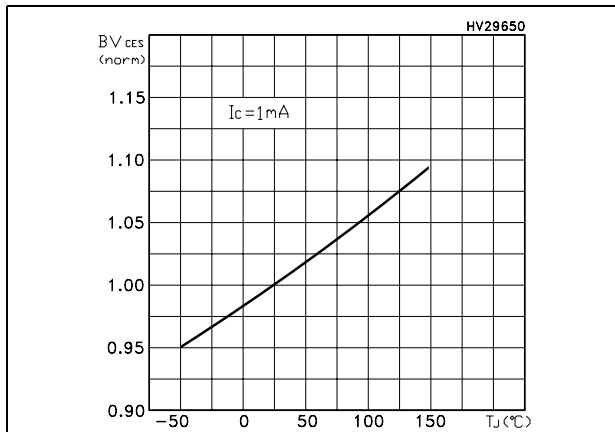


Figure 10. Switching losses vs temperature

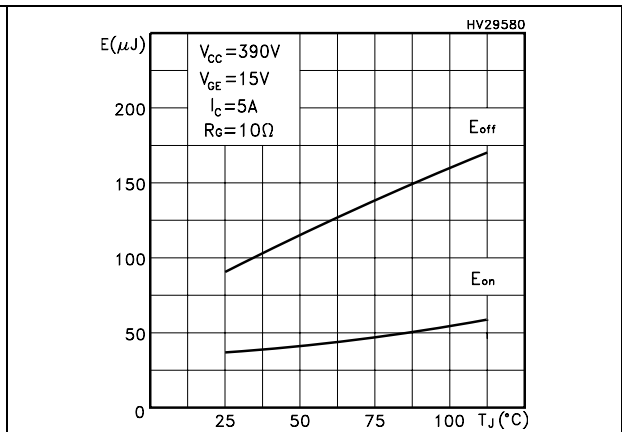


Figure 11. Switching losses vs gate resistance

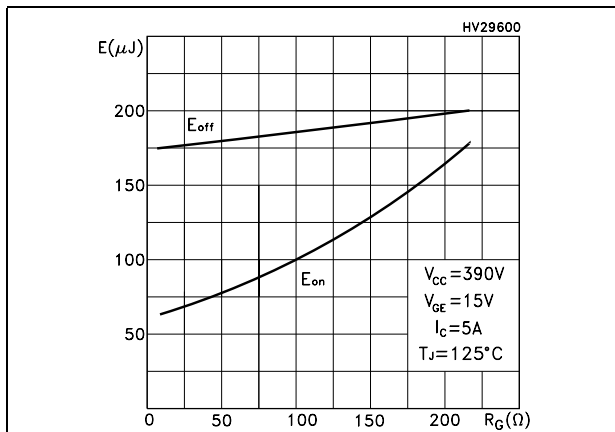


Figure 12. Switching losses vs collector current

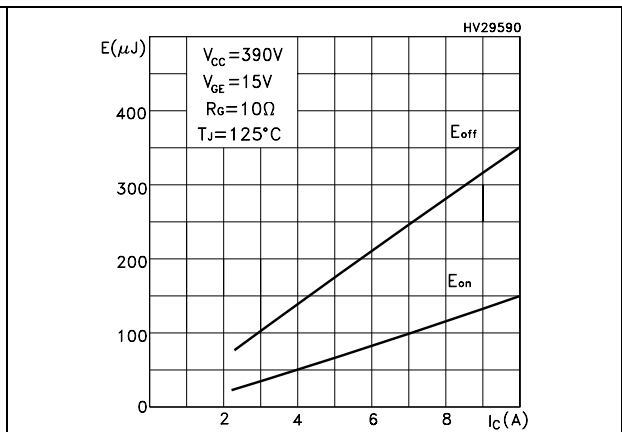


Figure 13. Thermal Impedance

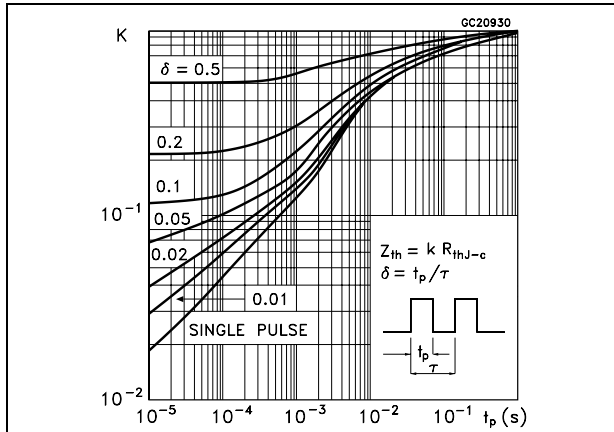
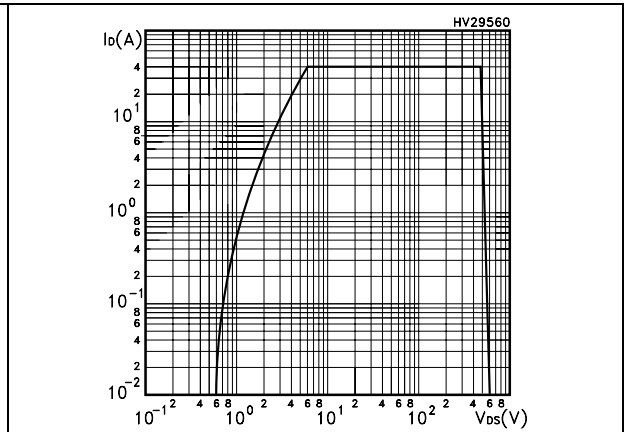


Figure 14. Turn-off SOA





### 3 Test circuits

Figure 15. Test circuit for inductive load switching

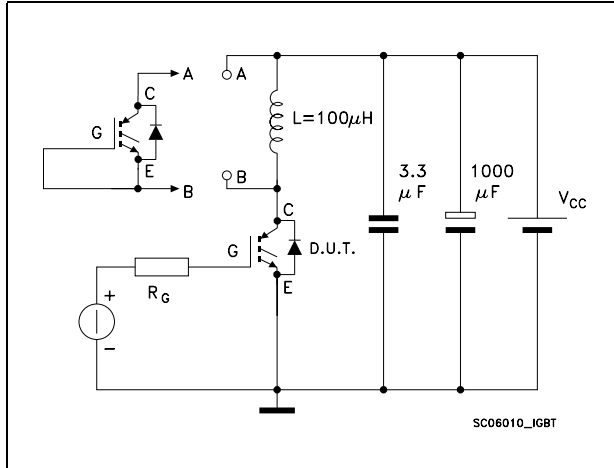


Figure 16. Gate charge test circuit

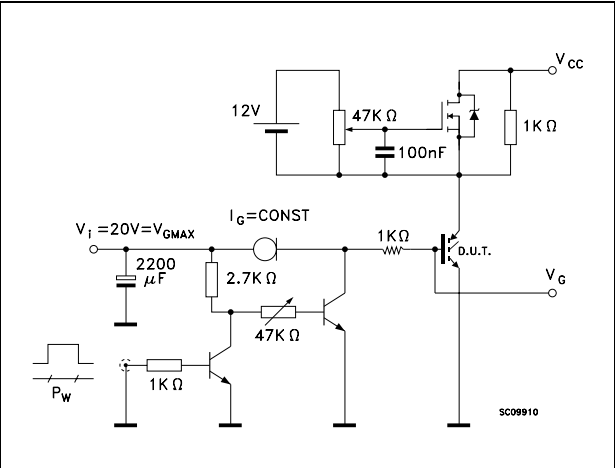
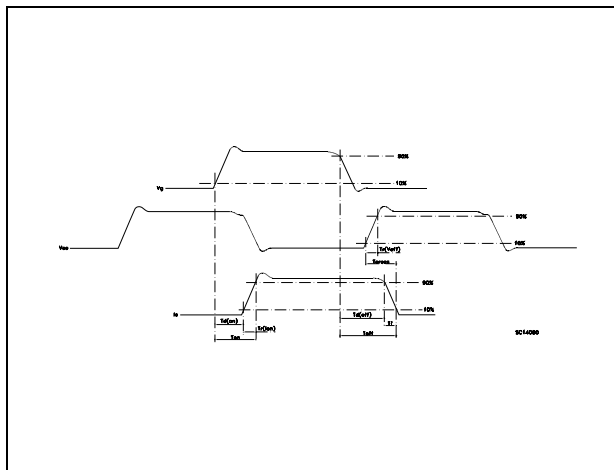


Figure 17. Switching waveform

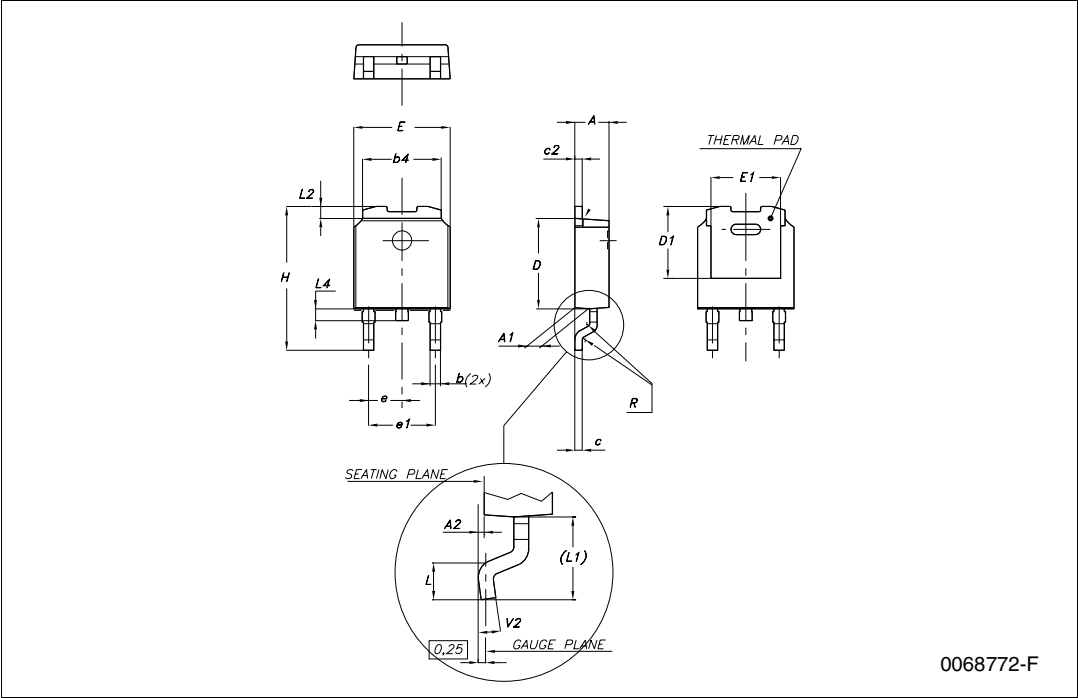


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

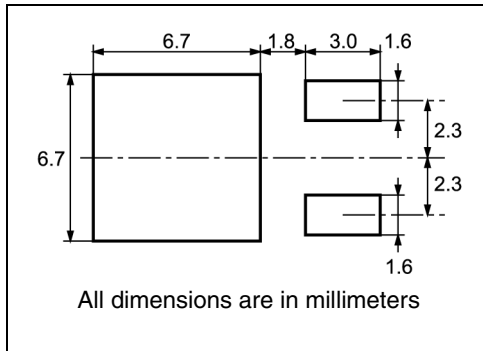
**DPAK MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



# 5 Packaging mechanical data

## DPAK FOOTPRINT



## TAPE AND REEL SHIPMENT

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY		BULK QTY	
2500		2500	

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

## 6 Revision history

Table 7. Revision history

Date	Revision	Changes
02-Apr-2007	1	Initial release.

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