

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT93** 4-bit binary ripple counter

Product specification  
File under Integrated Circuits, IC06

December 1990

# 4-bit binary ripple counter

# 74HC/HCT93

## FEATURES

- Various counting modes
- Asynchronous master reset
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT93 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT93 are 4-bit binary ripple counters. The devices consist of four master-slave flip-flops internally connected to provide a

divide-by-two section and a divide-by-eight section. Each section has a separate clock input ( $\overline{CP}_0$  and  $\overline{CP}_1$ ) to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q<sub>n</sub> outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous master reset (MR<sub>1</sub> and MR<sub>2</sub>) is provided which overrides both clocks and resets (clears) all flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages,

the device may be operated in various counting modes. In a 4-bit ripple counter the output Q<sub>0</sub> must be connected externally to input  $\overline{CP}_1$ . The input count pulses are applied to clock input  $\overline{CP}_0$ . Simultaneous frequency divisions of 2, 4, 8 and 16 are performed at the Q<sub>0</sub>, Q<sub>1</sub>, Q<sub>2</sub> and Q<sub>3</sub> outputs as shown in the function table. As a 3-bit ripple counter the input count pulses are applied to input  $\overline{CP}_1$ . Simultaneous frequency divisions of 2, 4 and 8 are available at the Q<sub>1</sub>, Q<sub>2</sub> and Q<sub>3</sub> outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

| SYMBOL                              | PARAMETER   | CONDITIONS                                    | TYPICAL |     | UNIT |
|-------------------------------------|---|---|---------|-----|------|
|                                     |   |   | HC      | HCT |      |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay $\overline{CP}_0$ to Q <sub>0</sub> | C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V | 12      | 15  | ns   |
| f <sub>max</sub>                    | maximum clock frequency                               |   | 100     | 77  | MHz  |
| C <sub>I</sub>                      | input capacitance                                     |   | 3.5     | 3.5 | pF   |
| C <sub>PD</sub>                     | power dissipation capacitance per package             | notes 1 and 2                                 | 22      | 22  | pF   |

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF; V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>; for HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

## ORDERING INFORMATION

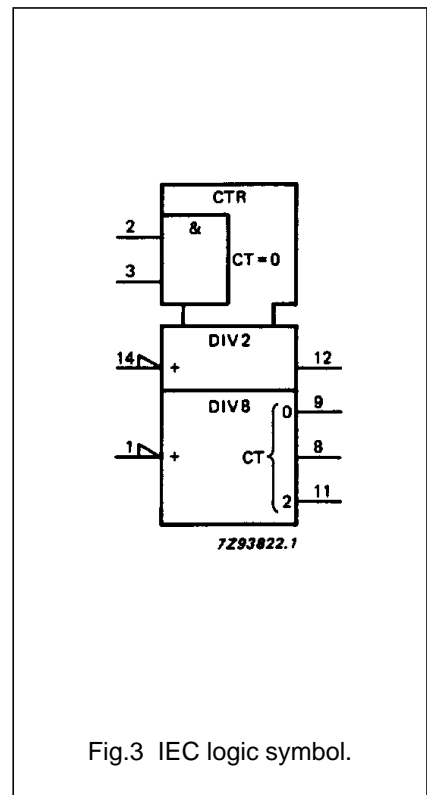
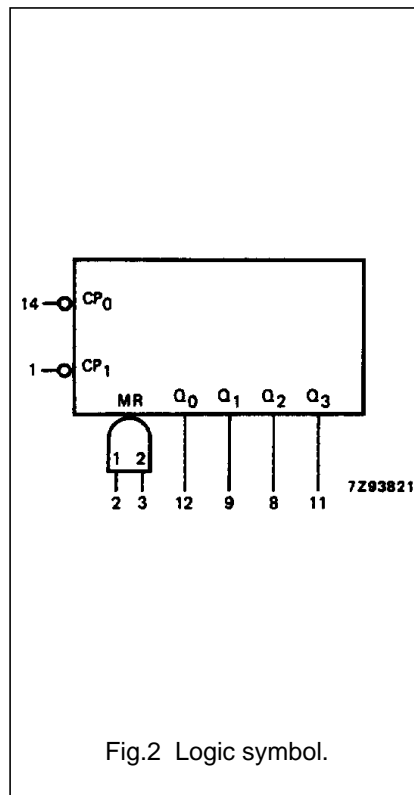
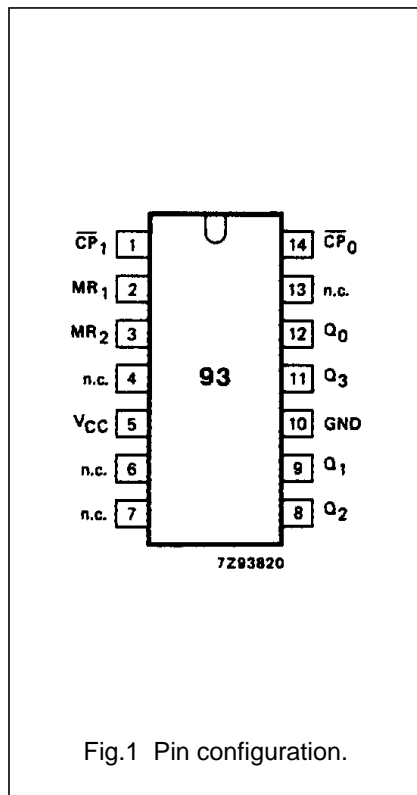
See "74HC/HCT/HCU/HCMOS Logic Package Information".

4-bit binary ripple counter

74HC/HCT93

PIN DESCRIPTION

| PIN NO.      | SYMBOL                            | NAME AND FUNCTION   |
|--------------|-----------------------------------|---|
| 1            | $\overline{CP}_1$                 | clock input 2 <sup>nd</sup> , 3 <sup>rd</sup> and 4 <sup>th</sup> section (HIGH-to-LOW, edge-triggered) |
| 2, 3         | MR <sub>1</sub> , MR <sub>2</sub> | asynchronous master reset (active HIGH)   |
| 4, 6, 7, 13  | n.c.                              | not connected   |
| 5            | V <sub>CC</sub>                   | positive supply voltage   |
| 10           | GND                               | ground (0 V)  |
| 12, 9, 8, 11 | Q <sub>0</sub> to Q <sub>3</sub>  | flip-flop outputs   |
| 14           | $\overline{CP}_0$                 | clock input 1 <sup>st</sup> section (HIGH-to-LOW, edge-triggered)                                       |



# 4-bit binary ripple counter

# 74HC/HCT93

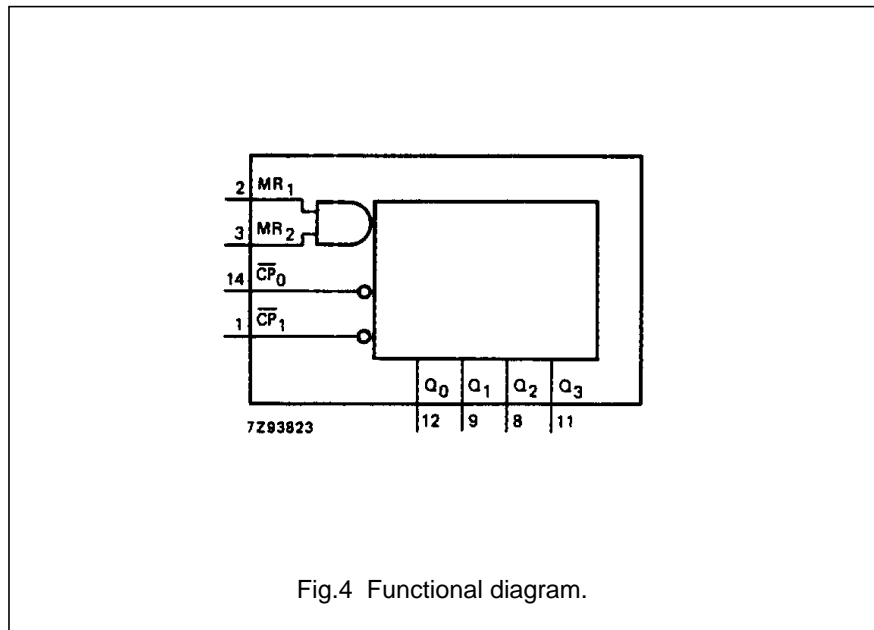


Fig.4 Functional diagram.

### FUNCTION TABLE

| COUNT | OUTPUTS        |                |                |                |
|-------|----------------|----------------|----------------|----------------|
|       | Q <sub>0</sub> | Q <sub>1</sub> | Q <sub>2</sub> | Q <sub>3</sub> |
| 0     | L              | L              | L              | L              |
| 1     | H              | L              | L              | L              |
| 2     | L              | H              | L              | L              |
| 3     | H              | H              | L              | L              |
| 4     | L              | L              | H              | L              |
| 5     | H              | L              | H              | L              |
| 6     | L              | H              | H              | L              |
| 7     | H              | H              | H              | L              |
| 8     | L              | L              | L              | H              |
| 9     | H              | L              | L              | H              |
| 10    | L              | H              | L              | H              |
| 11    | H              | H              | L              | H              |
| 12    | L              | L              | H              | H              |
| 13    | H              | L              | H              | H              |
| 14    | L              | H              | H              | H              |
| 15    | H              | H              | H              | H              |

### Notes

- Output Q<sub>0</sub> connected to  $\overline{CP_1}$ .  
 H = HIGH voltage level  
 L = LOW voltage level

### MODE SELECTION

| RESET INPUTS    |                 | OUTPUTS        |                |                |                |
|-----------------|-----------------|----------------|----------------|----------------|----------------|
| MR <sub>1</sub> | MR <sub>2</sub> | Q <sub>0</sub> | Q <sub>1</sub> | Q <sub>2</sub> | Q <sub>3</sub> |
| H               | H               | L              | L              | L              | L              |
| L               | H               | count          |                |                |                |
| H               | L               | count          |                |                |                |
| L               | L               | count          |                |                |                |

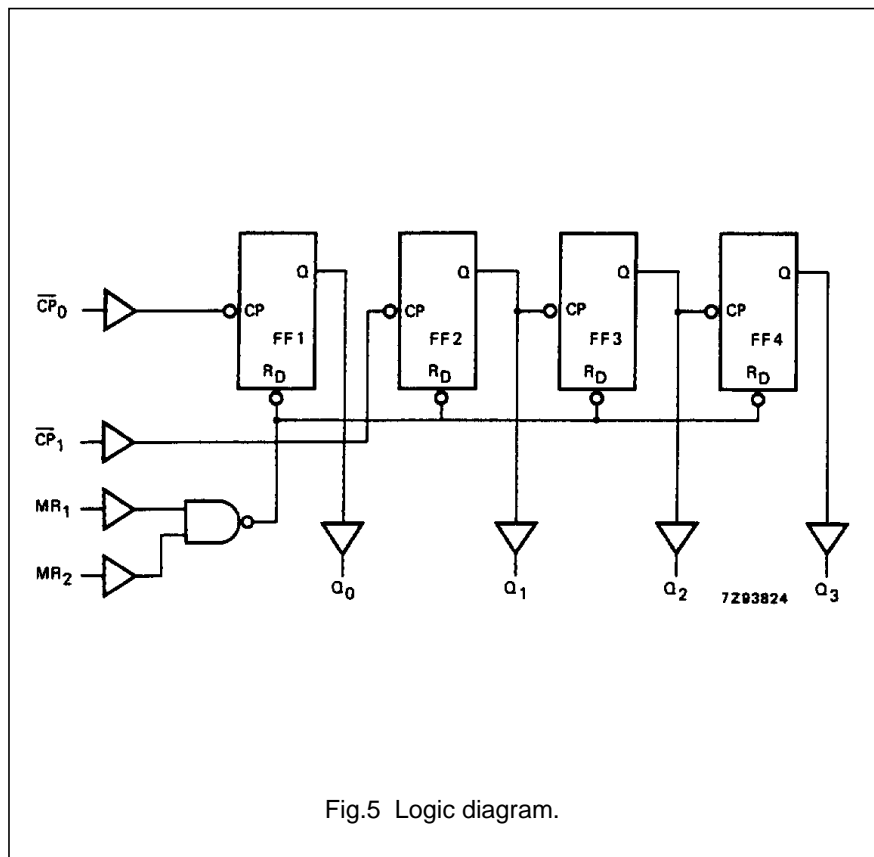


Fig.5 Logic diagram.

## 4-bit binary ripple counter

## 74HC/HCT93

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER   | T <sub>amb</sub> (°C) |                 |                 |                 |                 |                 |                 | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|---|-----------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|------------------------|-----------|
|                                     |   | 74HC                  |                 |                 |                 |                 |                 |                 |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |   | +25                   |                 |                 | -40 to +85      |                 | -40 to +125     |                 |      |                        |           |
|                                     |   | min.                  | typ.            | max.            | min.            | max.            | min.            | max.            |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>CP <sub>0</sub> to Q <sub>0</sub>                |                       | 41<br>15<br>12  | 125<br>25<br>21 |                 | 155<br>31<br>26 |                 | 190<br>38<br>32 | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>CP <sub>1</sub> to Q <sub>1</sub>                |                       | 49<br>16<br>13  | 135<br>27<br>23 |                 | 170<br>34<br>29 |                 | 205<br>41<br>35 | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>CP <sub>1</sub> to Q <sub>2</sub>                |                       | 61<br>22<br>18  | 185<br>37<br>31 |                 | 230<br>46<br>39 |                 | 280<br>56<br>48 | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>CP <sub>1</sub> to Q <sub>3</sub>                |                       | 80<br>29<br>23  | 245<br>49<br>42 |                 | 305<br>61<br>52 |                 | 370<br>71<br>63 | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>PHL</sub>                    | propagation delay<br>MR <sub>n</sub> to Q <sub>n</sub>                |                       | 50<br>18<br>14  | 155<br>31<br>26 |                 | 195<br>39<br>33 |                 | 235<br>47<br>40 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time  |                       | 19<br>7<br>6    | 75<br>15<br>13  |                 | 95<br>19<br>16  |                 | 110<br>22<br>19 | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>rem</sub>                    | removal time<br>MR <sub>n</sub> to CP <sub>0</sub> , CP <sub>1</sub>  | 50<br>10<br>9         | 8<br>3<br>2     |                 | 65<br>13<br>11  |                 | 75<br>15<br>13  |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>w</sub>                      | pulse width<br>CP <sub>0</sub> , CP <sub>1</sub>                      | 80<br>16<br>14        | 14<br>5<br>4    |                 | 100<br>20<br>17 |                 | 120<br>24<br>20 |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>w</sub>                      | master reset pulse width<br>MR <sub>n</sub>                           | 80<br>16<br>14        | 14<br>5<br>4    |                 | 100<br>20<br>17 |                 | 120<br>24<br>20 |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| f <sub>max</sub>                    | maximum clock pulse<br>frequency<br>CP <sub>0</sub> , CP <sub>1</sub> | 6.0<br>30<br>35       | 30<br>91<br>108 |                 | 4.8<br>24<br>28 |                 | 4.0<br>20<br>24 |                 | MHz  | 2.0<br>4.5<br>6.0      | Fig.6     |

## 4-bit binary ripple counter

## 74HC/HCT93

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT                              | UNIT LOAD COEFFICIENT |
|------------------------------------|-----------------------|
| $\overline{CP}_0, \overline{CP}_1$ | 0.60                  |
| $MR_n$                             | 0.40                  |

**AC CHARACTERISTICS FOR 74HCT**

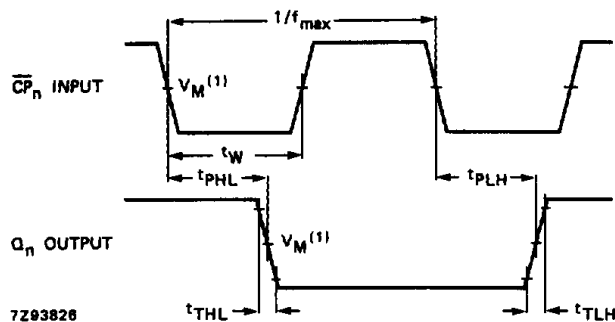
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

| SYMBOL                              | PARAMETER  | T <sub>amb</sub> (°C) |      |      |            |      |             |      | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|--|-----------------------|------|------|------------|------|-------------|------|------|------------------------|-----------|
|                                     |  | 74HCT                 |      |      |            |      |             |      |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |  | +25                   |      |      | -40 to +85 |      | -40 to +125 |      |      |                        |           |
|                                     |  | min.                  | typ. | max. | min.       | max. | min.        | max. |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>$\overline{CP}_0$ to Q <sub>0</sub>               |                       | 18   | 34   |            | 43   |             | 51   | ns   | 4.5                    | Fig.6     |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>CP <sub>1</sub> to Q <sub>1</sub>                 |                       | 18   | 34   |            | 43   |             | 51   | ns   | 4.5                    | Fig.6     |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>$\overline{CP}_1$ to Q <sub>2</sub>               |                       | 24   | 46   |            | 58   |             | 69   | ns   | 4.5                    | Fig.6     |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>$\overline{CP}_1$ to Q <sub>3</sub>               |                       | 30   | 58   |            | 73   |             | 87   | ns   | 4.5                    | Fig.6     |
| t <sub>PHL</sub>                    | propagation delay<br>MR <sub>n</sub> to Q <sub>n</sub>                 |                       | 17   | 33   |            | 41   |             | 50   | ns   | 4.5                    | Fig.7     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time   |                       | 7    | 15   |            | 19   |             | 22   | ns   | 4.5                    | Fig.6     |
| t <sub>rem</sub>                    | removal time<br>MR <sub>n</sub> to $\overline{CP}_0, \overline{CP}_1$  | 10                    | 3    |      | 13         |      | 15          |      | ns   | 4.5                    | Fig.7     |
| t <sub>w</sub>                      | pulse width<br>$\overline{CP}_0, \overline{CP}_1$                      | 16                    | 7    |      | 20         |      | 24          |      | ns   | 4.5                    | Fig.6     |
| t <sub>w</sub>                      | master reset pulse width<br>MR <sub>n</sub>                            | 16                    | 5    |      | 20         |      | 24          |      | ns   | 4.5                    | Fig.7     |
| f <sub>max</sub>                    | maximum clock pulse<br>frequency<br>$\overline{CP}_0, \overline{CP}_1$ | 30                    | 70   |      | 24         |      | 20          |      | MHz  | 4.5                    | Fig.6     |

4-bit binary ripple counter

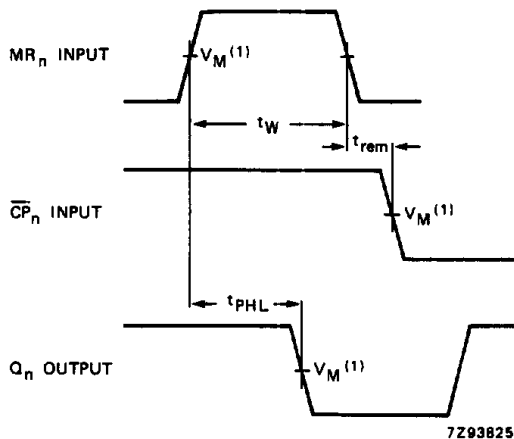
74HC/HCT93

AC WAVEFORMS



(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.6 Waveforms showing the clock ( $\overline{CP}_n$ ) to output ( $Q_n$ ) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.



(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.7 Waveforms showing the master reset ( $MR_n$ ) pulse width, the master reset to output ( $Q_n$ ) propagation delays and the master reset to clock ( $\overline{CP}_n$ ) removal time.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".