

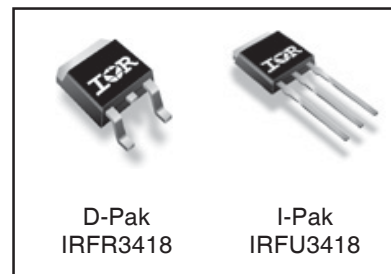
Applications

- High frequency DC-DC converters

V_{DSS}	R_{DS(on)} Max	I_D
80V	14mΩ	30A

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
V _{DS}	Drain-to-Source Voltage	80	V
V _{GS}	Gate-to-Source Voltage	± 20	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	70 [ⓐ]	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	50	
I _{DM}	Pulsed Drain Current [ⓑ]	280	
P _D @ T _C = 25°C	Maximum Power Dissipation	140	W
P _D @ T _A = 25°C	Maximum Power Dissipation	3.8	
	Linear Derating Factor	0.95	W/°C
dv/dt	Peak Diode Recovery dv/dt [ⓒ]	5.2	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	1.05	°C/W
R _{θJA}	Junction-to-Ambient (PCB Mount) *	—	40	
R _{θJA}	Junction-to-Ambient	—	110	

Notes [ⓐ] through [ⓒ] are on page 10

www.irf.com

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	80	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.08	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	11.5	14	mΩ	V _{GS} = 10V, I _D = 18A ④
V _{GS(th)}	Gate Threshold Voltage	3.5	—	5.5	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V _{DS} = 80V, V _{GS} = 0V
		—	—	250		V _{DS} = 64V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V

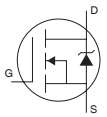
Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	66	—	—	S	V _{DS} = 25V, I _D = 18A
Q _g	Total Gate Charge	—	63	94	nC	I _D = 18A
Q _{gs}	Gate-to-Source Charge	—	23	—		V _{DS} = 40V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	23	—		V _{GS} = 10V ④
t _{d(on)}	Turn-On Delay Time	—	24	—	ns	V _{DD} = 40V
t _r	Rise Time	—	72	—		I _D = 18A
t _{d(off)}	Turn-Off Delay Time	—	41	—		R _G = 6.8Ω
t _f	Fall Time	—	27	—		V _{GS} = 10V ④
C _{iss}	Input Capacitance	—	3510	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	330	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	190	—		f = 1.0MHz
C _{oss}	Output Capacitance	—	1220	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	240	—		V _{GS} = 0V, V _{DS} = 64V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance	—	360	—		V _{GS} = 0V, V _{DS} = 0V to 64V ③

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy ^{②⑥}	—	260	mJ
I _{AR}	Avalanche Current ①	—	18	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	70	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	280		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 18A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	57	—	ns	T _J = 25°C, I _F = 18A, V _{DD} = 25V
Q _{rr}	Reverse Recovery Charge	—	130	—	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

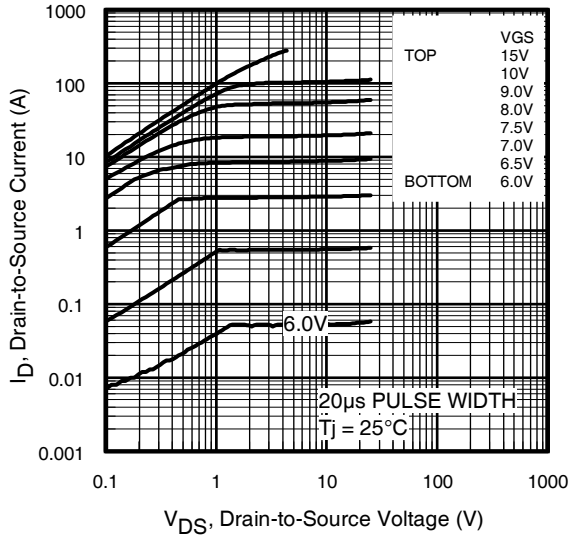


Fig 1. Typical Output Characteristics

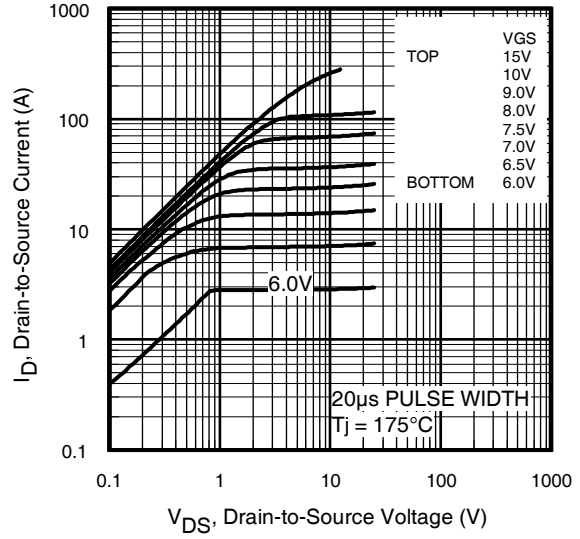


Fig 2. Typical Output Characteristics

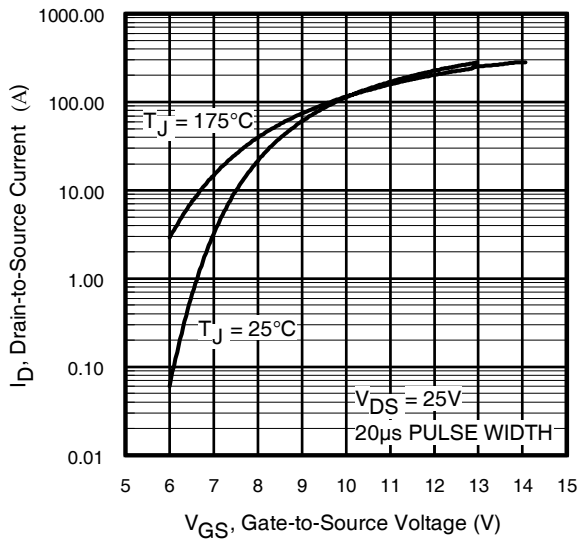


Fig 3. Typical Transfer Characteristics

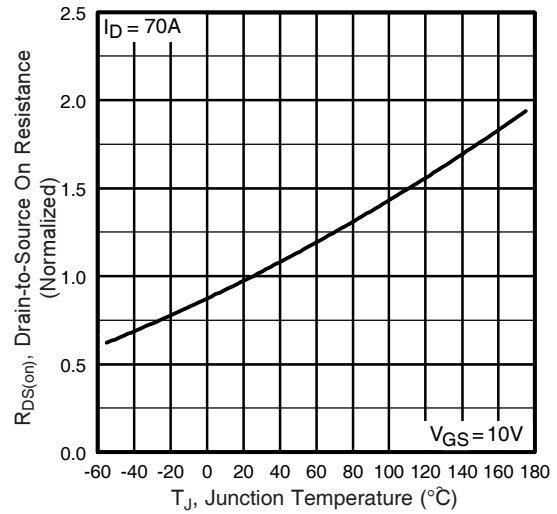


Fig 4. Normalized On-Resistance Vs. Temperature

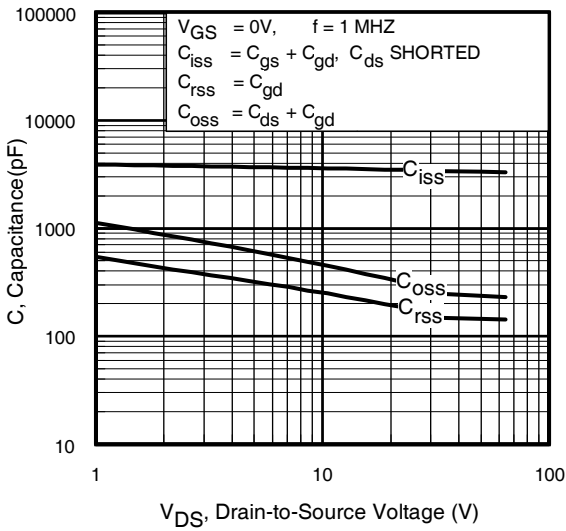


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

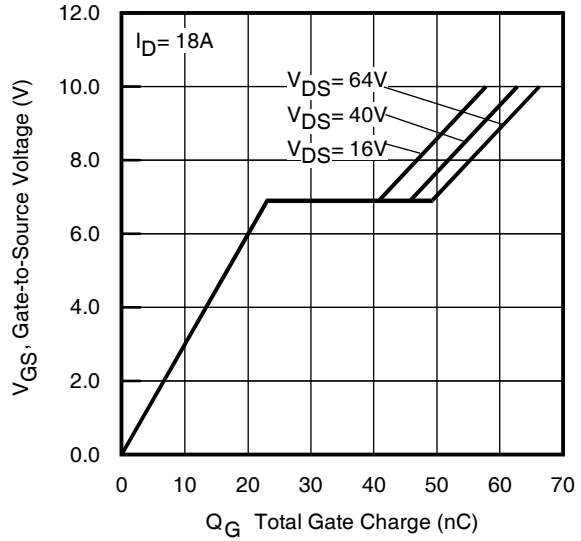


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

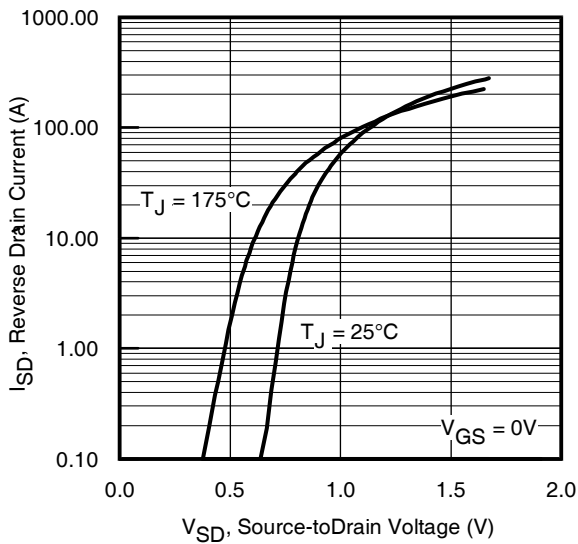


Fig 7. Typical Source-Drain Diode Forward Voltage

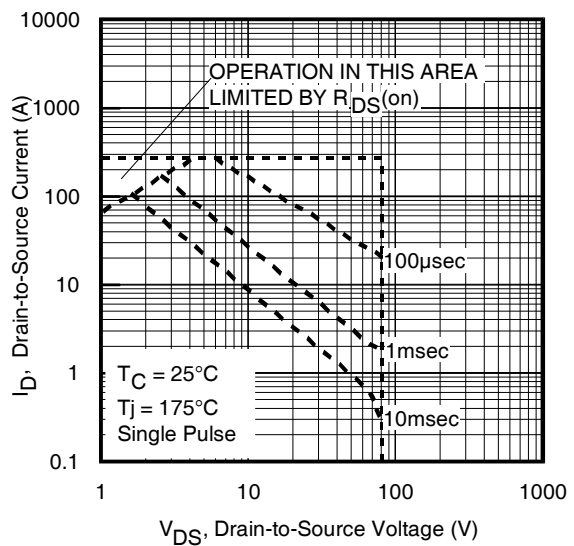


Fig 8. Maximum Safe Operating Area

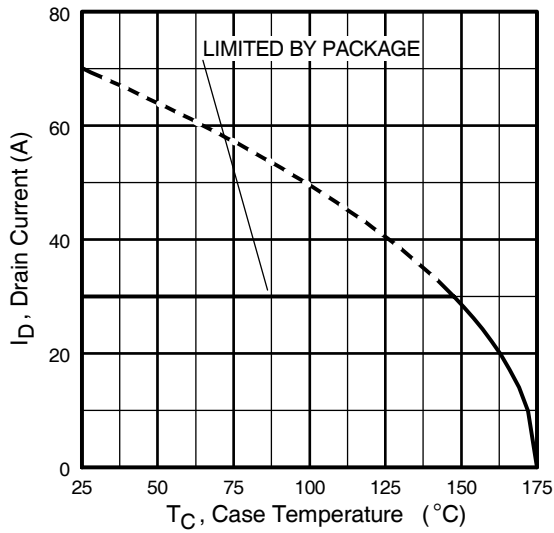


Fig 9. Maximum Drain Current Vs. Case Temperature

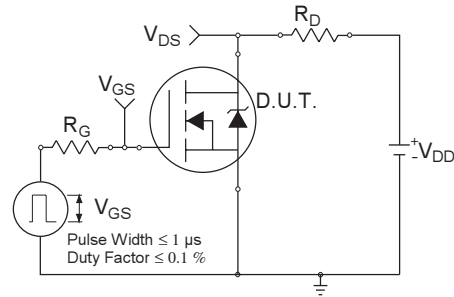


Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

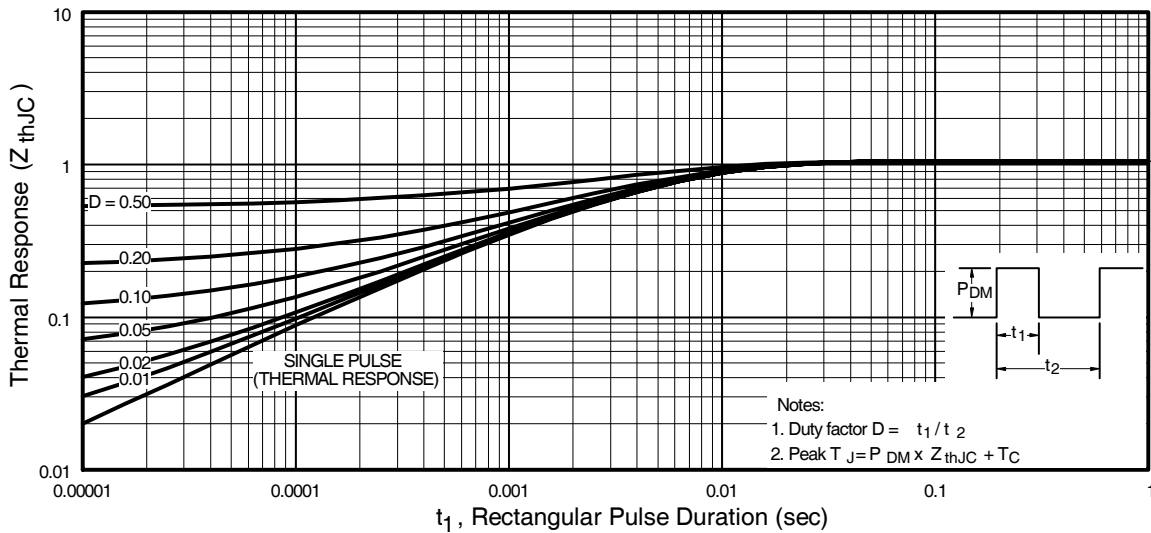


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

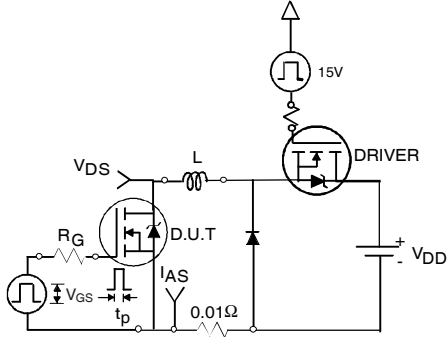


Fig 12a. Unclamped Inductive Test Circuit

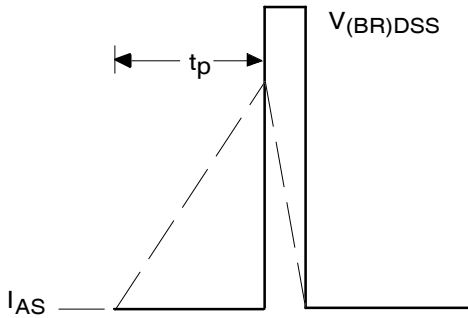


Fig 12b. Unclamped Inductive Waveforms

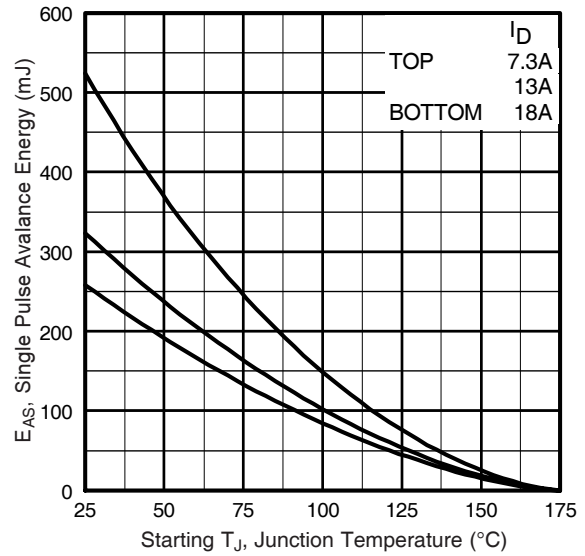


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

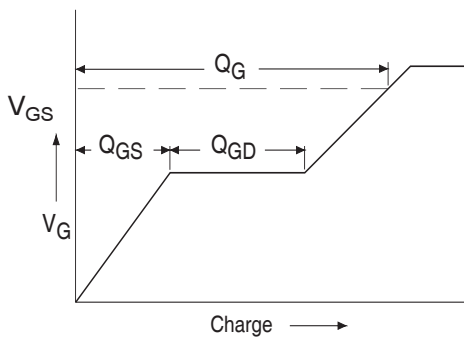


Fig 13a. Basic Gate Charge Waveform

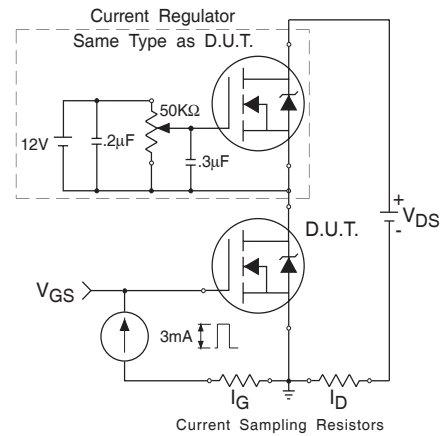
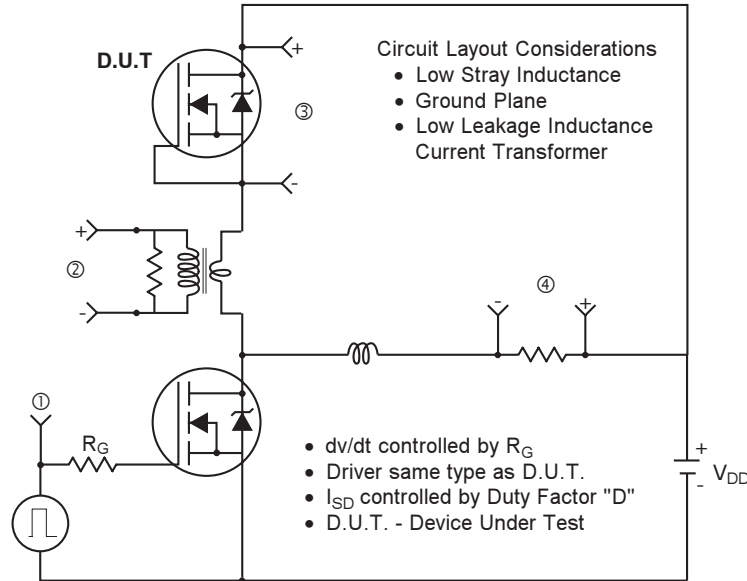


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

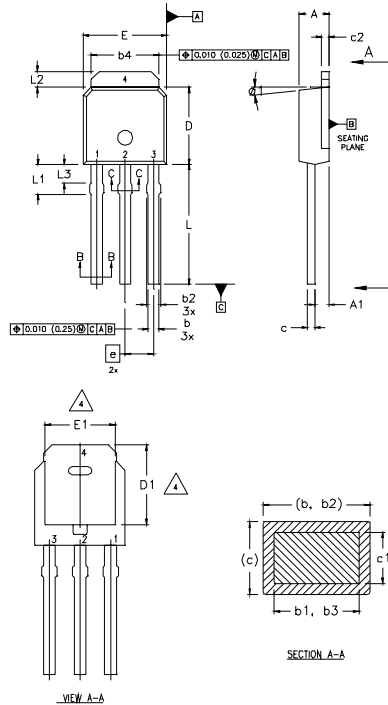
Fig 14. For N-Channel HEXFET® Power MOSFETs

IRFR/U3418

International
IR Rectifier

I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
 - 2 DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 - 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 - 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4. L2, E1 & D1.
 - 5 LEAD DIMENSION UNCONTROLLED IN L3.
 - 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
 - 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
 - 8 CONTROLLING DIMENSION : INCHES.

LEAD ASSIGNMENTS

HEXFEET

- 1.- CATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.06	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	-	0.205	-	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.52	-	0.170	-	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	Ø	15'	Ø	15'	

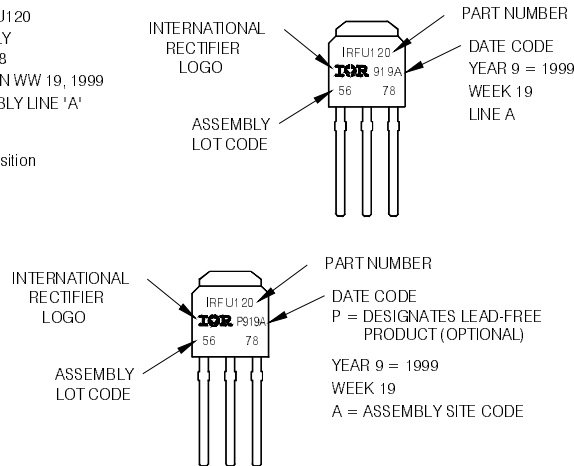
I-Pak (TO-251AA) Part Marking Information

Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 1999
IN THE ASSEMBLY LINE 'A'

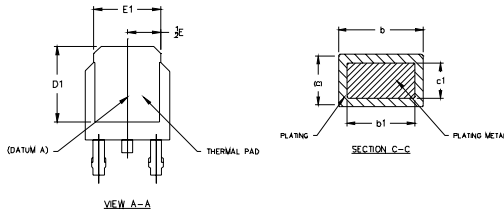
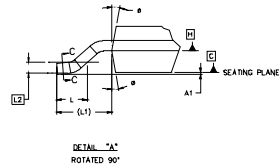
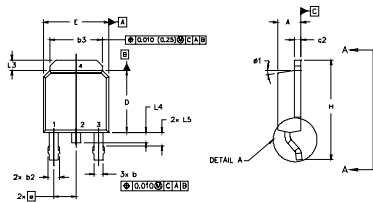
Note: 'P' in assembly line position
indicates Lead-Free'

OR



D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1.0 DIMENSIONS AND TOLERANCING PER ASME Y14.5 M - 1994.
- 2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.0 LEAD DIMENSION UNCONTROLLED IN L5
- 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 (0.127) AND .010 (0.254) FROM THE LEAD TIP.
- 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	0.15	0.15	.006	.006	
B	0.64	0.89	.025	.035	5
B1	0.54	0.79	.025	.032	5
B2	0.78	1.14	.030	.045	
B3	4.95	5.46	.195	.215	
C	0.48	0.61	.018	.024	5
C1	0.41	0.56	.016	.022	5
C2	.048	0.89	.018	.035	5
D	1.97	6.22	.235	.246	6
D1	5.21	-	.205	-	4
E	6.20	6.73	.250	.265	6
E1	4.52	-	.178	-	4
H	2.29	-	.090	.092	
H1	8.45	10.41	.332	.410	
L	1.40	1.78	.055	.070	
L1	2.74	NOF	.108	NOF	
L2	0.500	NSC	.020	NSC	
L3	0.88	1.27	.035	.050	
L4	1.14	1.52	.045	.060	
L5	1.14	1.52	.045	.060	
#	0"	10"	0"	10"	J
#1	0"	15"	0"	15"	

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

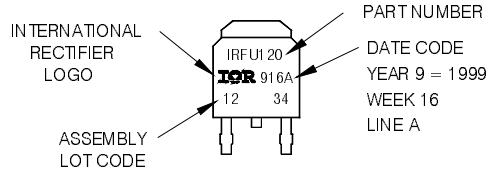
IRF16A COPACK

- 1 - GATE
- 2 - COLLECTOR
- 3 - EMITTER
- 4 - COLLECTOR

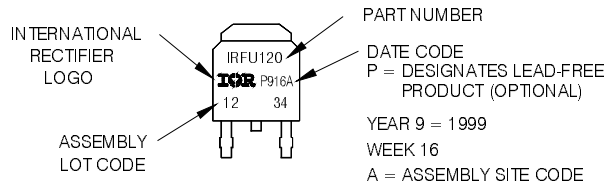
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE 'A'

Note: 'P' in assembly line position
indicates 'Lead-Free'



OR

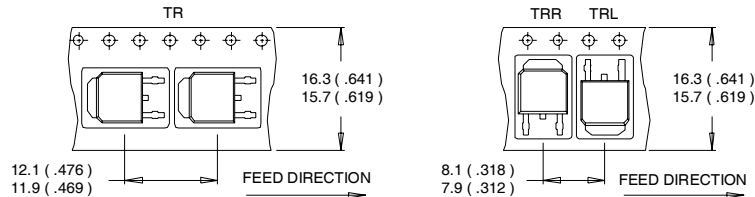


IRFR/U3418

International
IR Rectifier

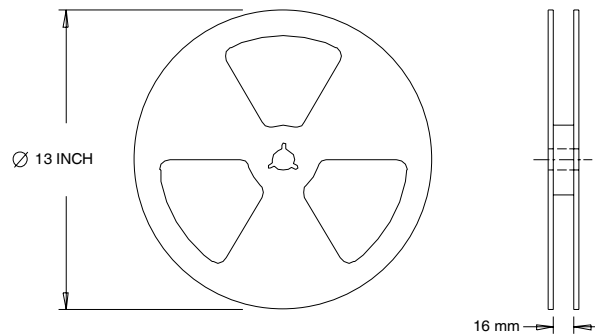
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 1.6\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 18\text{A}$.
- ③ $I_{SD} \leq 18\text{A}$, $di/dt \leq 350\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A.

* When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.

This product has been designed and qualified for the Industrial market.

Qualification Standards can be found on IR's Web site.

International
IR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.03/05

www.irf.com

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>