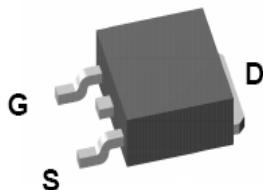


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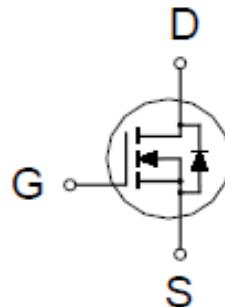
N-Channel Logic Level Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
40V	29mΩ @ $V_{GS} = 10V$	25A



TO-252



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	$T_A = 25^\circ C$	I_D	25	A
	$T_A = 70^\circ C$		20	
Pulsed Drain Current ¹		I_{DM}	75	A
Avalanche Current		I_{AS}	27	
Avalanche Energy ²	$L=0.1mH$	E_{AS}	37	mJ
Power Dissipation	$T_C = 25^\circ C$	P_D	30	W
	$T_C = 70^\circ C$		20	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$	4.1	4.1	°C / W
Junction-to-Ambient	$R_{\theta JA}$		40	

¹Pulse width limited by maximum junction temperature.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

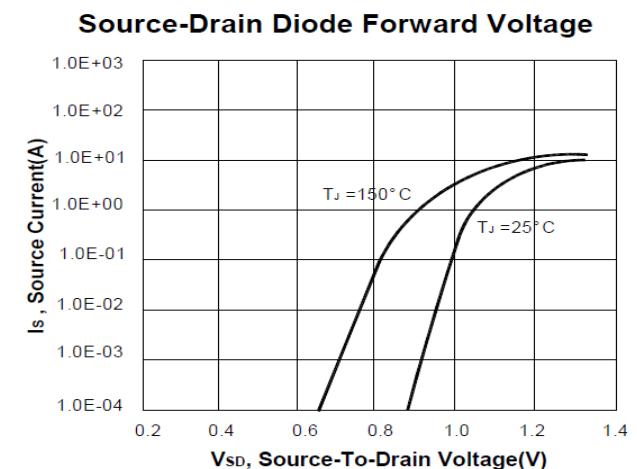
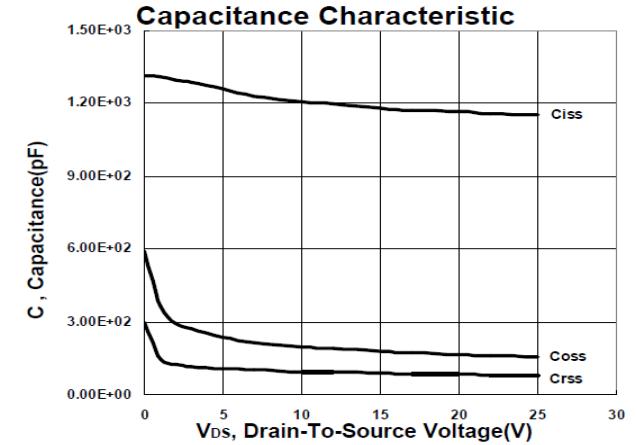
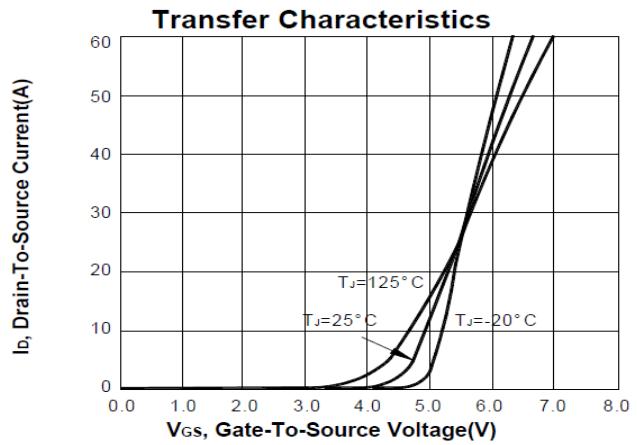
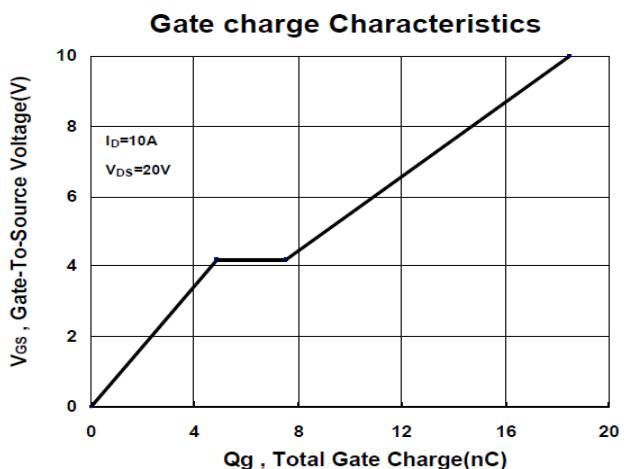
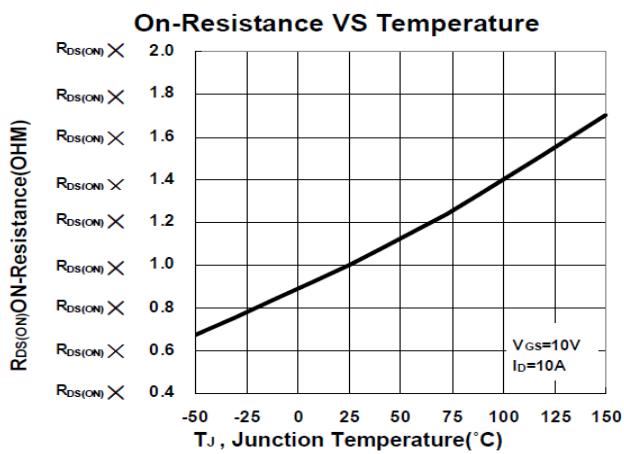
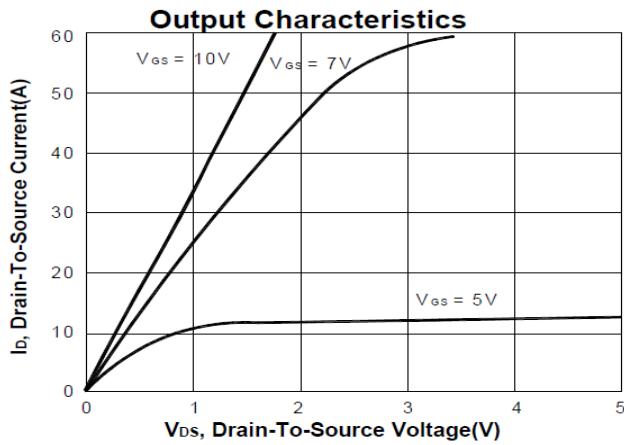
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT S
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	40			V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	2	2.4	3	
Gate-Body Leakage	I_{GSS}	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = \pm 20\text{V}$			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 32\text{V}, V_{\text{GS}} = 0\text{V}$			1	μA
		$V_{\text{DS}} = 30\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 125^\circ\text{C}$			10	
On-State Drain Current ¹	$I_{\text{D}(\text{ON})}$	$V_{\text{DS}} = 5\text{V}, V_{\text{GS}} = 10\text{V}$	75			A
Drain-Source On-State Resistance ¹	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}} = 10\text{V}, I_D = 10\text{A}$		19	29	$\text{m}\Omega$
		$V_{\text{GS}} = 7\text{V}, I_D = 8\text{A}$		22	45	
		$V_{\text{GS}} = 5\text{V}, I_D = 8\text{A}$		26	50	
Forward Transconductance ¹	g_{fs}	$V_{\text{DS}} = 5\text{V}, I_D = 10\text{A}$		30		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 20\text{V}, f = 1\text{MHz}$		1150		pF
Output Capacitance	C_{oss}			157		
Reverse Transfer Capacitance	C_{rss}			80		
Total Gate Charge ²	Q_g	$V_{\text{GS}} = 10\text{V}$		19		nC
		$V_{\text{GS}} = 4.5\text{V}$		9		
Gate-Source Charge ²	Q_{gs}	$V_{\text{DS}} = 0.5V_{(\text{BR})\text{DSS}}, I_D = 10\text{A}$		4.5		
Gate-Drain Charge ²	Q_{gd}			3		
Gate Resistance	R_g	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 0\text{V}, f = 1\text{MHz}$		1.55		Ω
Turn-On Delay Time ²	$t_{\text{d}(\text{on})}$			10		nS
Rise Time ²	t_r	$V_{\text{DS}} = 20\text{V}, R_L = 1\Omega$ $I_D \cong 1\text{A}, V_{\text{GS}} = 10\text{V}, R_{\text{GS}} = 6\Omega$		6		
Turn-Off Delay Time ²	$t_{\text{d}(\text{off})}$			26		
Fall Time ²	t_f			6		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ\text{C}$)						
Continuous Current	I_S				23	A
Forward Voltage ¹	V_{SD}	$I_F = 10\text{A}, V_{\text{GS}} = 0\text{V}$			1.3	V
Reverse Recovery Time	t_{rr}	$I_F = 10\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$		38		nS
Reverse Recovery Charge	Q_{rr}			29		nC

¹Pulse test : Pulse Width $\leq 300\ \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

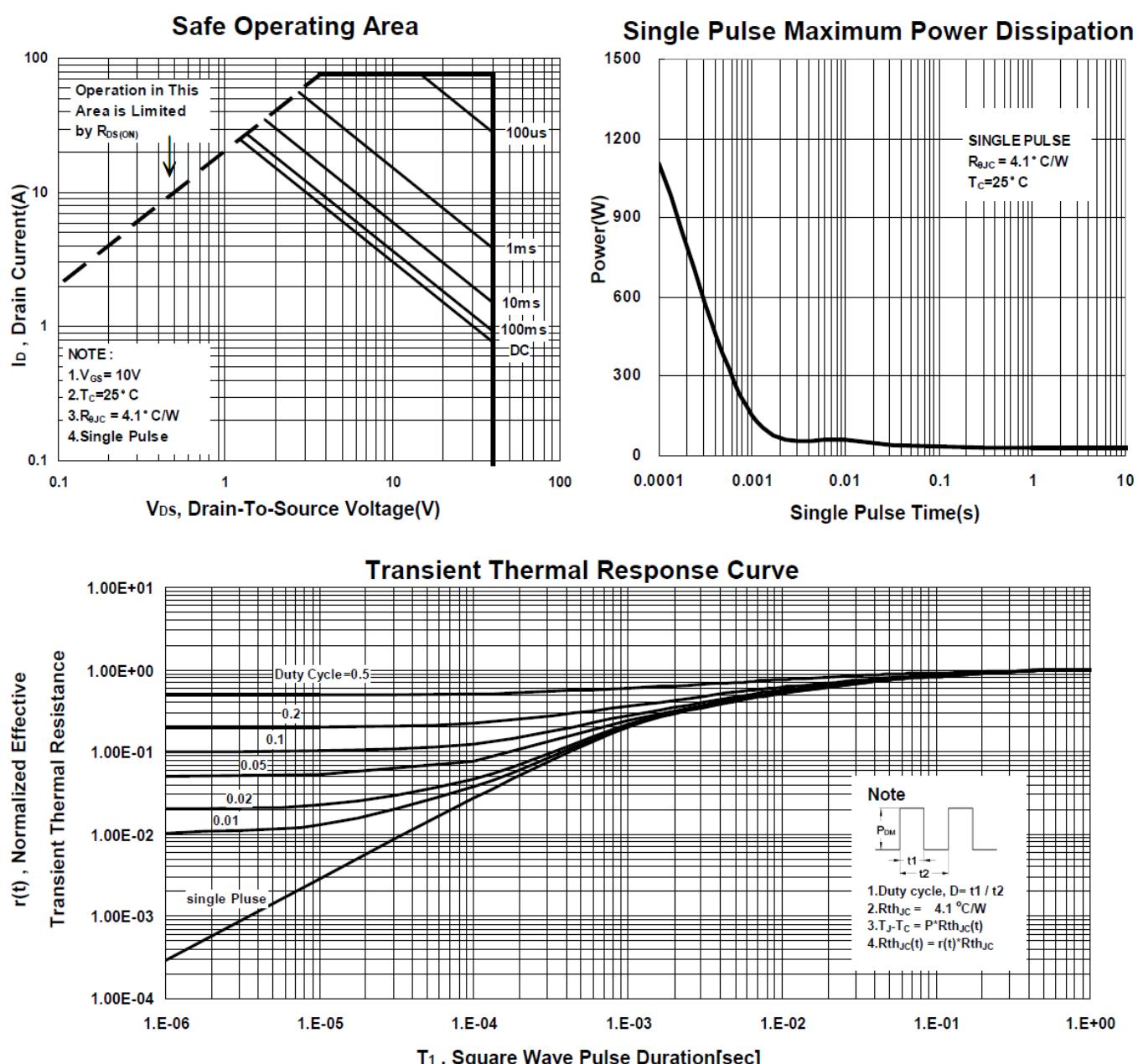
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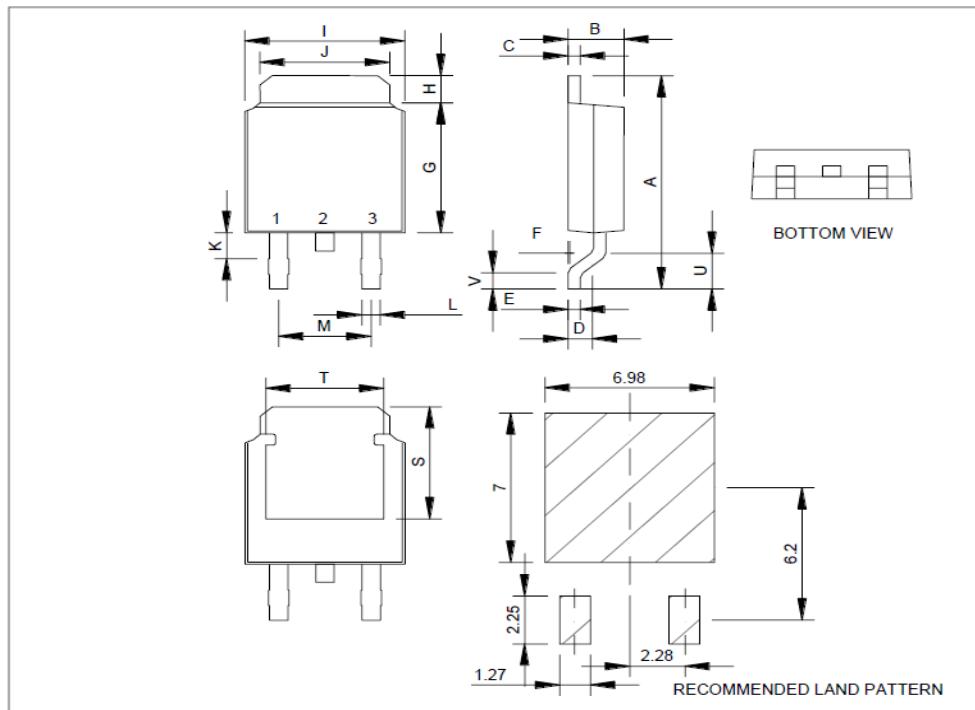
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N-Channel Logic Level Enhancement Mode MOSFET

Package Dimension

TO-252 (DPAK) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	8.9	10	10.41	J	4.8		5.64
B	2.1	2.2	2.4	K	0.15		1.1
C	0.4	0.5	0.61	L	0.4	0.76	0.89
D	0.82	1.2	1.5	M	4.2	4.58	5
E	0.4	0.5	0.61	S	4.9	5.1	5.3
F	0		0.2	T	4.6	4.75	5.44
G	5.3	6.1	6.3	U	1.4		1.78
H	0.9		1.7	V	0.55	1.25	1.7
I	6.3	6.5	6.8				



*因为各家封装模具不同而外观略有差异，不影响电性及Layout。