

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOS^{III}-H)

TK150E09NE

■ E-Bike

- Low drain-source ON resistance : $R_{DS(ON)} = 3.6\text{ m}\Omega$ (typ.) ($V_{GS} = 10\text{ V}$)
- Low leakage current : $I_{DSS} = 10\text{ }\mu\text{A}$ (max) ($V_{DS} = 85\text{ V}$)
- Enhancement mode : $V_{th} = 2.5\sim 4.5\text{ V}$ ($V_{DS} = 10\text{ V}$, $I_D = 1.0\text{ mA}$)

Absolute Maximum Ratings (Ta = 25°C)

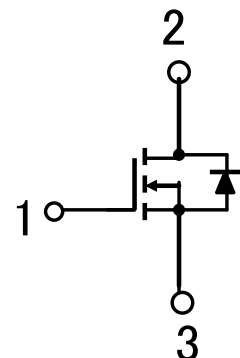
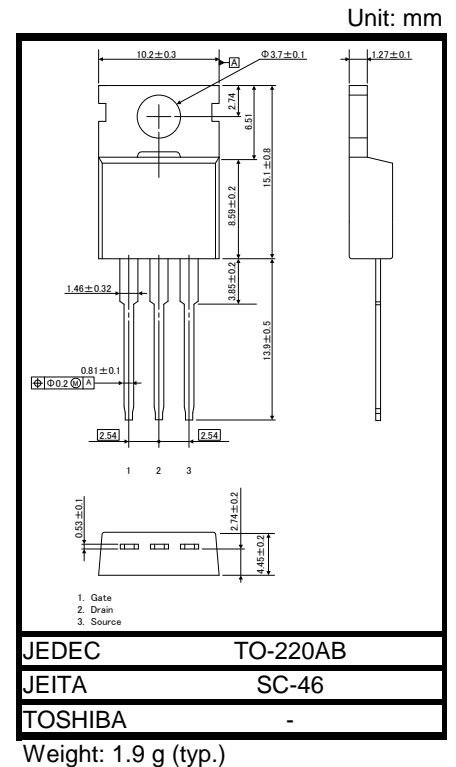
| Characteristics | Symbol | Rating | Unit |
|----------------------------------------|--------------------------|----------|------|
| Drain-source voltage | V_{DSS} | 85 | V |
| Gate-source voltage | V_{GSS} | ± 20 | |
| Drain current | DC (Tc = 25°C) (Note 1) | I_D | 150 |
| | DC (Tc = 100°C) (Note 1) | I_D | 120 |
| | Pulse (Note 1) | I_{DP} | 450 |
| Drain power dissipation (Tc = 25°C) | P_D | 230 | W |
| Single pulse avalanche energy (Note 2) | E_{AS} | 161 | mJ |
| Avalanche current (Note 2) | I_{AS} | 72 | A |
| Peak diode recovery dv/dt (Note 5) | dv/dt | 12 | V/ns |
| Channel temperature | T_{ch} | 175 | °C |
| Storage temperature range | T_{stg} | -55~175 | |

Thermal Characteristics

| Characteristics | Symbol | Max | Unit |
|----------------------------------------|----------------|------|--------|
| Thermal resistance, channel to case | $R_{th(ch-c)}$ | 0.65 | °C / W |
| Thermal resistance, channel to ambient | $R_{th(ch-a)}$ | 83.3 | |

- Note 1: Ensure that the channel temperature does not exceed 175°C.
 Note 2: $V_{DD} = 64\text{ V}$, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 24\text{ }\mu\text{H}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 72\text{ A}$
 Note 3: Repetitive rating: pulse width limited by maximum channel temperature
 Note 4: $I_{DR} \leq 180\text{ A}$, $di/dt \leq 160\text{ A}/\mu\text{s}$, $T_{ch} \leq T_{ch\text{ max}}$.
 This transistor is an electrostatic-sensitive device.
 Please handle with caution.

Note :Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
 Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).Thermal Characteristics



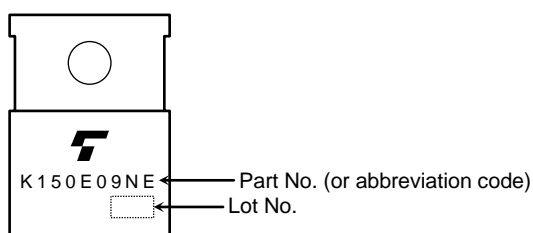
Electrical Characteristics (Ta = 25°C)

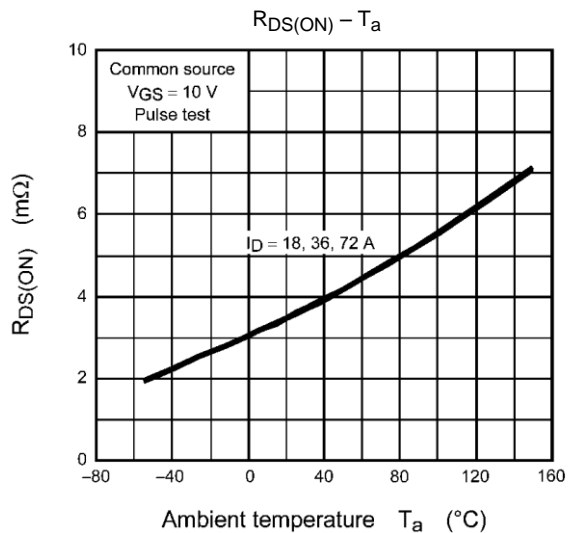
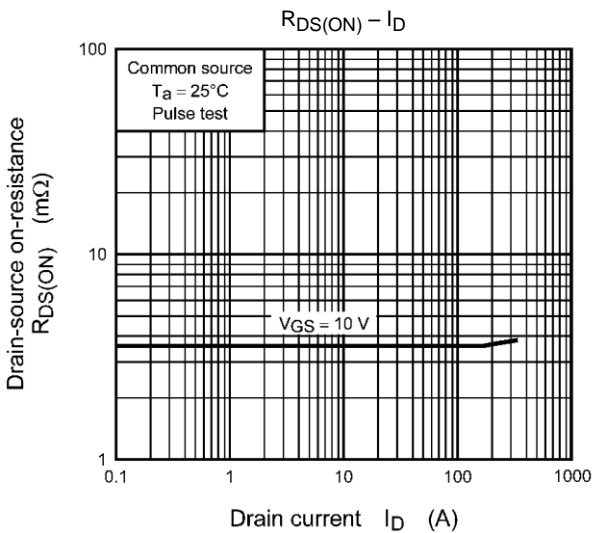
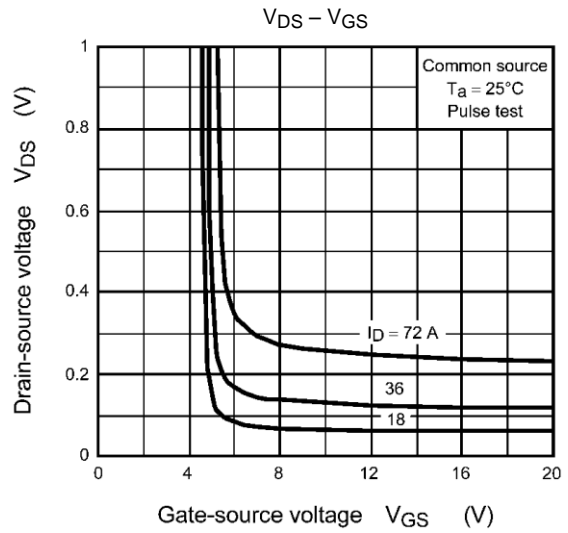
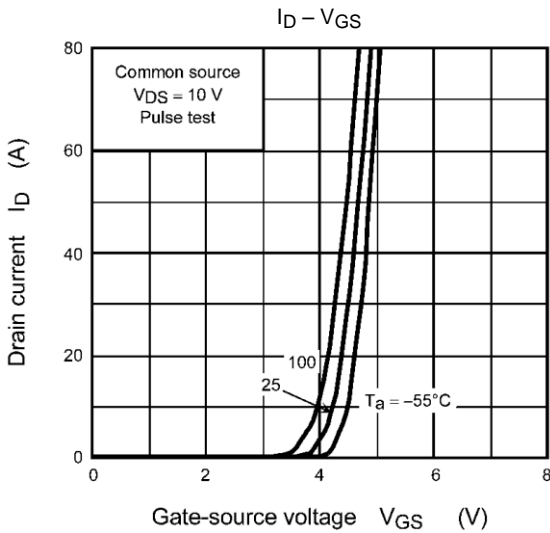
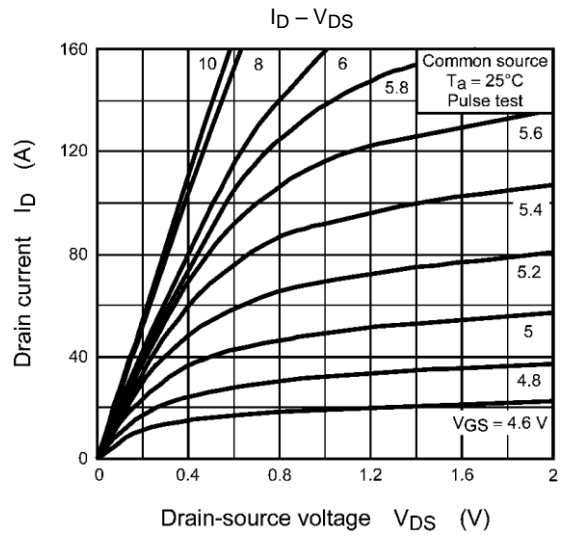
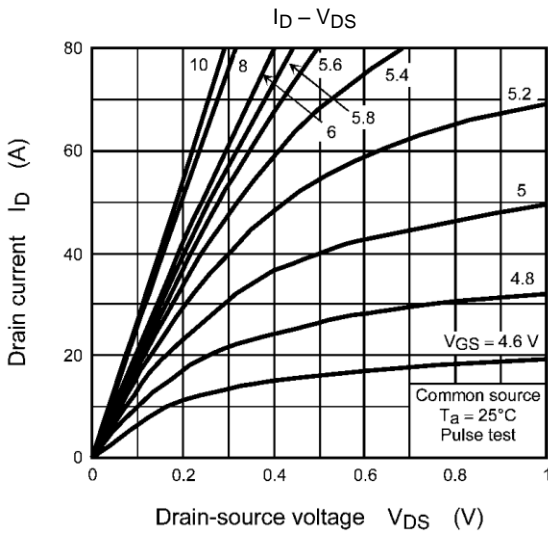
| Characteristics | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|-------------------------------------------------|---------------|---------------|-----------------------------------------------------------------------|-----|------|-----------|------------------|
| Gate leakage current | | I_{GSS} | $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ | — | — | ± 0.1 | μA |
| Drain cut-off current | | I_{DSS} | $V_{DS} = 85\text{ V}, V_{GS} = 0\text{ V}$ | — | — | 10 | |
| Drain-source breakdown voltage | | $V_{(BR)DSS}$ | $I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$ | 85 | — | — | V |
| Drain-source breakdown voltage | | $V_{(BR)DSX}$ | $I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$ | 60 | — | — | |
| Gate threshold voltage | | V_{th} | $V_{DS} = 10\text{ V}, I_D = 1.0\text{ mA}$ | 2.5 | — | 4.5 | |
| Drain-source ON resistance | | $R_{DS(ON)}$ | $V_{GS} = 10\text{ V}, I_D = 75\text{ A}$ | — | 3.65 | 5.0 | $\text{m}\Omega$ |
| Input capacitance | | C_{iss} | $V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | — | 5500 | — | pF |
| Reverse transfer capacitance | | C_{rss} | | — | 38 | — | |
| Output capacitance | | C_{oss} | | — | 1300 | — | |
| Switching time | Rise time | t_r | | — | 19 | — | ns |
| | Turn-on time | t_{on} | | — | 42 | — | |
| | Fall time | t_f | | — | 28 | — | |
| | Turn-off time | t_{off} | | — | 93 | — | |
| Total gate charge (Gate-source plus gate-drain) | | Q_g | $V_{DD} \approx 64\text{ V}, V_{GS} = 10\text{ V}, I_D = 72\text{ A}$ | — | 81 | — | nC |
| Gate-source charge 1 | | Q_{gs1} | | — | 29 | — | |
| Gate-drain charge | | Q_{gd} | | — | 21 | — | |
| Gate switch charge | | Q_{SW} | | — | 33 | — | |

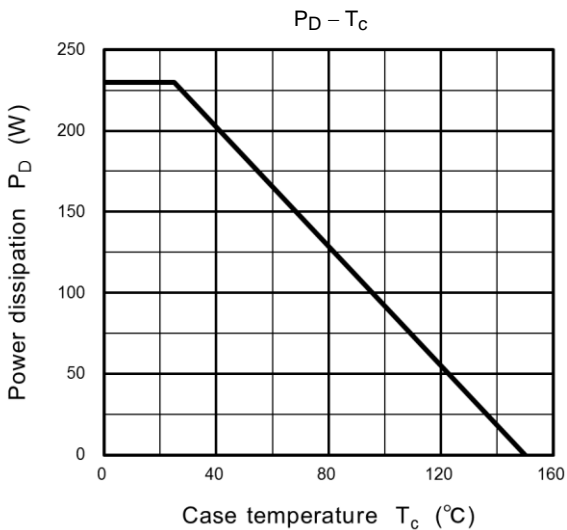
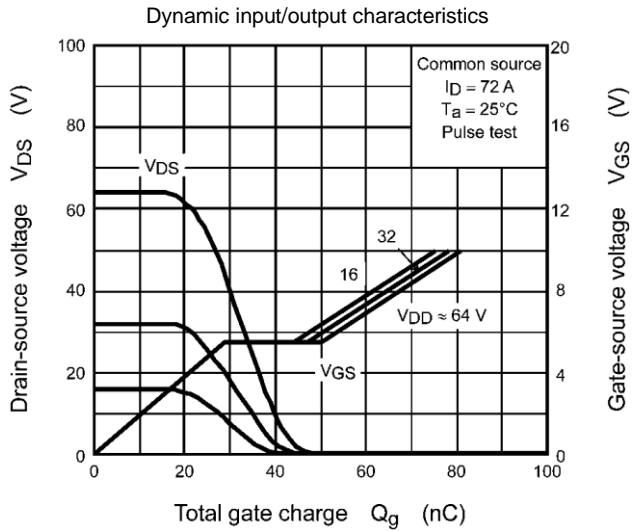
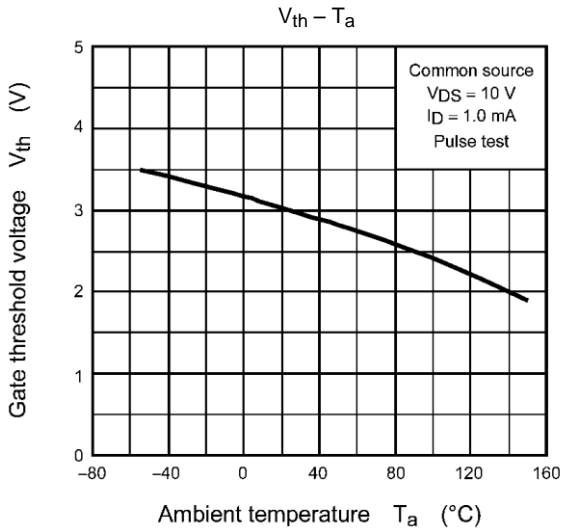
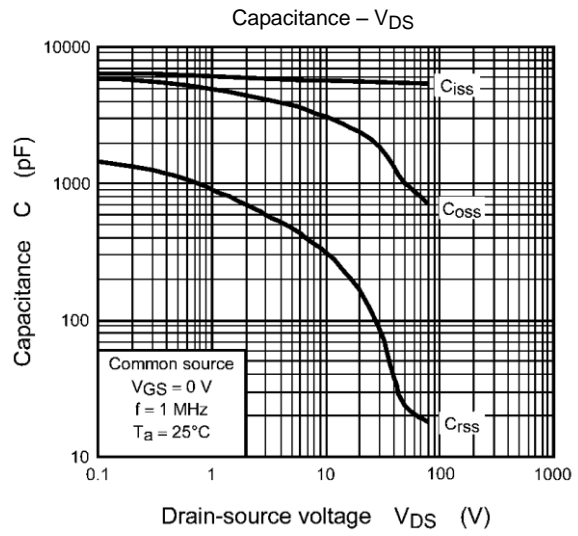
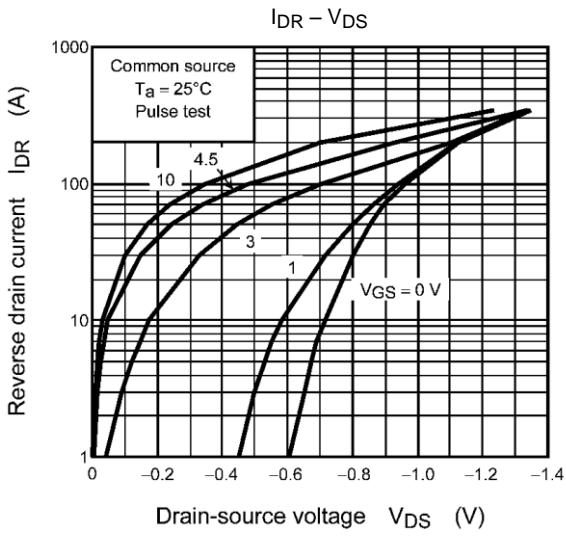
Source-Drain Ratings and Characteristics (Ta = 25°C)

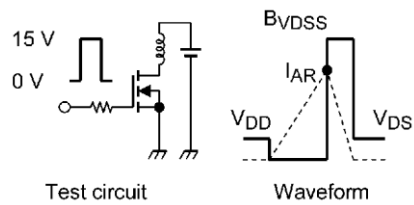
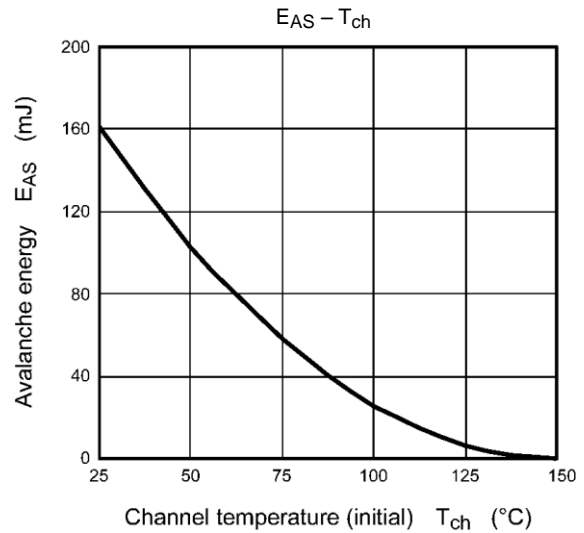
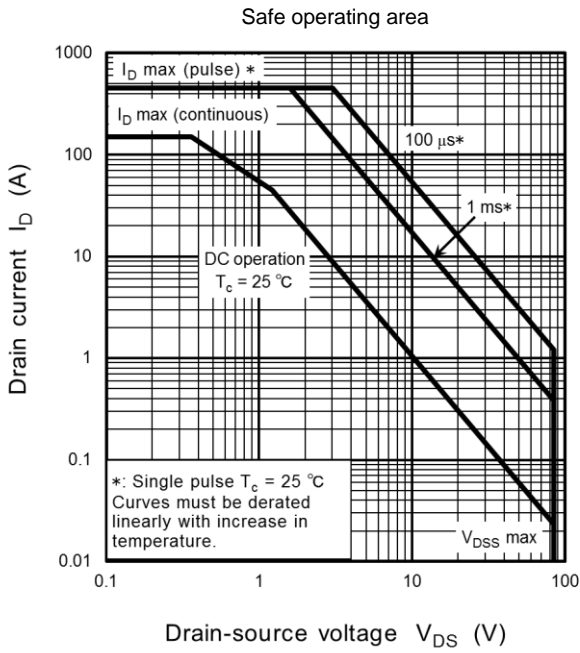
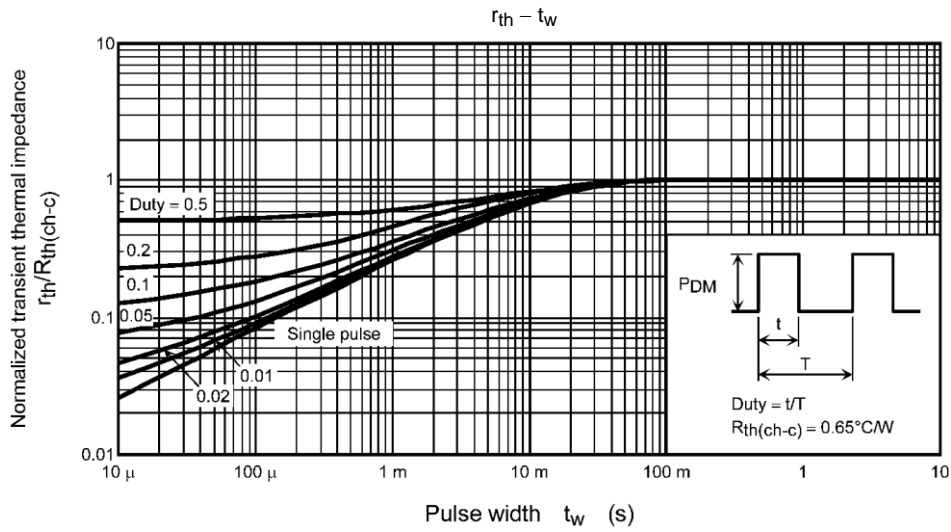
| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|-------------------------------------------------------|-----------|----------------------------------------------|-----|------|------|------|
| Continuous drain reverse current (Tc = 25°C) (Note 1) | I_{DR} | — | — | — | 150 | A |
| Pulse drain reverse current (Note 1) | I_{DRP} | — | — | — | 450 | A |
| Forward voltage (diode) | V_{DSF} | $I_{DR} = 150\text{ A}, V_{GS} = 0\text{ V}$ | — | — | -1.3 | V |
| Reverse recovery time | t_{rr} | $I_{DR} = 72\text{ A}, V_{GS} = 0\text{ V}$ | — | 77 | — | ns |
| Reverse recovery charge | Q_{rr} | $-dI_{DR} / dt = 100\text{ A} / \mu\text{s}$ | — | 150 | — | nC |

Marking









$$V_{DD} = 64 \text{ V}, I_{AR} = 72 \text{ A} \quad E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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