TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOSIV)

TK80A08K3

Switching Regulator Applications

• Low drain-source ON-resistance: R_{DS} (ON) = 3.6 m Ω (typ.)

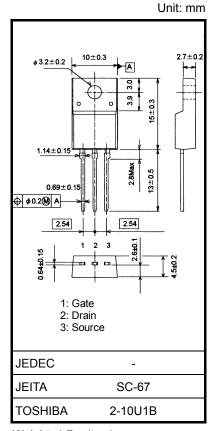
• High forward transfer admittance: $|Y_{fs}| = 200 \text{ S}$

• Low leakage current: $IDSS = 10 \mu A (max) (VDS = 75 V)$

• Enhancement mode: $V_{th} = 2.0$ to 4.0 V ($V_{DS} = 10$ V, $I_{D} = 1$ mA)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit		
Drain-source voltage			V_{DSS}	75	V	
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)			V_{DGR}	75	V	
Gate-source voltage			V _{GSS}	± 20	V	
Drain current	DC (Not	te 1)	ID	80	Α	
	Pulse (Not	e 1)	I _{DP}	320	A 	
Drain power dissipation (Tc = 25°C)			P_{D}	40	W	
Single pulse avalanche energy (Note 2)			E _{AS}	443	mJ	
Avalanche current			I _{AR}	80	Α	
Repetitive avalanche energy (Note 3)			E _{AR}	4	mJ	
Channel temperature			T _{ch}	150	°C	
Storage temperature range			T _{stg}	-55 to 150	°C	



Weight: 1.7 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	R _{th (ch-c)}	3.125	°C/W
Thermal resistance, channel to ambient	R _{th (ch-a)}	62.5	°C/W

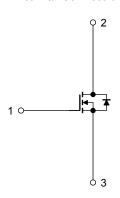
Note 1: Ensure that the channel and lead temperatures do not exceed 150°C.

Note 2: $~V_{DD}=25$ V, $T_{ch}=25^{\circ}C,~L=100~\mu H,~I_{AR}=80$ A, $R_{G}=1~\Omega$

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device. Handle with care.

Internal Connection



Electrical Characteristics (Ta = 25°C)

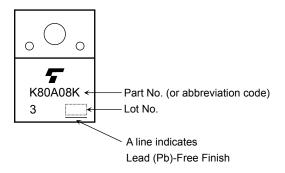
Chara	cteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage cur	rent	nt I_{GSS} $V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$		_	_	±1	μА
Drain cut-OFF cu	rrent	I _{DSS}	V _{DS} = 75 V, V _{GS} = 0 V	_	_	10	μА
Drain-source breakdown voltage		V (BR) DSS	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	75	_		V
		V (BR) DSX	$I_D = 10 \text{ mA}, V_{GS} = -20 \text{ V}$	55	_	_	
Gate threshold vo	oltage	V _{th}	V _{DS} = 10 V, I _D = 1 mA	2.0	_	4.0	V
Drain-source ON-	-resistance (Note 4)	R _{DS} (ON)	V _{GS} = 10 V, I _D = 40A		3.6	4.5	mΩ
Forward transfer	admittance	Y _{fs}	V _{DS} = 10 V, I _D = 40 A	100	200	_	S
Input capacitance Reverse transfer capacitance Output capacitance		C _{iss}	V _{DS} = 10V, V _{GS} = 0 V, f = 1 MHz	_	8200	_	pF
		C _{rss}		_	770	_	
		C _{oss}		_	1140	_	
Switching time	Rise time	t _r	V_{GS} 0 V V_{GS} 0 V 0	_	30	_	ns
	Turn-ON time	t _{on}			55		
	Fall time	t _f			33		
	Turn-OFF time	t _{off}		l	150		
Total gate charge (gate-source plus gate-drain) Gate-source charge 1		Qg	$V_{DD} \simeq 60 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 80 \text{A}$	_	175	_	nC
		Q _{gs1}		_	40	_	
Gate-drain ("miller") charge		Q _{gd}		_	65	_	
Gate switch charge		Q_{SW}		_	80	_	

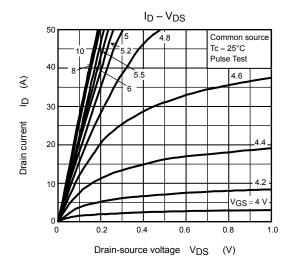
Note 4: Measured at lead standoff.

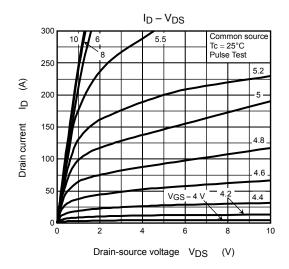
Source-Drain Ratings and Characteristics (Ta = 25°C)

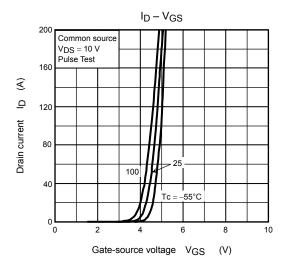
Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Continuous drain reverse current (Note 1)	I _{DR}	_	_	_	80	Α
Pulse drain reverse current (Note 1)	I _{DRP}	_	_	_	320	Α
Forward voltage (diode)	V _{DSF}	I _{DR} = 80 A, V _{GS} = 0 V	_	-0.9	-1.2	V
Reverse recovery time	t _{rr}	I _{DR} = 80 A, V _{GS} = 0 V,	_	60	_	ns
Reverse recovery charge	Q _{rr}	dI _{DR} /dt = 50 A/μs	_	60	_	nC

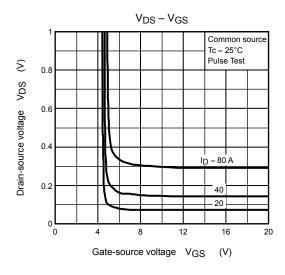
Marking

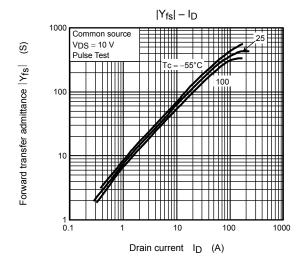


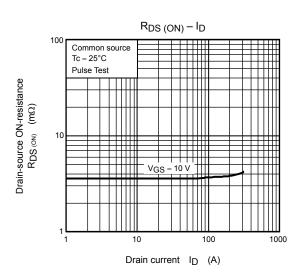


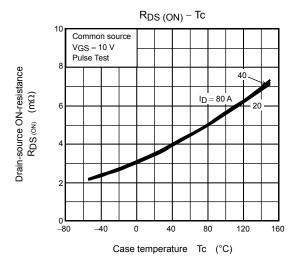


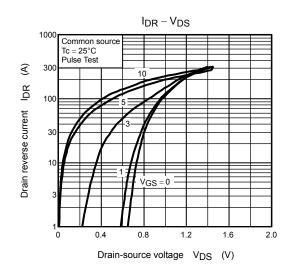


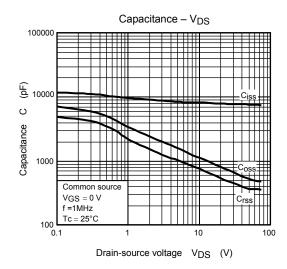


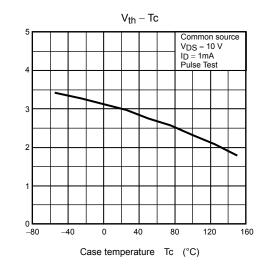


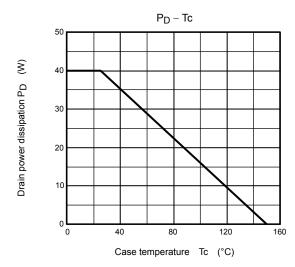


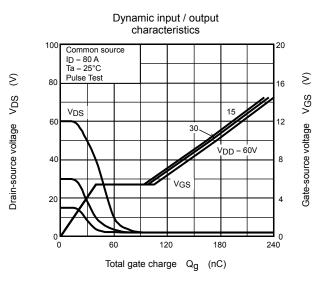






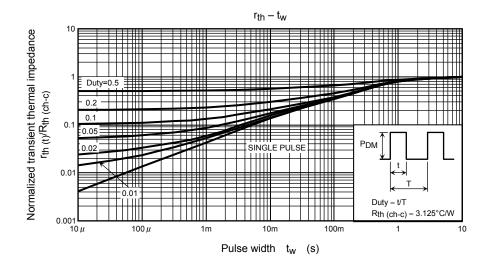


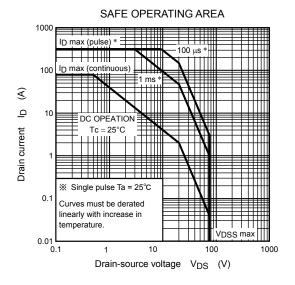


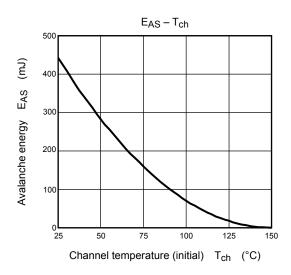


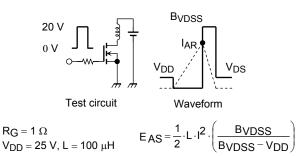
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Gate threshold voltage Vth









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20070701-EN GENERAL

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