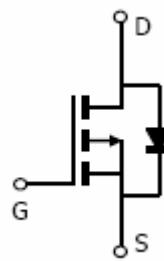


FNK P-Channel Enhancement Mode Power MOSFET

Description

The FNK3070PC/D uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.



Schematic diagram

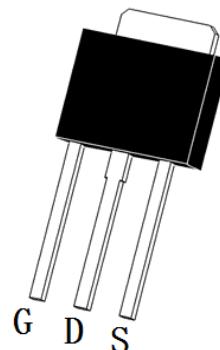
General Features

- $V_{DS} = -30V$, $I_D = -70A$
- $R_{DS(ON)} < 8.3 \text{ m}\Omega$ @ $V_{GS} = -10V$

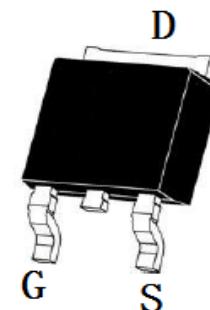
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Battery and loading switching



TO-251 top view



TO-252-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
3070PC	FNK3070PC	TO-251(SIPARK)	-	-	-
3070PD	FNK3070PD	TO-252(DPARK)	-	-	-

Absolute Maximum Ratings ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-70	A
Pulsed Drain Current	I_{DM}	-280	A
Maximum Power Dissipation	P_D	50	W
Derating factor		0.28	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 5)	E_{AS}	158	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	3.6	$^\circ\text{C/W}$
--	-----------------	-----	--------------------

Electrical Characteristics (TC=25°C unless otherwise noted)

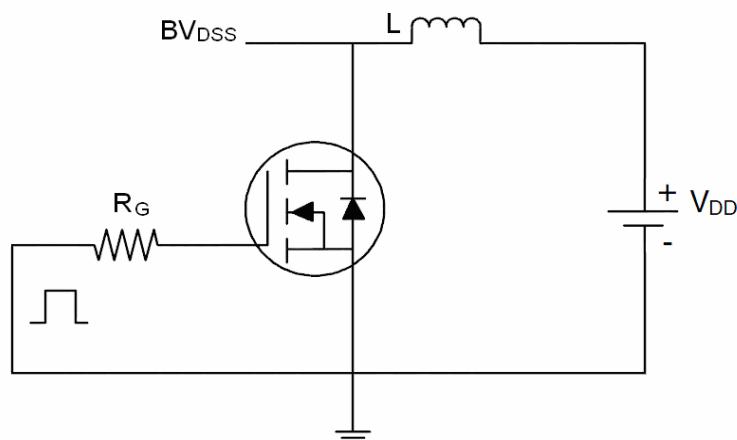
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	V_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30	-33	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.7	-1.2	-1.8	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-10A$	-	7	8.3	$m\Omega$
Forward Transconductance	g_{FS}	$V_{DS}=-10V, I_D=-15A$	-	20	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V, F=1.0MHz$	-	3515	-	PF
Output Capacitance	C_{oss}		-	410	-	PF
Reverse Transfer Capacitance	C_{rss}		-	355	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-15V, I_D=-10A$ $V_{GS}=-10V, R_{GEN}=6\Omega$	-	13	-	nS
Turn-on Rise Time	t_r		-	12	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	48	-	nS
Turn-Off Fall Time	t_f		-	14	-	nS
Total Gate Charge	Q_g	$V_{DS}=-15V, I_D=-10A, V_{GS}=-10V$	-	84	-	nC
Gate-Source Charge	Q_{gs}		-	11.9	-	nC
Gate-Drain Charge	Q_{gd}		-	25	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=-10A$	-	-0.85	-1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	-50	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ C, IF = -10A$ $di/dt = 100A/\mu s$ (Note 3)	-	-	49	nS
Reverse Recovery Charge	Q_{rr}		-	-	43	nC

Notes:

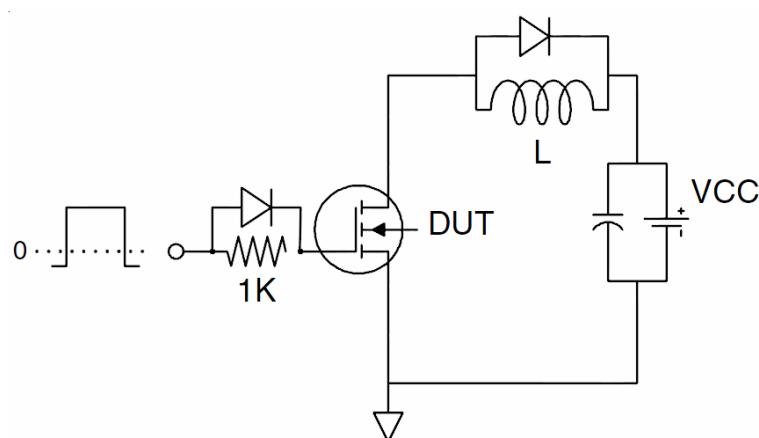
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_j=25^\circ C, V_{DD}=-15V, V_G=-10V, L=0.5mH, R_g=25\Omega$

Test Circuit

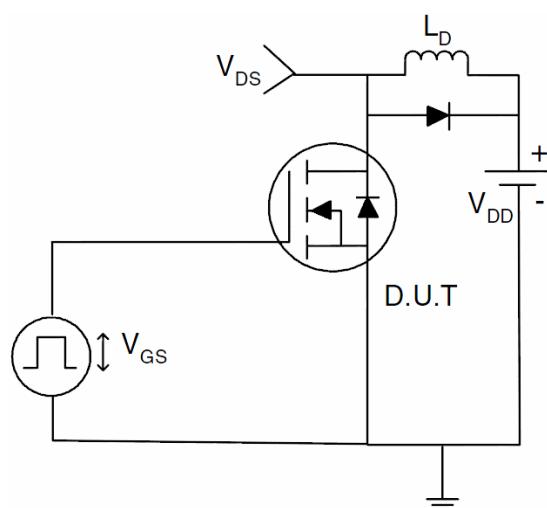
1) E_{AS} Test Circuits

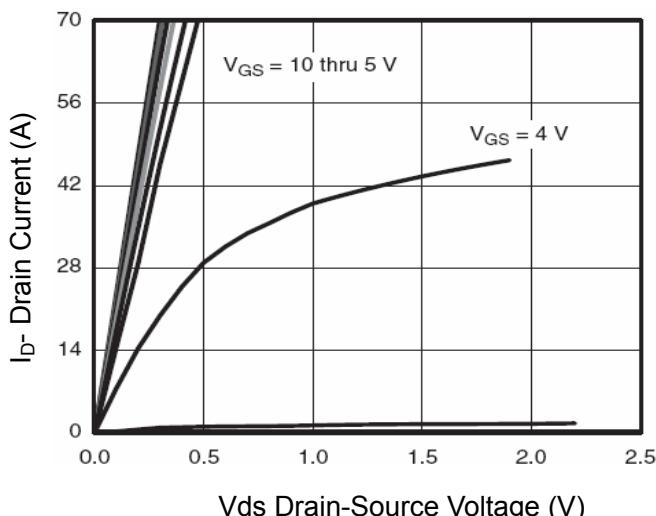
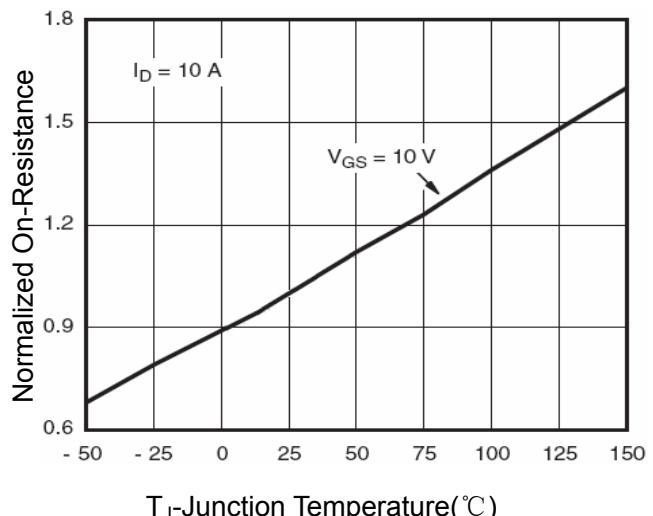
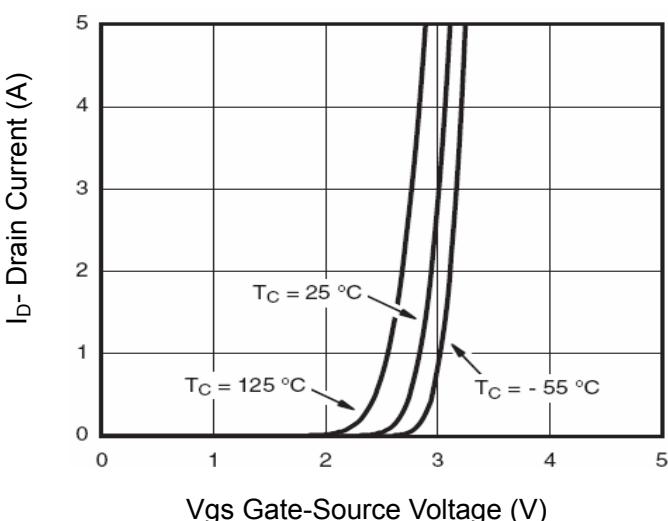
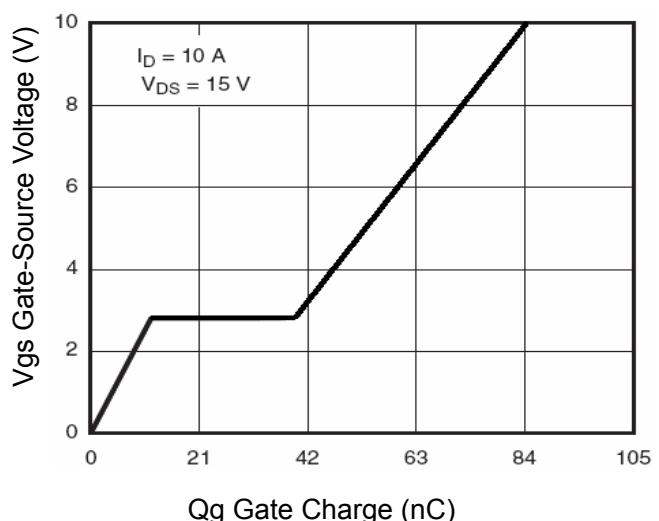
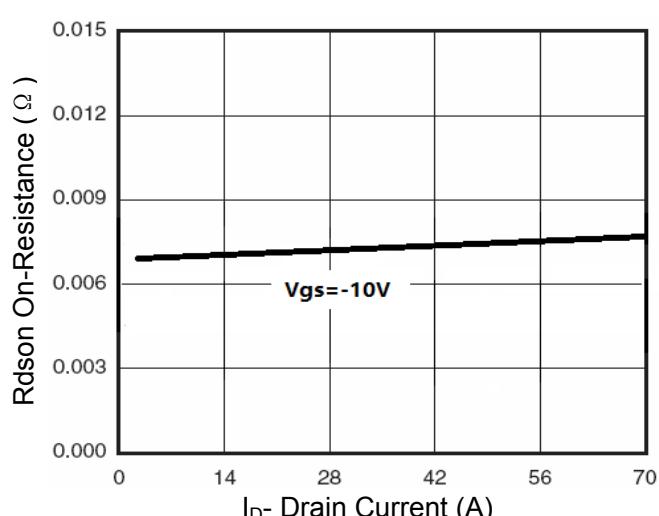
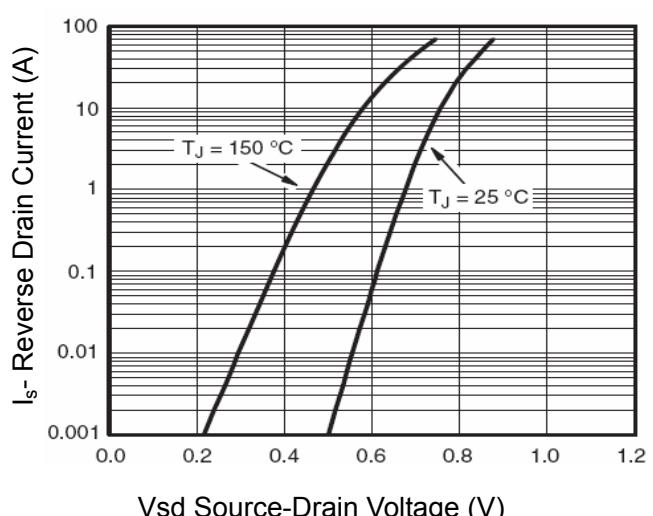


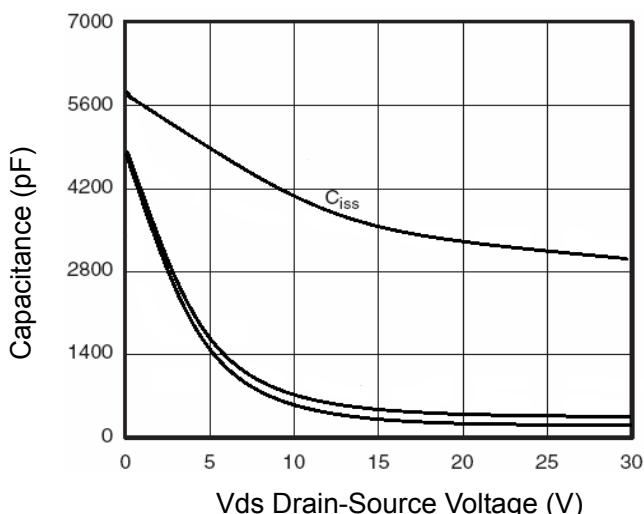
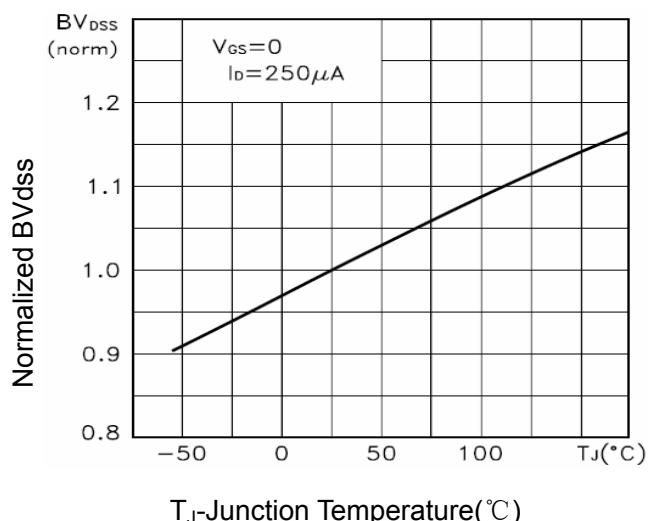
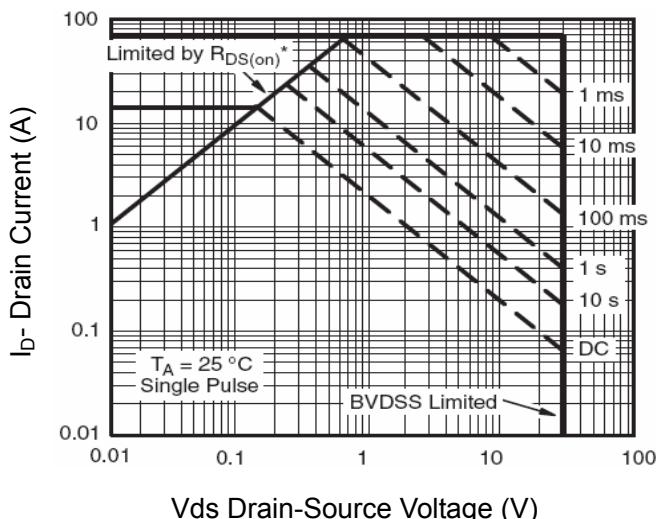
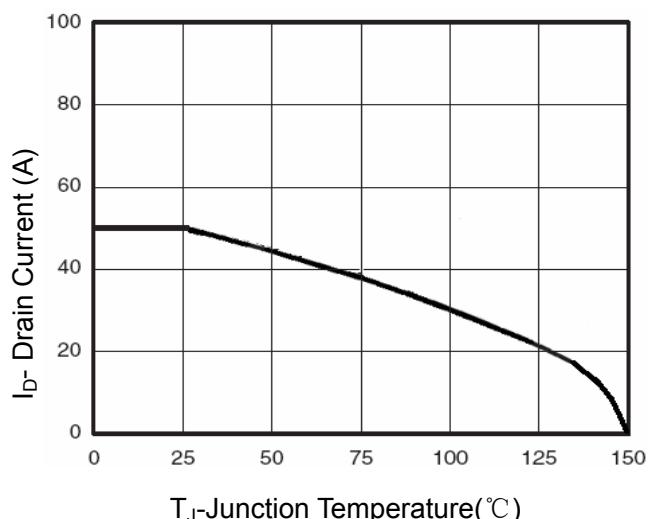
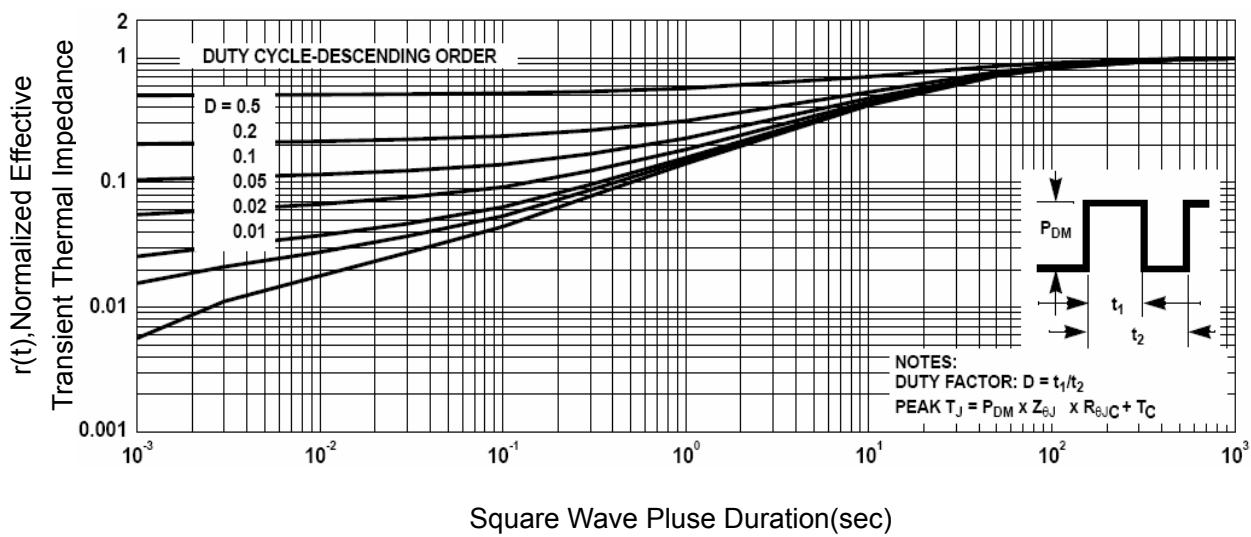
2) Gate Charge Test Circuit



3) Switch Time Test Circuit

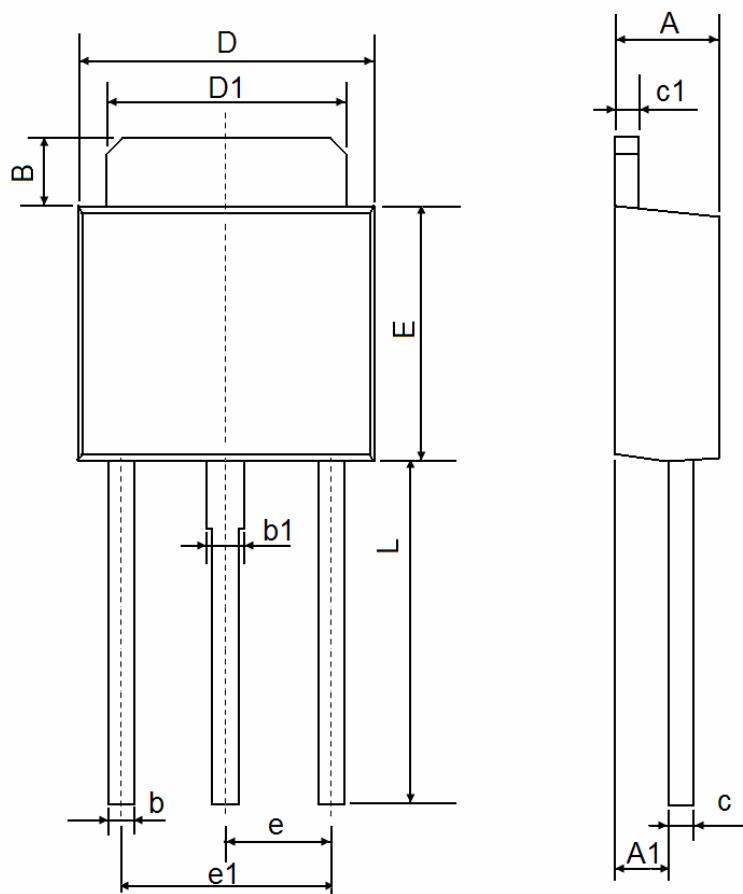


Typical Electrical and Thermal Characteristics (Curves)

Figure 1 Output Characteristics

Figure 4 Rdson-Junction Temperature

Figure 2 Transfer Characteristics

Figure 5 Gate Charge

Figure 3 Rdson- Drain Current

Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 BV_{dss} vs Junction Temperature

Figure 8 Safe Operation Area

Figure 10 I_D Current Derating vs Junction Temperature

Figure 11 Normalized Maximum Transient Thermal Impedance

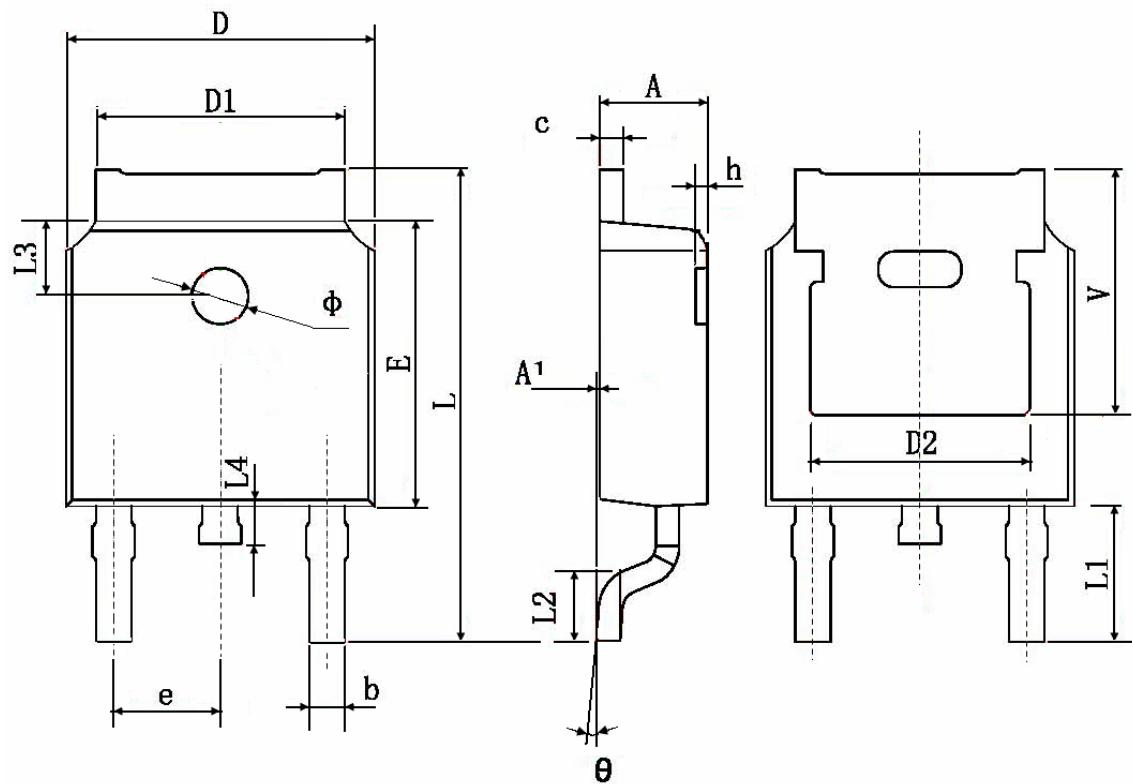


TO-251 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	1.050	1.350	0.042	0.054
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP.		0.091 TYP.	
e1	4.500	4.700	0.177	0.185
L	7.500	7.900	0.295	0.311

TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

Disclaimer:

- FNK reserves the right to make changes to the information herein for the improvement of the design and performance without further notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
- All semiconductor products malfunction or fail with some probability under special conditions. When using FNK products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.
- FNK will supply the best possible product for customers!