

# MOS FIELD EFFECT POWER TRANSISTOR

## 2SK2131

### SWITCHING

### N-CHANNEL POWER MOS FET

### INDUSTRIAL USE

#### DESCRIPTION

The 2SK2131 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

#### FEATURES

- Low On-state Resistance.  
 $R_{DS(on)} \leq 0.12 \Omega$  ( $V_{GS} = -10 \text{ V}$ ,  $I_D = 8 \text{ A}$ )  
 $R_{DS(on)} \leq 0.20 \Omega$  ( $V_{GS} = -4 \text{ V}$ ,  $I_D = 8 \text{ A}$ )
- Low  $C_{iss}$   $C_{iss} = 1\,600 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diode

#### QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

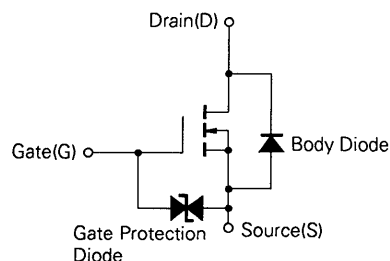
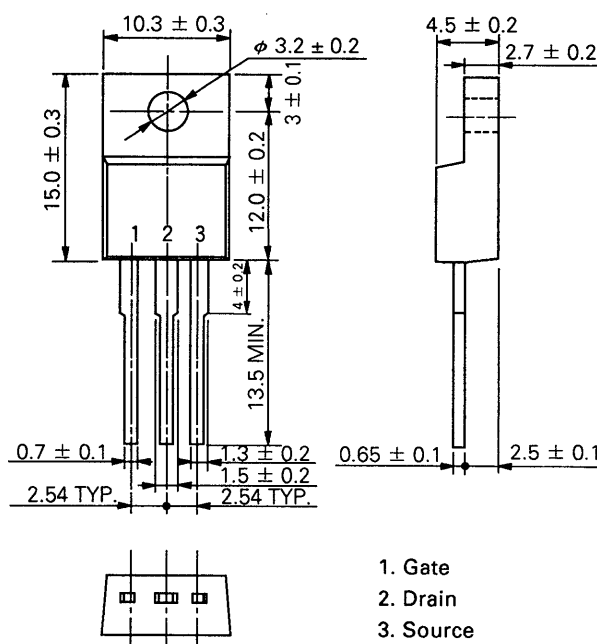
#### ABSOLUTE MAXIMUM RATINGS ( $T_a = 25^\circ\text{C}$ )

Drain to Source Voltage	$V_{DS}$	150	V
Gate to Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current (DC)	$I_D(\text{DC})$	$\pm 15$	A
Drain Current (pulse)	$I_D(\text{pulse})^*$	$\pm 60$	A
Total Power Dissipation ( $T_c = 25^\circ\text{C}$ )	$P_{T1}$	35	W
Total Power Dissipation ( $T_a = 25^\circ\text{C}$ )	$P_{T2}$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

\*  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

#### PACKAGE DIMENSIONS

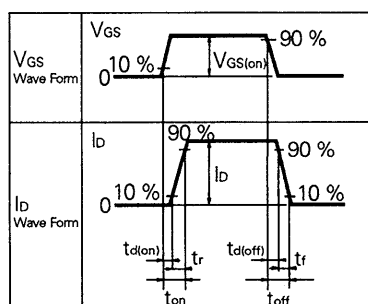
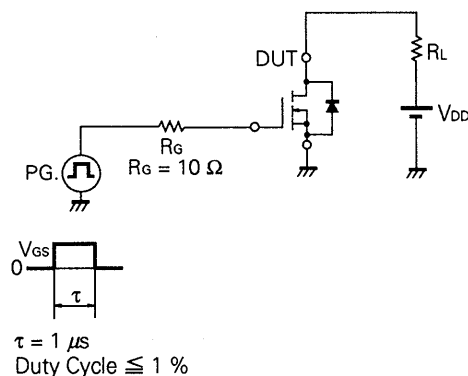
in millimeters



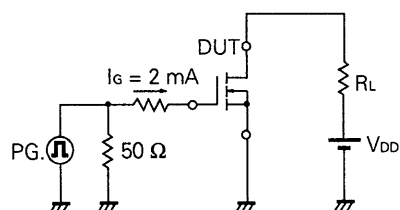
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		0.09	0.12	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 8 A
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		0.12	0.20	Ω	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 8 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	1.0		2.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	Y <sub>fs</sub>	10			S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 8 A
Drain Leakage Current	I <sub>DSS</sub>			10	μA	V <sub>DS</sub> = 150 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		1600		pF	V <sub>DS</sub> = 10 V V <sub>GS</sub> = 0 f = 1 MHz
Output Capacitance	C <sub>oss</sub>		360		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>		160		pF	
Turn-On Delay Time	t <sub>d(on)</sub>		20		ns	V <sub>GS(on)</sub> = 10 V V <sub>DD</sub> = 100 V I <sub>D</sub> = 8 A, R <sub>G</sub> = 10 Ω R <sub>L</sub> = 12.5 Ω
Rise Time	t <sub>r</sub>		50		ns	
Turn-Off Delay Time	t <sub>d(off)</sub>		200		ns	
Fall Time	t <sub>f</sub>		110		ns	
Total Gate Charge	Q <sub>G</sub>		60		nC	V <sub>GS</sub> = 10 V I <sub>D</sub> = 15 A V <sub>DD</sub> = 120 V
Gate to Source Charge	Q <sub>GS</sub>		4		nC	
Gate to Drain Charge	Q <sub>GD</sub>		20		nC	
Diode Forward Voltage	V <sub>SD</sub>		1.0		V	I <sub>F</sub> = 15 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		170		ns	I <sub>F</sub> = 15 A di/dt = 50 A/μs
Reverse Recovery Charge	Q <sub>rr</sub>		500		nC	

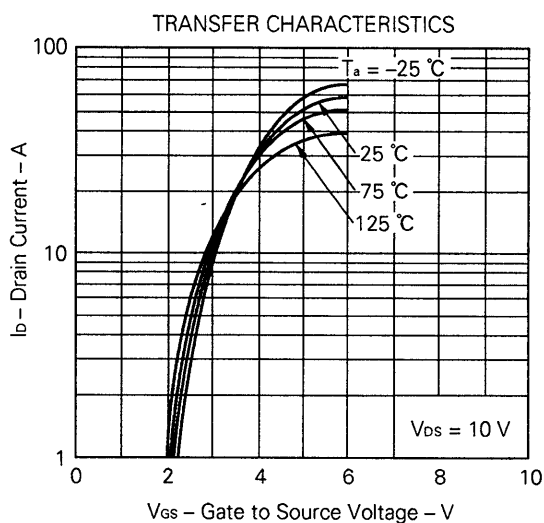
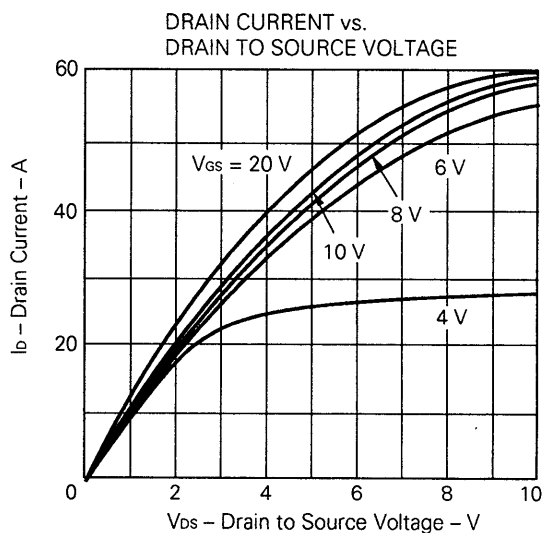
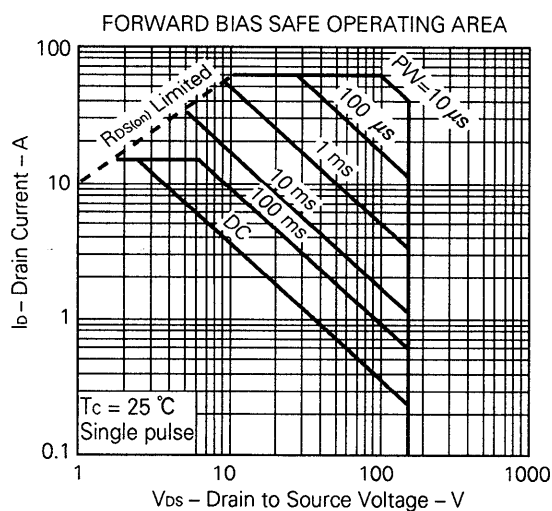
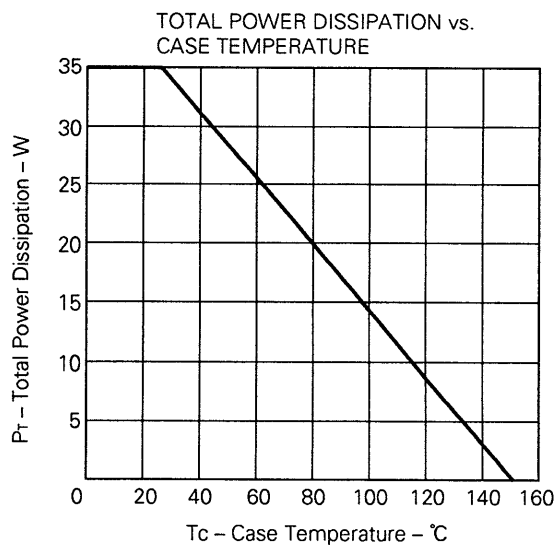
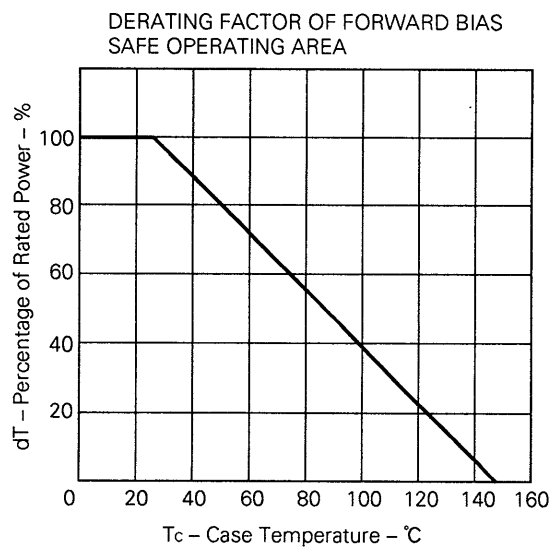
**Test Circuit 1 : Switching Time**



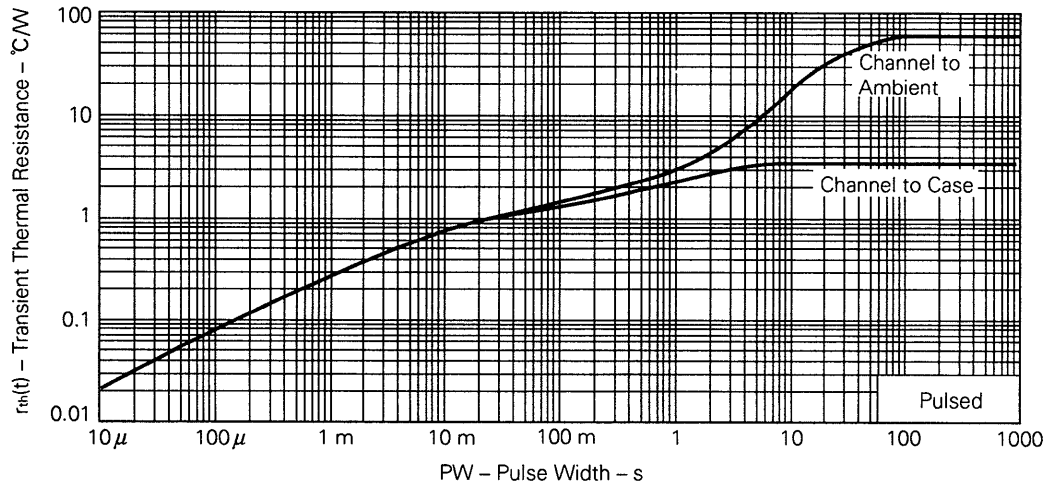
**Test Circuit 2 : Gate Charge**



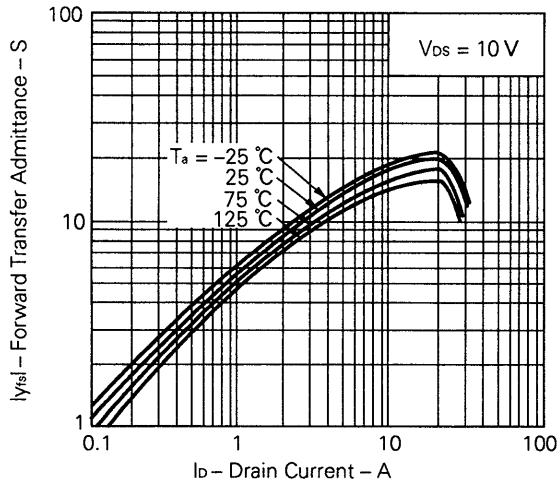
TYPICAL CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ )



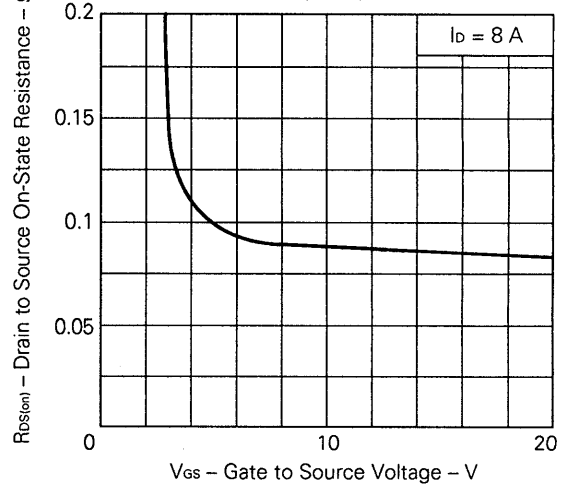
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



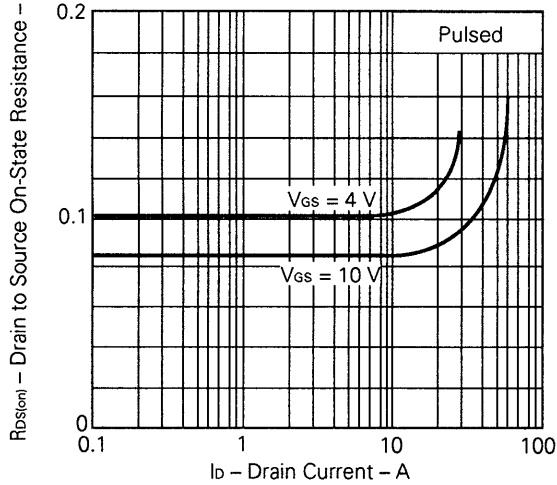
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



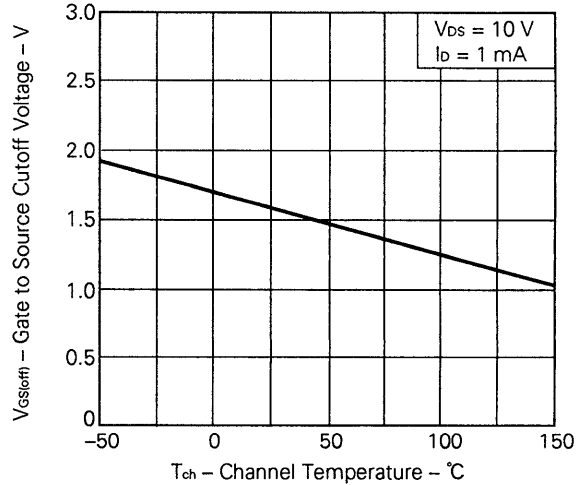
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

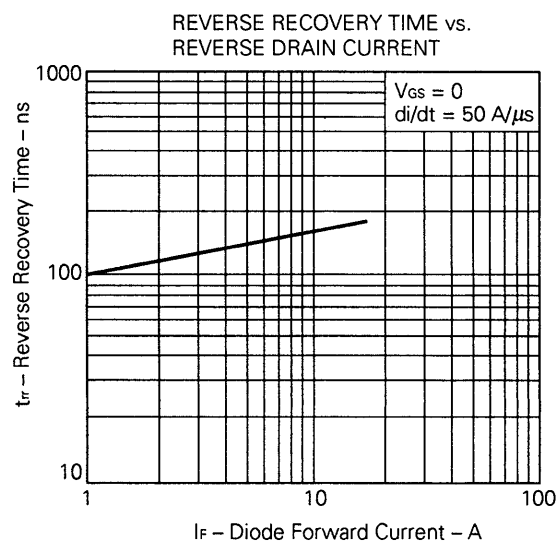
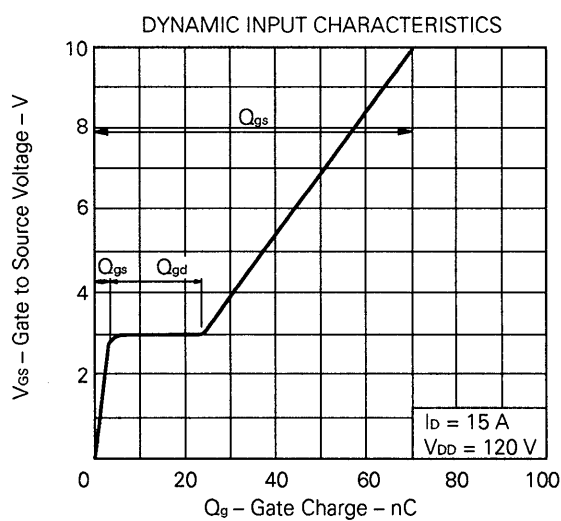
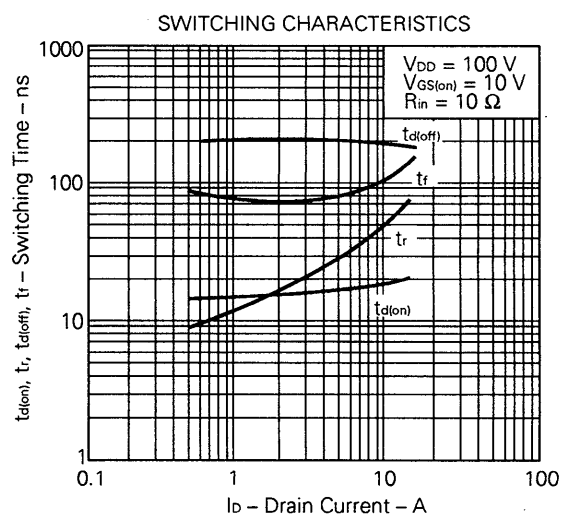
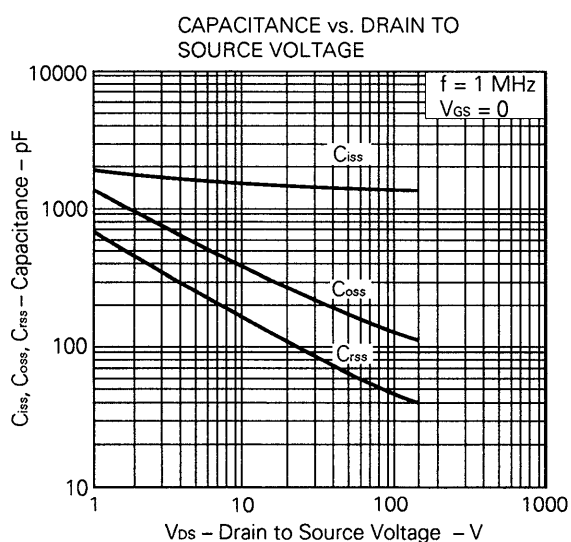
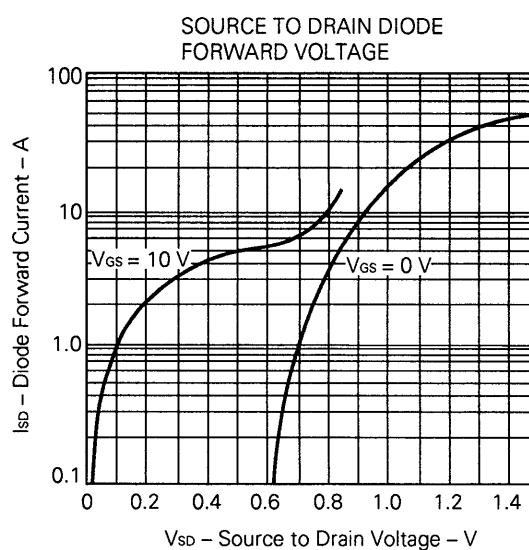
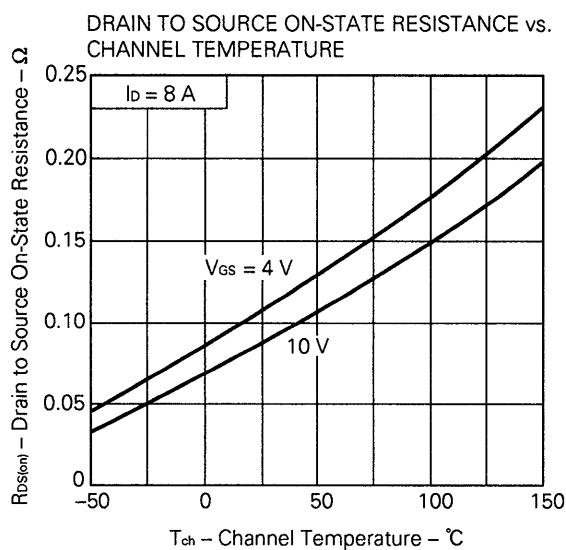


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





# Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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