# 2PG006

### Silicon N-channel enhancement IGBT

For plasma display panel drive For high speed switching circuits

#### Features

- Low collector-emitter saturation voltage:  $V_{CE(sat)} < 2.4 \text{ V}$
- High-speed switching:  $t_f = 175$  ns (typ.)

#### Absolute Maximum Ratings $T_C = 25^{\circ}C$

Parameter	Symbol	Rating	Unit	
Collector-emitter voltage (E-B short)	V <sub>CES</sub>	430	V	
Gate-emitter voltage (E-B short)	V <sub>GES</sub>	-30 to +35	v	
Collector current	I <sub>C</sub>	40	А	
Peak collector current *	I <sub>CP</sub>	230	А	
Power dissipation $T_a = 25^{\circ}C$	P <sub>C</sub>	40	W	
		2.0	W	
Junction temperature	Tj	150	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	

Note) \*: Assurance of repetitive pulse. (Repetitive period  $\leq 5 \ \mu s$  on-duty  $\leq 20\%$ )

But, it must stay within 40% of all that the time impressed pulse repetitively.

$$T \leq 5.0 \ 00\mu s, On-duty \leq 20\%$$

#### Electrical Characteristics $T_C = 25^{\circ}C \pm 3^{\circ}C$

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Collector-emitter voltage (E-B short)	V <sub>CES</sub>	$I_C = 1 \text{ mA}, V_{GE} = 0$	430			V
Collector-emitter cutoff current (E-B short) *	I <sub>CES</sub>	$V_{CE} = 344 V, V_{GE} = 0$			5.0	μΑ
Gate-emitter cutoff current (E-B short)	I <sub>GES</sub>	$V_{GE} = \pm 35 \text{ V}, -30 \text{ V}, V_{CE} = 0$			±1.0	μΑ
Gate-emitter threshold voltage	V <sub>GE(th)</sub>	$V_{CE} = 10 \text{ V}, I_C = 1.0 \text{ mA}$	3.0		5.5	V
Collector-emitter saturation voltage	V <sub>CE(sat)</sub>	$V_{GE} = 15 \text{ V}, I_C = 40 \text{ A}$		1.75	2.4	V
Collector-emitter reverse break down voltage	-V <sub>CE</sub>	$I_{\rm C} = -100 \text{ mA}, V_{\rm GE} = 15 \text{ V}$	18	22.5		V
Short-circuit input capacitance (Common emitter)	Cies	and the second sec		1 200		pF
Short-circuit output capacitance (Common emitter)	C <sub>oes</sub>	$V_{CE} = 25 \text{ V}, V_{GE} = 0, f = 1 \text{ MHz}$		130		pF
Reverse transfer capacitance (Common emitter)	C <sub>res</sub>			20		pF
Gate charge load	Qg			54		nC
Gate-emitter charge	Q <sub>ge</sub>	$V_{CC} = 200 \text{ V}, I_C = 40 \text{ A}, V_{GE} = 15 \text{ V}$		7		nC
Gate-collector charge	Q <sub>gc</sub>			22		nC
Turn-on delay time	t <sub>d(on)</sub>			65		ns
Rise time	t <sub>r</sub>	$V_{\rm CC} = 200 \text{ V}, I_{\rm C} = 40 \text{ A},$		400		ns
Turn-off delay time	t <sub>d(off)</sub>	$RL \approx 5 \Omega, V_{GE} = 15 V$		185		ns
Fall time	t <sub>f</sub>			175	260	ns

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. \*:  $I_{CES}$  is 100% tested according to the  $I_{CES}$  inspection standards. (< 1.0  $\mu$ A under the conditions of  $V_{CE}$  = 344 V,  $V_{GE}$  = 0)

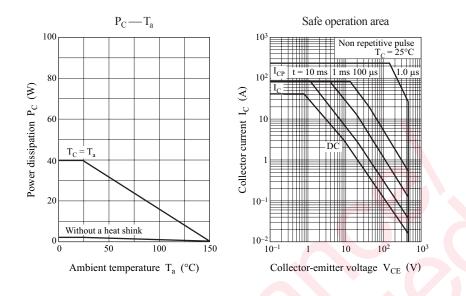
- Package
- Code
- TO-220D-A1
- Marking Symbol: 2PG006
- Pin Name
  - 1. Gate
- 2. Collector
- 3. Emitter

Internal Connection

Ε

#### 2PG006

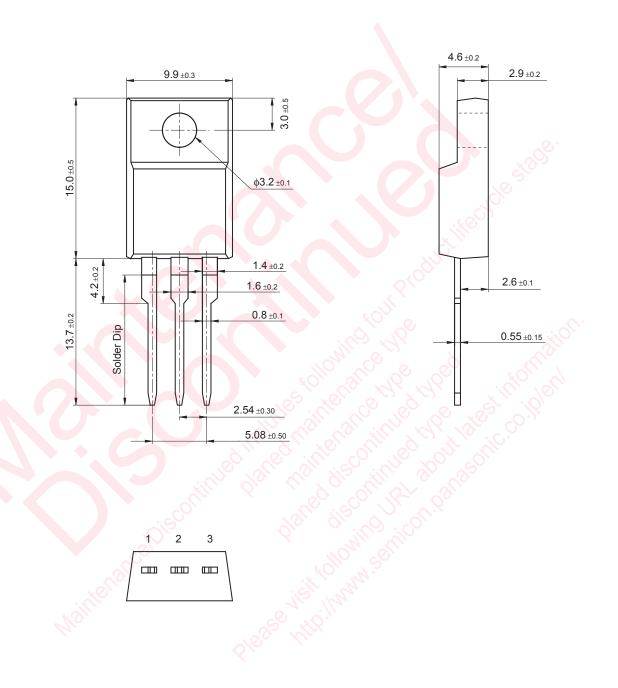
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### **Panasonic**

### TO-220D-A1

Unit: mm



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