3.5A Synchronous buck Converter

❖ GENERAL DESCRIPTION

AX3121 consists of step-down switching regulator with synchronous PWM converter. These devise include a reference voltage source, oscillation circuit, error amplifier, internal PMOS and NMOS etc.

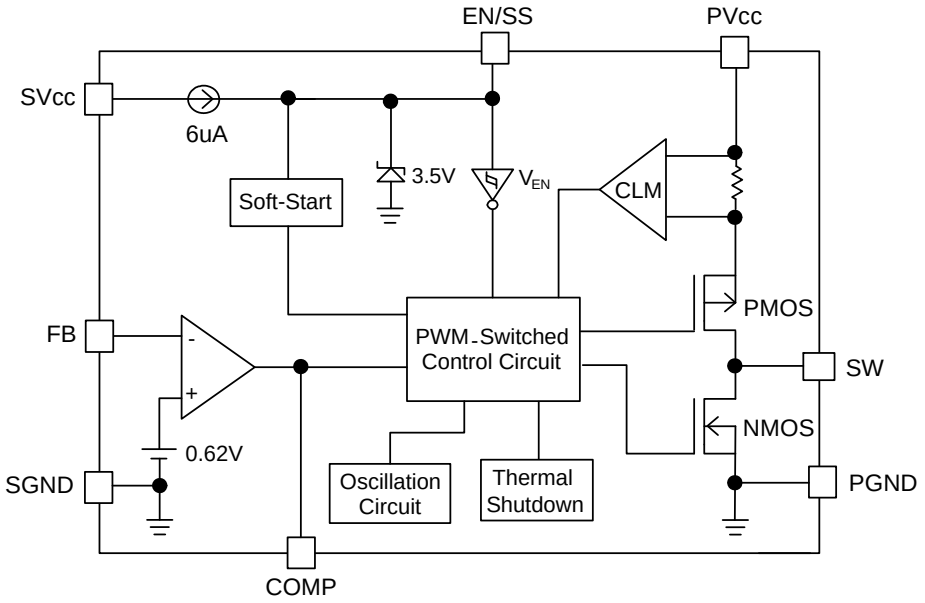
AX3121 provides low-ripple power, high efficiency, and excellent transient characteristics. The PWM control circuit is able to the duty ratio linearly form 0 up to 100%. This converter also contains an error amplifier circuit as well as an enable/soft-start circuit that prevents overshoot at startup. An enable function, an over current protect function and short circuit protect function are built inside, and when OCP or SCP happens, the operation frequency will be reduced. Also, an external compensation is easily to system stable.

With the addition of internal PMOS and NMOS, a coil and capacitors externally, these ICs can function as step-down switching regulators. They serve as ideal power supply units for portable devices when coupled with the SOP-8L-EP package, providing such outstanding features as low current consumption. Since this converter can accommodate an input voltage up to 23V.

❖ FEATURES

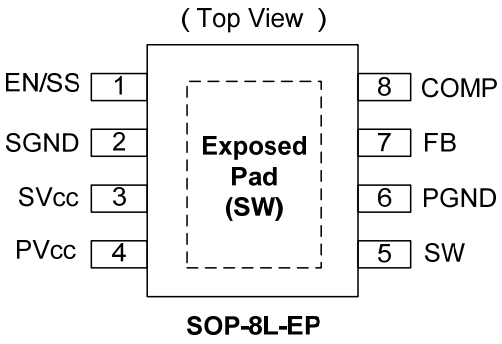
- Input voltage：4.5V to 23V
- Output voltage：V_{FB} to V_{CC}
- Duty ratio：0% to 100% PWM control
- Oscillation frequency：250KHz typ.
- Enable/Soft-Start and Current Limit (CL).
- Thermal Shutdown function.
- Short Circuit Protect (SCP).
- Built-in internal SW P-channel and N-channel MOS.
- SOP-8L with Exposed Pad Pb-Free package.

❖ BLOCK DIAGRAM



❖ PIN ASSIGNMENT

The package of AX3121 is SOP-8L-EP; the pin assignment is given by:



SOP-8L-EP

Name	Description
FB	Feedback pin
EN/SS	ON/OFF Shutdown and Soft-start pin
COMP	Compensation pin
PV_{CC}	Driver power supply pin
SVcc	IC power supply pin
SW	Switch pin. Connect external inductor here.
PGND	Power ground pin
SGND	Signal ground pin

❖ ORDER/MARKING INFORMATION

Order Information	Top Marking
AX3121 XX X Package Type ES: SOP-8L-EP Packing Blank : Tube A : Taping	Logo ← AX 3 1 2 1 → Part number Y Y W W X → ID code:internal WW: 01~52 Year: 10=2010 11=2011

❖ ABSOLUTE MAXIMUM RATINGS (at T_A=25°C)

Characteristics	Symbol	Rating	Unit
SVCC,PVCC Pin Voltage	V_{CC}	V_{SS} - 0.3 to V_{SS} + 24	V
Feedback Pin Voltage	V_{FB}	V_{SS} - 0.3 to V_{CC}	V
EN/SS Pin Voltage	$V_{EN/SS}$	V_{SS} - 0.3 to 5	V
COMP Pin Voltage	V_{COMP}	V_{SS} - 0.3 to 5	V
Switch Pin Voltage	V_{SW}	V_{SS} - 0.3 to V_{CC} + 0.3	V
Power Dissipation	PD	Internally limited	mW
Storage Temperature Range	T_{ST}	-40 to +165	°C
Junction Temperature Range	T_J	-40 to +150	°C
Operating Supply Voltage	V_{OP}	4.5 to 23	V
Thermal Resistance from Junction to case	θ_{JC}	15	°C/W
Thermal Resistance from Junction to ambient	θ_{JA}	40	°C/W

Note: θ_{JA} is measured with the PCB copper area(need connect to Exposed pad) of approximately 1 in^2(Multi-layer).

❖ ELECTRICAL CHARACTERISTICS

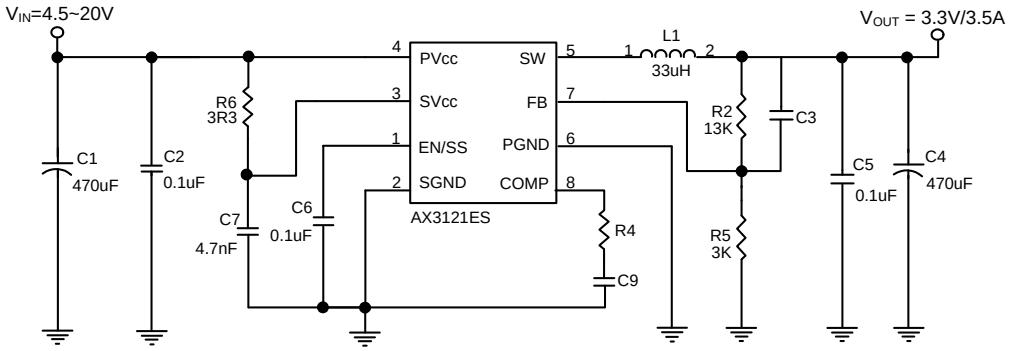
(V_{IN} = 12V, V_{OUT}=3.3V, T_A=25°C, unless otherwise specified)

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	I_{OUT}=0.1A	0.605	0.620	0.635	V
Feedback Bias Current	I_{FB}	I_{OUT}=0.1A	-	0.1	0.5	uA
Quiescent Current	I_{CCQ}	V_{FB}=1.2V force driver off	-	6	8	mA
Shutdown Supply Current	I_{SD}	V_{EN} =0V	-	45	80	uA
Switch Current Limit	I_{SW-Lim}		4.0	-	-	A
Line Regulation	$\triangle V_{OUT}/V_{OUT}$	V_{IN} = 4.5V~23V, I_{OUT}=0.2A	-	0.02	0.1	%
Load Regulation	$\triangle V_{OUT}/V_{OUT}$	I_{OUT} = 0.1A to 3.5A	-	0.3	0.7	%
Oscillation Frequency	F_{OSC}	SW pin	200	250	300	KHz
Short Oscillation Frequency	F_{OSC1}	V_{FB}<0.4V	-	40	-	KHz
Dead Time	T_{DR}	Rising	-	50	-	nS
	T_{DF}	Falling	-	50	-	
EN/SS shutdown threshold voltage	V_{ENL}	regulator OFF	-	-	0.4	V
EN/SS current	$I_{EN/SS}$	$V_{EN/SS}$=0V	-	6	12	uA
Internal PMOS R_{DSON}	$R_{DS(ON)-P}$	V_{IN}=5V, V_{FB}=0V	-	90	150	mΩ
		V_{IN}=12V, V_{FB}=0V	-	50	120	
Internal NMOS R_{DSON} (Note1)	$R_{DS(ON)-N}$		-	75	140	mΩ
			-	45	120	
Thermal Shutdown	T_{SD}		-	150	-	°C
Thermal Shutdown Hysteresis	T_{SH}		-	30	-	°C

Note1: Guaranteed by design.

❖ APPLICATION CIRCUIT

1. Using Aluminum Electrolytic Capacitor (AL)

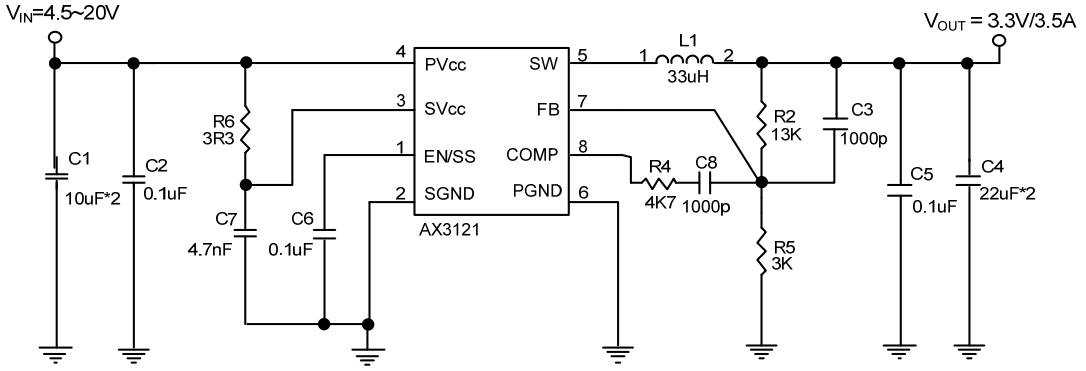


$$V_{OUT} = V_{FB} \times (1 + \frac{R2}{R5})$$

V_{FB} = 0.62V ; R5 suggest 3K ~ 6.8k

C_{OUT} ESR Range	V_{IN}	V_{OUT}	R4(Ω)	C9	C3
30m~80mΩ	4.5V~20V	1.2~5V	1.2K	10n	1000p
80m~300mΩ	4.5V~20V	1.2~1.8V	240	10n	22p
	4.5V~20V	2.0~5V	240	10n	180p~270p

2. Using Multilayer Ceramic Capacitor (MLCC)



$$V_{OUT} = V_{FB} \times (1 + \frac{R2}{R5})$$

V_{FB} = 0.62V ; R5 suggest 3K ~ 6.8k

V_{IN}	V_{OUT}	R4	C8	C3
4.5V~20V	2.0V~5V	4K7	1000p	1000p

❖ FUNCTION DESCRIPTIONS

PWM Control

The AX3121 consists of DC/DC converters that employ a synchronous pulse-width modulation (PWM) system. In converters of the AX3121, the pulse width varies in a range from 0 to 100%, according to the load current. The ripple voltage produced by the switching can easily be removed through a filter because the switching frequency remains constant. Therefore, these converters provide a low-ripple power over broad ranges of input voltage and load current.

Setting the Output Voltage

Application circuit item shows the basic application circuit with adjustable output version. The external resistor sets the output voltage according to the following equation:

$$V_{OUT} = 0.62V \times \left(1 + \frac{R2}{R5}\right)$$

Table 1 Resistor select for output voltage setting

V_{OUT}	R5	R2
5.0V	4.7K	33K
3.3V	3K	13K
2.5V	3.3K	10K
1.8V	6.8K	13K
1.5V	3.3K	4.7K
1.184V	3.3K	3.0K
1.0V	3.3K	2.0K

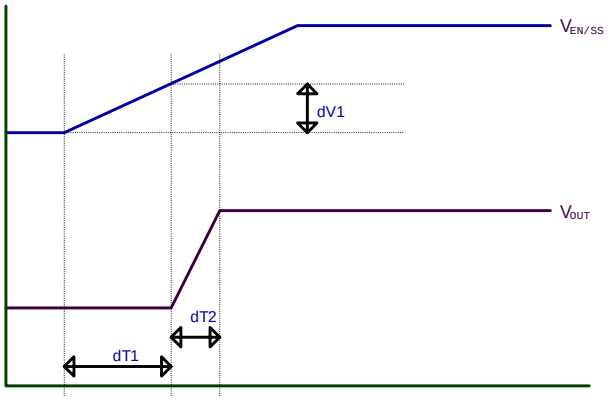
COMP

Compensation pin. For EL output capacitor application, the COMP pin connects R4 and C9 to GND for all condition and for MLCC output capacitor application, the COMP connects R4 and C8 to FB, please refer the application circuit table.

EN/SS

This pin can be supplied shutdown or soft start function. It is inside pull high function. For normal application, the pin must be connected a capacitor to ground. There is a 6uA current to charge this capacitor, vary the different capacitor value to control soft start time. Allow the switching regulator circuit to be shutdown pulling this pin below a 0.4V threshold voltage; the shutdown supply current is approximately 45uA.

The soft-start time can be calculated by below formula, please refer the formula to design.



Calculate Start-up Delay Time (dT1)

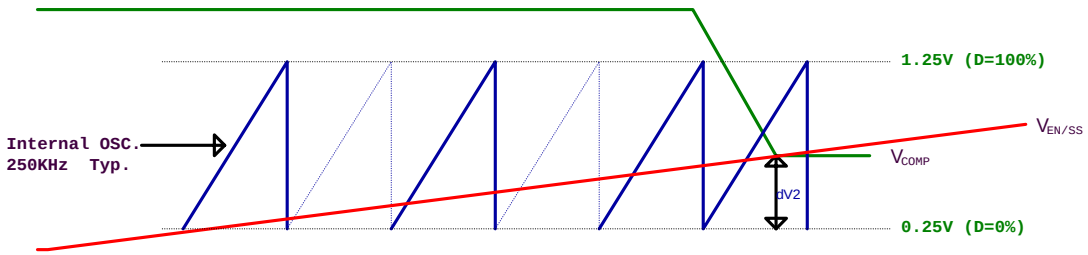
➔ $dT1 = C6 \times dV1 \div I_{EN/SS1}$

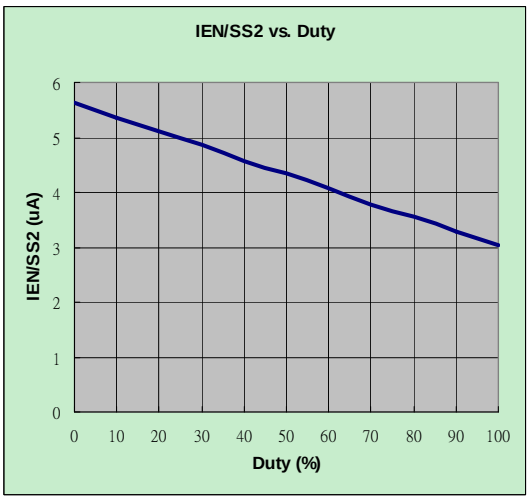
Where:

$I_{EN/SS1}$=6uA

C6=10nF~1000nF

dV1=0.76V (EN/SS V_{IH})





Calculate Soft Start Time (dT2)

$dT2 = C6 \times dV2 \div I_{EN/SS2}$

Where:

$dV2 = (1.25-0.25) \times Duty = V_{OUT}/V_{IN}$ (V)

$I_{EN/SS2} = 5.64-(5.64-3.03) \times dV2 \div (1.25-0.25)$

$= 5.64-2.61 \times V_{OUT}/V_{IN}$ (uA)

※ Duty (%) = $V_{OUT}/V_{IN} \times 100$

Example：

@ C6=100nF, VIN=12V, VOUT=2.5V, IOUT=1A, EN-ON

$dT1 = C6 \times dV1 \div I_{EN/SS1} = 100n \times 0.76 \div 6u = 12.67mS$

$dT2 = C6 \times dV2 \div I_{EN/SS2} = 100n \times 0.208 \div 5.1u = 4.08mS$

Inductor Selection

For most designs, the inductor is suggested 22μH to 33μH. Please refer the below table to design.

L1 recommend value (V_{IN}=12V ,I_{OUT}=3.5A)					
V_{OUT}	1.2V	1.8V	2.5V	3.3V	5V
L1 Value	22uH	22H	22uH	33uH	33uH

Where is inductor Ripple Current. Large value inductors lower ripple current and small value inductors result in high ripple currents. Choose inductor ripple current approximately 15% of the maximum load current 3.5A, ΔI_L=0.52A. The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation (3.5A+0.26A).

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency shall be less than input source impedance to prevent high frequency switching current passing to the input. A low ESR input capacitor sized for maximum RMS current must be used.

The capacitor voltage rating should be at least 1.5 times greater than the input voltage, and often much higher voltage ratings are needed to satisfy.

Output Capacitor Selection

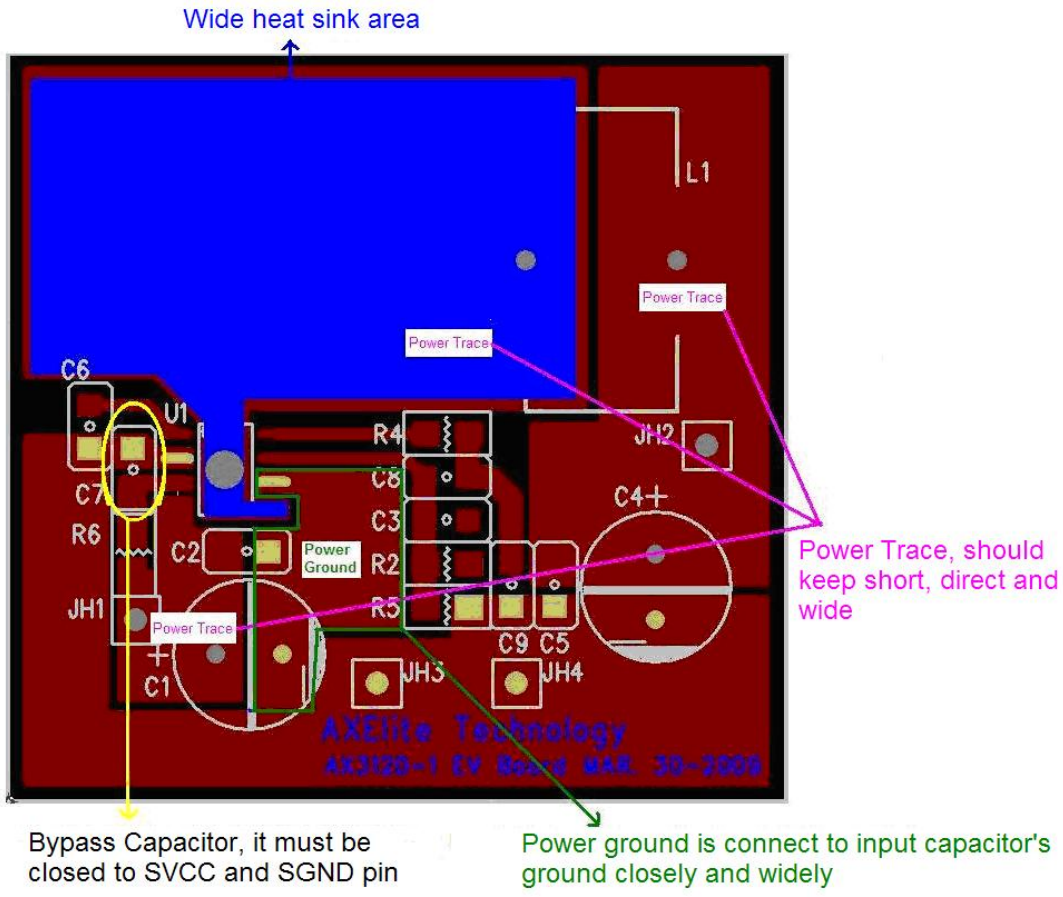
The output capacitor is required to keep the output voltage ripple small and to ensure regulation loop stability. The output capacitor must have low impedance at the switching frequency. A low ESR capacitor sized for maximum RMS current must be used. The low ESR requirements needed for low output ripple voltage.

The capacitor voltage rating should be at least 1.5 times greater than the input voltage, and often much higher voltage ratings are needed to satisfy.

Layout Guidance (please refer layout picture)

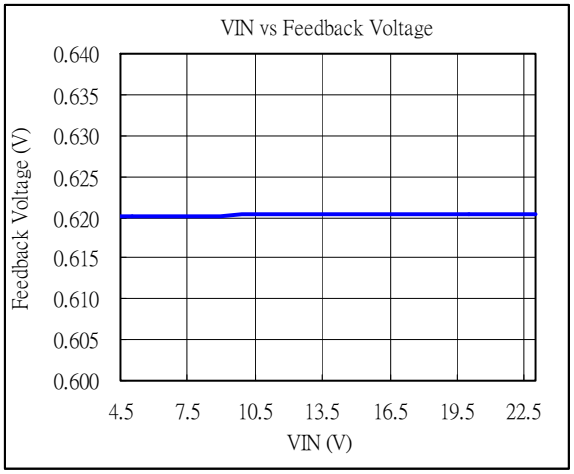
When laying out the PC board, the following suggestions should be taken to ensure proper operation of the AX3121. These items are also illustrated graphically in below.

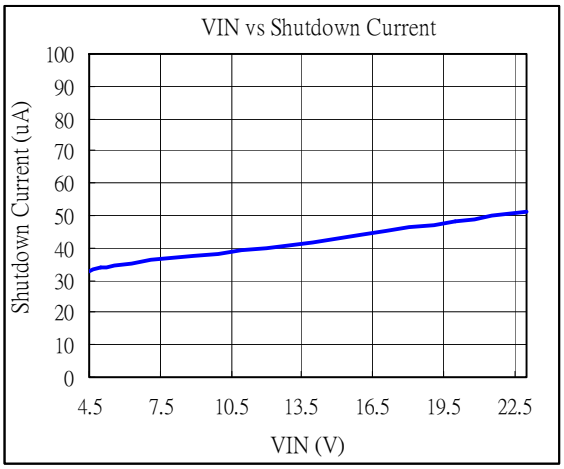
1. The power traces, including the source trace, the output trace and the inductor trace should be kept short, direct and wide to allow large current flow.
2. The power ground is keep input capacitor's (C4) ground closed and far away signal ground.
3. The C7 bypass capacitor must be closed to SVCC and SGND pin.
4. The exposed pad is connecting to SW trace closely and widely. (Reduce IC temperature)
5. Do not trace signal line under inductor.

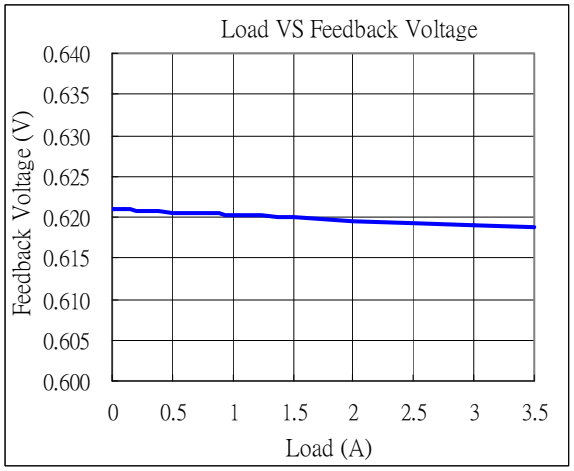


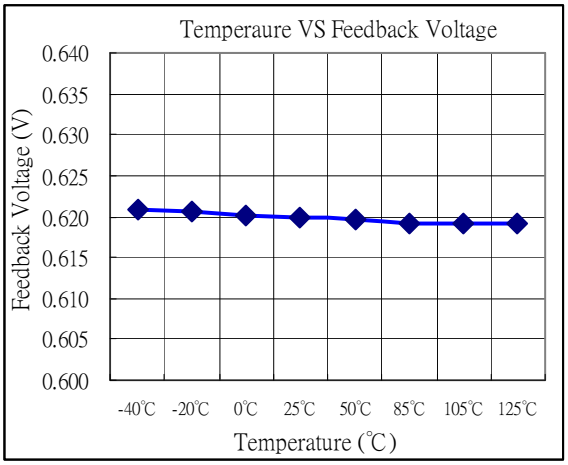
(AX3121 SOP-8L-EP PCB Layout -Top View)

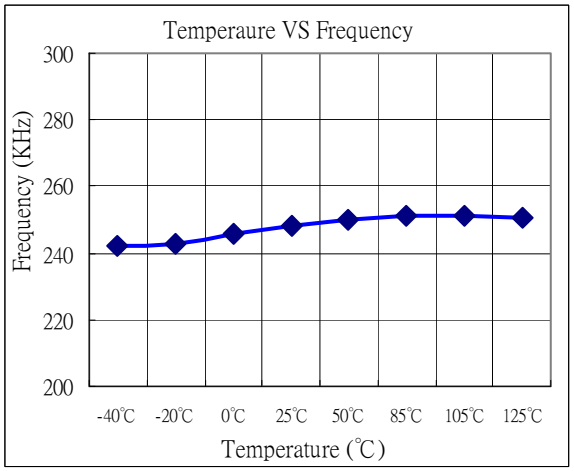
❖ TYPICAL CHARACTERISTICS

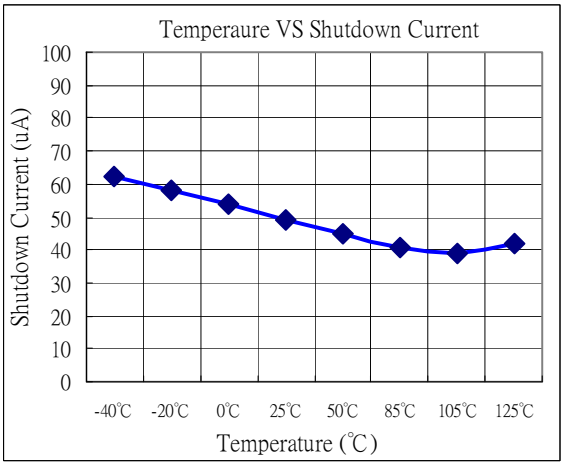




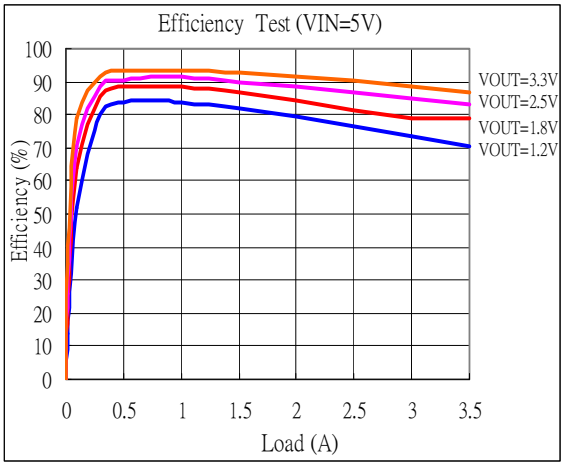


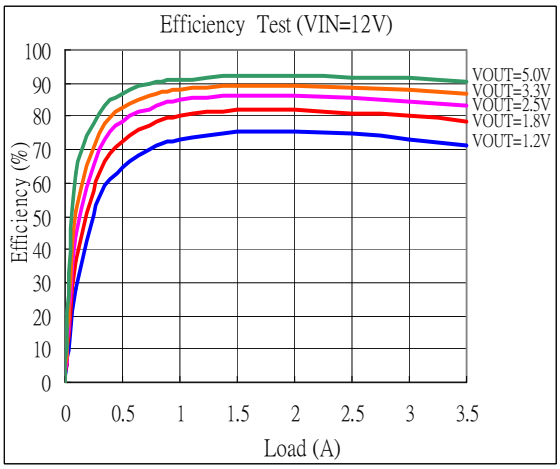




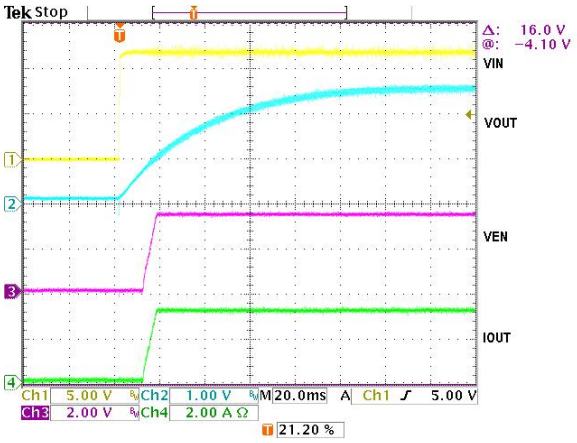


❖ TYPICAL CHARACTERISTICS (CONTINUES)

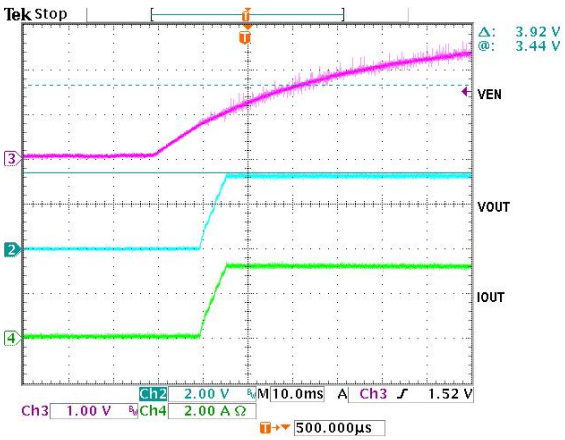




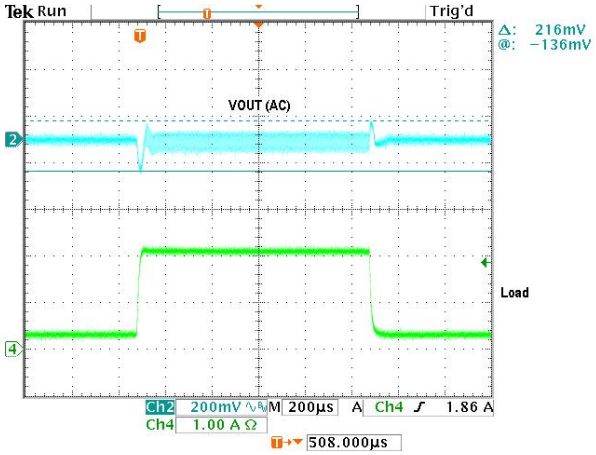
Power-ON Wave
(V_{IN}=12V, V_{OUT}=2.5V, Load=3.5A, C6=0.1uF)



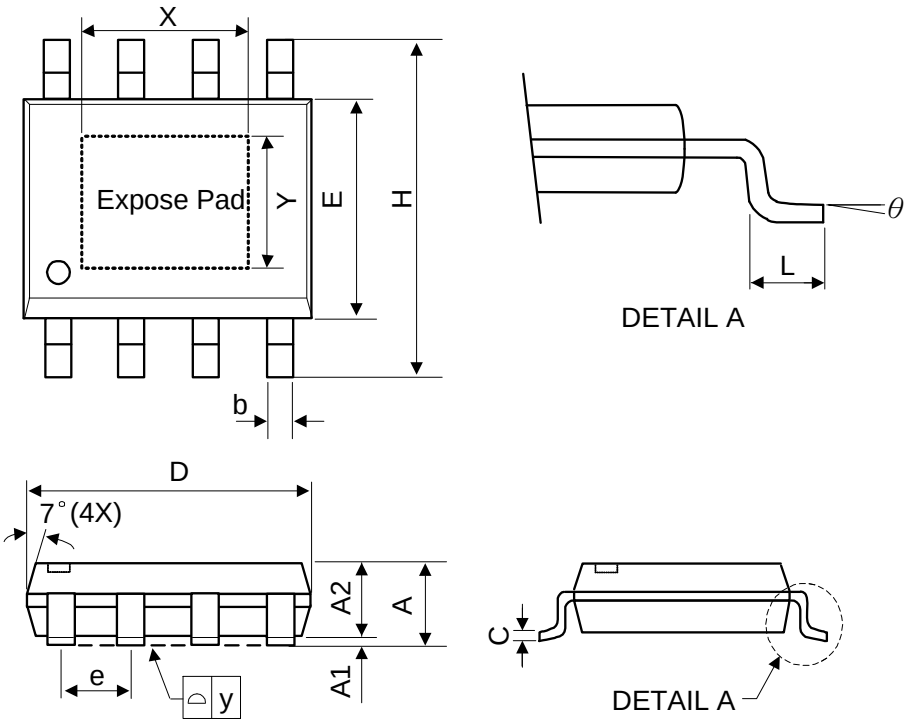
Enable-ON Wave
(V_{IN}=12V, V_{OUT}=2.5V, Load=3.5A, C6=0.1uF)



Load Transient
(V_{IN}=12V, V_{OUT}=2.5V, Load=0.2~2A)



❖ PACKAGE OUTLINES



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.75	-	-	0.069
A1	0	-	0.15	0	-	0.06
A2	1.25	-	-	0.049	-	-
C	0.1	0.2	0.25	0.0075	0.008	0.01
D	4.7	4.9	5.1	0.185	0.193	0.2
E	3.7	3.9	4.1	0.146	0.154	0.161
H	5.8	6	6.2	0.228	0.236	0.244
L	0.4	-	1.27	0.015	-	0.05
b	0.31	0.41	0.51	0.012	0.016	0.02
e	1.27 BSC			0.050 BSC		
y	-	-	0.1	-	-	0.004
X	-	2.34	-	-	0.092	-
Y	-	2.34	-	-	0.092	-
θ	0°	-	8°	0°	-	8°

Mold flash shall not exceed 0.25mm per side
JEDEC outline: MS-012 BA