



# STF7N95K3 STP7N95K3, STW7N95K3

N-channel 950 V, 1.1  $\Omega$ , 7.2 A, TO-220, TO-220FP, TO-247  
Zener-protected SuperMESH3™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>	P <sub>w</sub>
STF7N95K3	950 V	< 1.35 $\Omega$	7.2 A	35 W
STP7N95K3	950 V	< 1.35 $\Omega$	7.2 A	150 W
STW7N95K3	950 V	< 1.35 $\Omega$	7.2 A	150 W

- 100% avalanche tested
- Extremely large avalanche performance
- Gate charge minimized
- Very low intrinsic capacitances
- Zener-protected

## Application

- Switching applications

## Description

The new SuperMESH3™ series is obtained through the combination of a further fine tuning of ST's well established strip-based PowerMESH™ layout with a new optimized vertical structure. In addition to pushing on-resistance significantly down, special attention has been taken to ensure a very good dynamic performances coupled with a very large avalanche capability for the most demanding application.

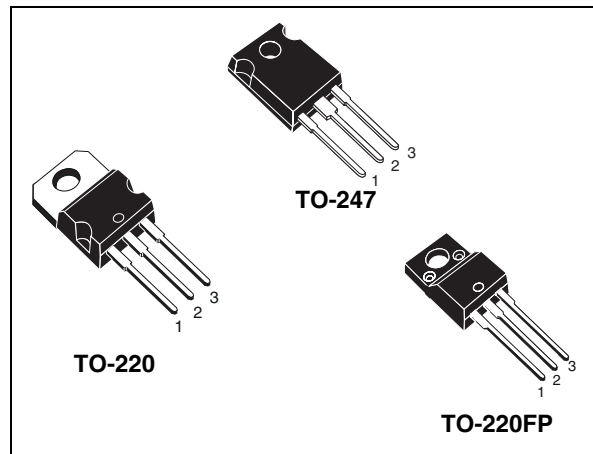


Figure 1. Internal schematic diagram

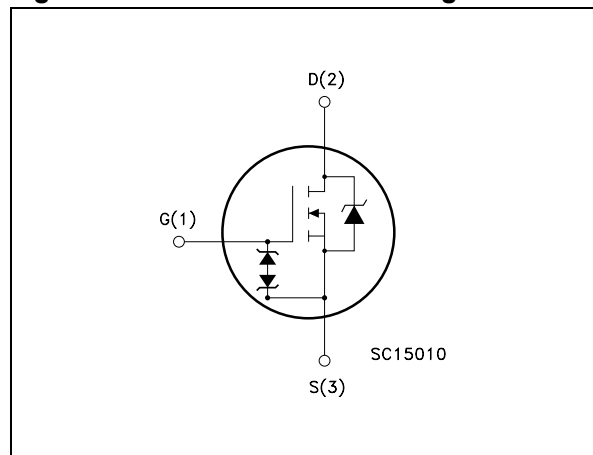


Table 1. Device summary

Order codes	Marking	Package	Packaging
STF7N95K3	7N95K3	TO-220FP	Tube
STP7N95K3	7N95K3	TO-220	Tube
STW7N95K3	7N95K3	TO-247	Tube

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits</b> .....	<b>9</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>10</b>
<b>5</b>	<b>Revision history</b> .....	<b>14</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220, TO-247	TO-220FP	
$V_{GS}$	Gate-source voltage	± 30		V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	7.2	7.2 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ °C}$	4.5	4.5 <sup>(1)</sup>	A
$I_{DM}$ <sup>(2)</sup>	Drain current (pulsed)	28.8	28.8 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ °C}$	150	35	W
$I_{AR}$	Max current during repetitive or single pulse avalanche (pulse width limited by $T_{JMAX}$ )	9		A
$E_{AS}$	Single pulse avalanche energy <sup>(3)</sup>	220		mJ
	Derating factor	1.12	0.24	W/°C
$dv/dt$ <sup>(4)</sup>	Peak diode recovery voltage slope	6		V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t=1\text{ s}; T_C=25\text{ °C}$ )		2000	V
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150		°C

- Limited by package
- Pulse width limited by safe operating area
- Starting  $T_j = 25\text{ °C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$
- $I_{SD} \leq 7.2\text{ A}$ ,  $di/dt = 100\text{ A}/\mu\text{s}$ ,  $V_{Peak} < V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	TO-220	TO-247	TO-220FP	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.83		3.57	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	50	62.5	°C/W
$T_l$	Maximum lead temperature for soldering purpose	300			°C

## 2 Electrical characteristics

(T<sub>case</sub> = 25 °C unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	950			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating V <sub>DS</sub> = Max rating, T <sub>C</sub> =125 °C			1 50	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			10	μA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100 μA	3	4	5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.6 A		1.1	1.35	Ω

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> <sup>(1)</sup>	Forward transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3.6 A		5		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	V <sub>DS</sub> = 100 V, f = 1 MHz, V <sub>GS</sub> = 0		1031 79 0.9		pF pF pF
C <sub>o(tr)</sub> <sup>(2)</sup>	Equivalent capacitance time related	V <sub>DS</sub> = 0 to 760 V, V <sub>GS</sub> = 0		60		pF
C <sub>o(er)</sub> <sup>(3)</sup>	Equivalent capacitance energy related	V <sub>DS</sub> = 0 to 760 V, V <sub>GS</sub> = 0		36		pF
R <sub>G</sub>	Gate input resistance	f=1 MHz Gate DC Bias=0 Test signal level = 20 mV open drain		2.4		Ω
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	V <sub>DD</sub> = 760 V, I <sub>D</sub> = 7.2 A, V <sub>GS</sub> = 10 V (see <a href="#">Figure 20</a> )		34 6 20		nC nC nC

1. Pulsed: pulse duration = 300 μs, duty cycle 1.5%
2. C<sub>oss eq</sub> time related is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>
3. C<sub>oss eq</sub> energy related is defined as a constant equivalent capacitance giving the same stored energy as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475\text{ V}$ , $I_D = 3.6\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 19</a> )		14		ns
$t_r$	Rise time			9		ns
$t_{d(off)}$	Turn-off-delay time			36		ns
$t_f$	Fall time			23		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				7.2	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				28.8	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 7.2\text{ A}$ , $V_{GS} = 0$			1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 7.2\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 24</a> )		450		ns
$Q_{rr}$	Reverse recovery charge			6		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			28		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 7.2\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 24</a> )		550		ns
$Q_{rr}$	Reverse recovery charge			8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			28		A

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{gs} = \pm 1\text{ mA}$ (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

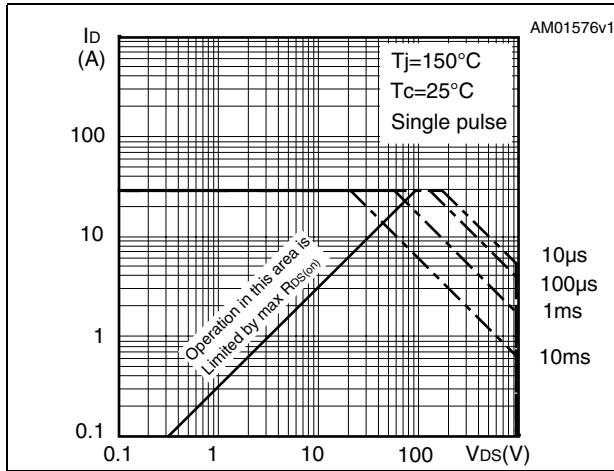


Figure 3. Thermal impedance for TO-220

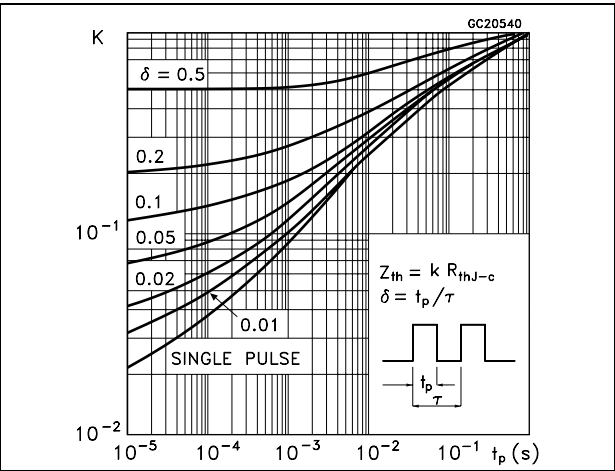


Figure 4. Safe operating area for TO-220FP

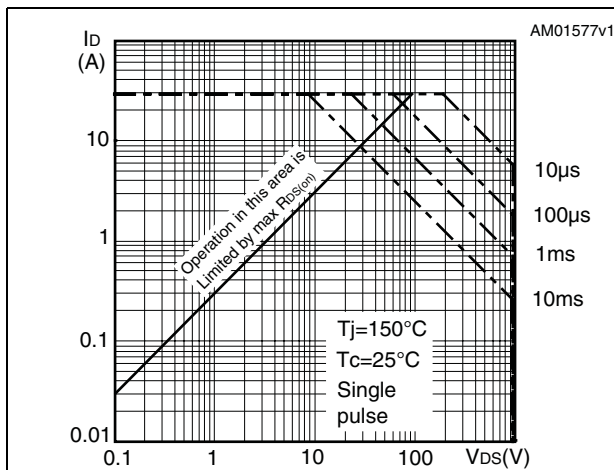


Figure 5. Thermal impedance for TO-220FP

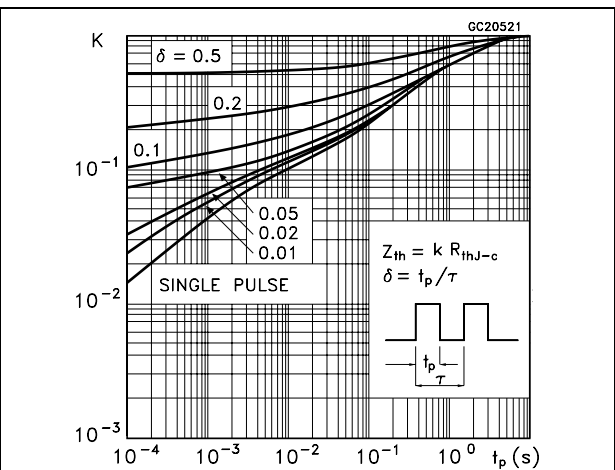


Figure 6. Safe operating area for TO-247

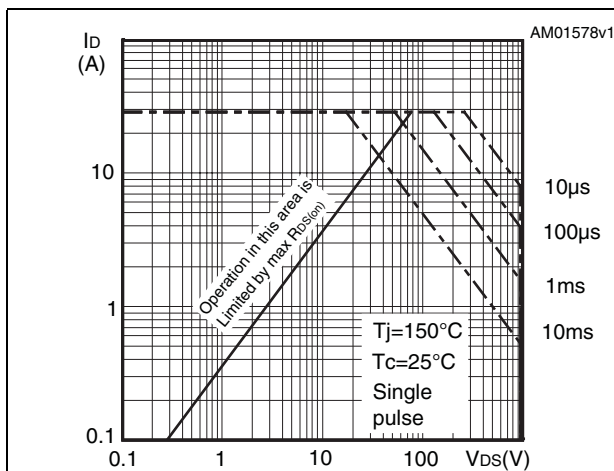


Figure 7. Thermal impedance for TO-247

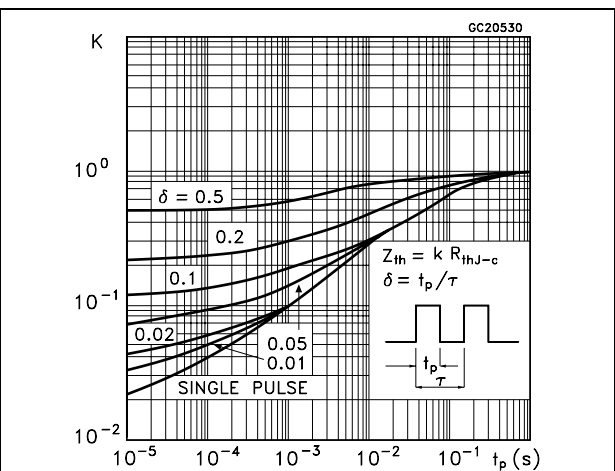


Figure 8. Output characteristics

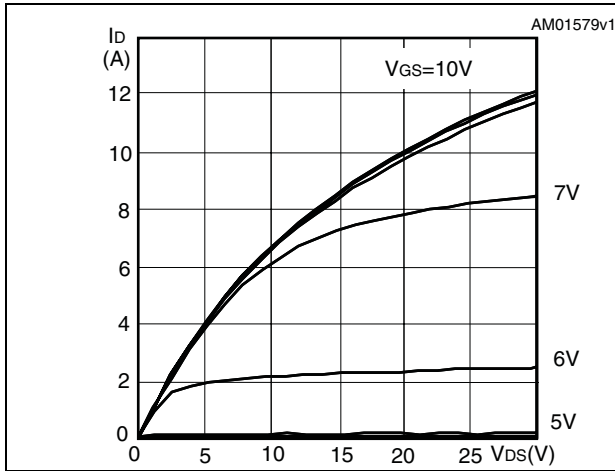


Figure 9. Transfer characteristics

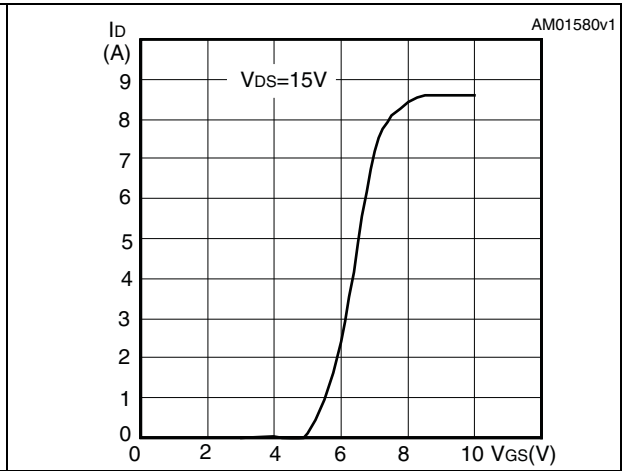


Figure 10. Normalized  $B_{VDSS}$  vs temperature

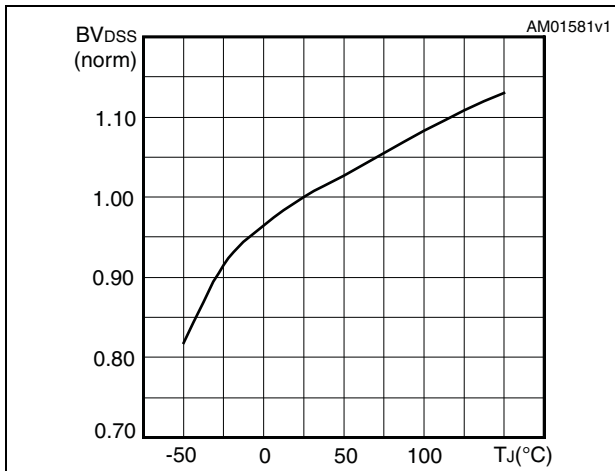


Figure 11. Static drain-source on resistance

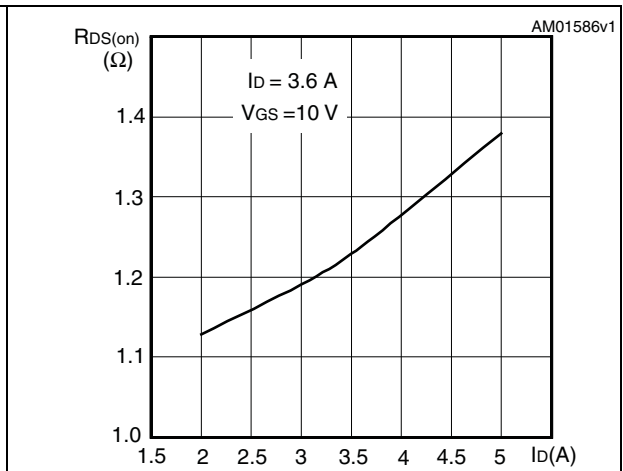


Figure 12. Gate charge vs gate-source voltage

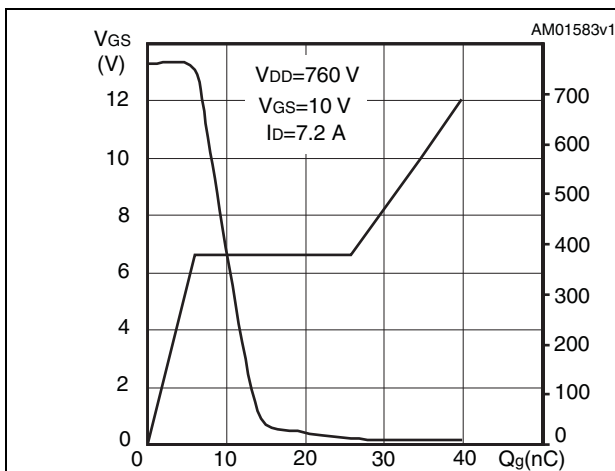


Figure 13. Capacitance variations

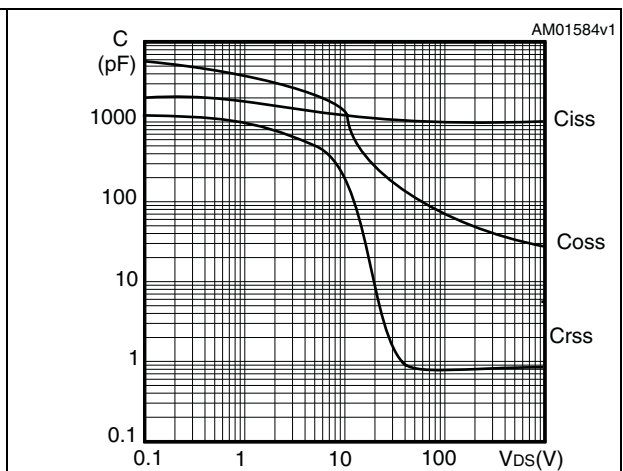


Figure 14. Output capacitance stored energy

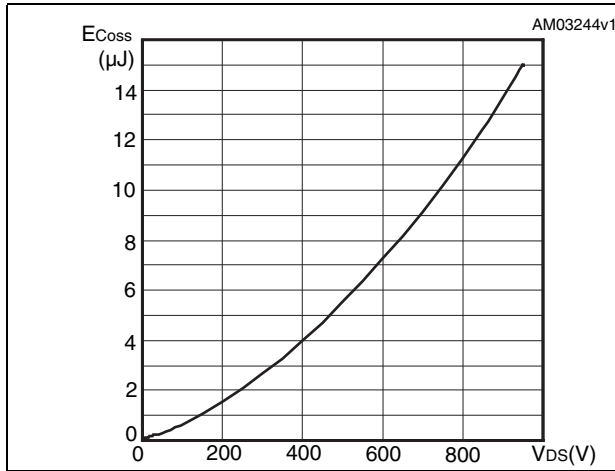


Figure 15. Normalized on resistance vs temperature

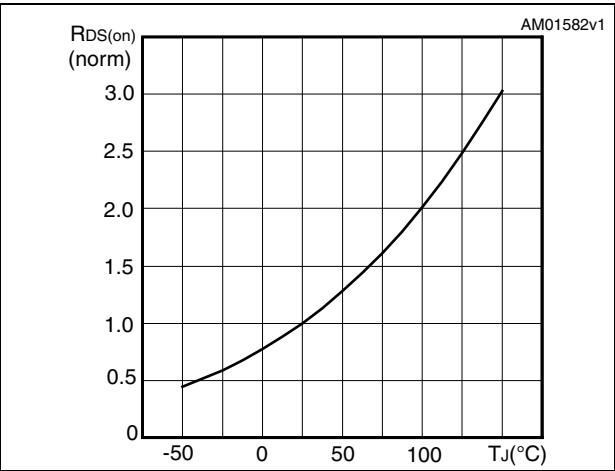


Figure 16. Source-drain diode forward characteristics

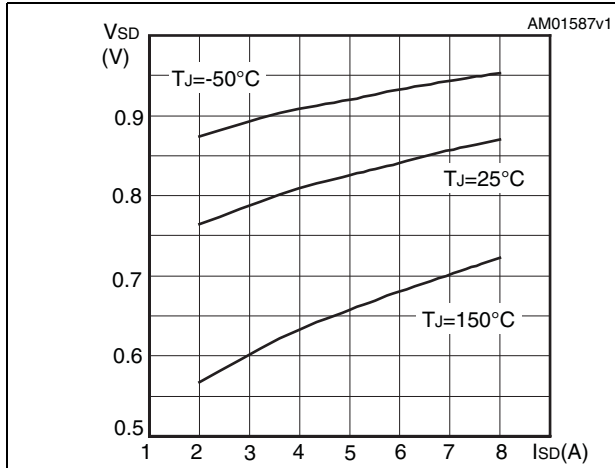


Figure 17. Normalized gate threshold voltage vs temperature

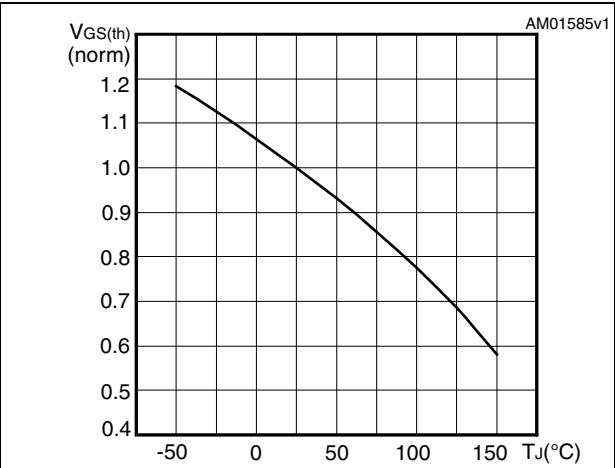
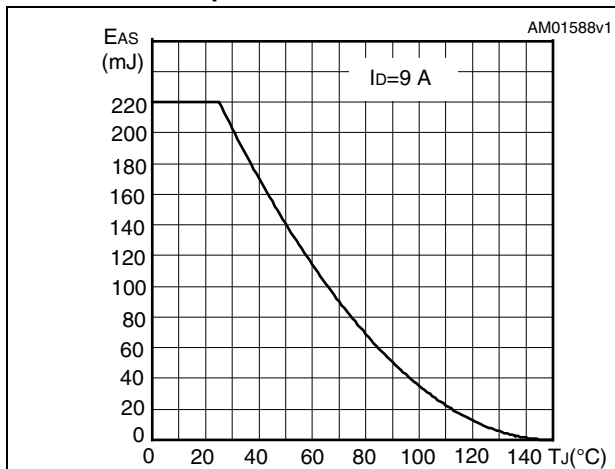


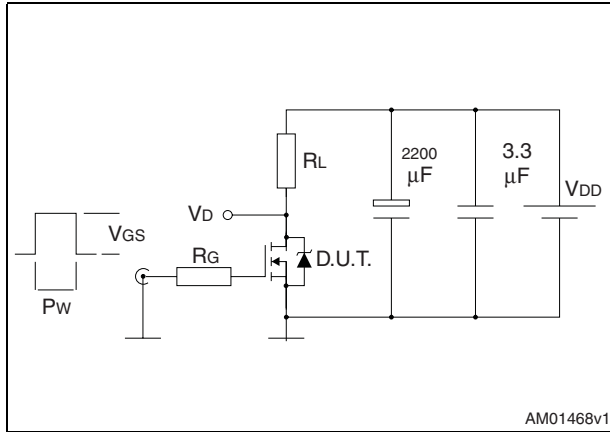
Figure 18. Maximum avalanche energy vs temperature





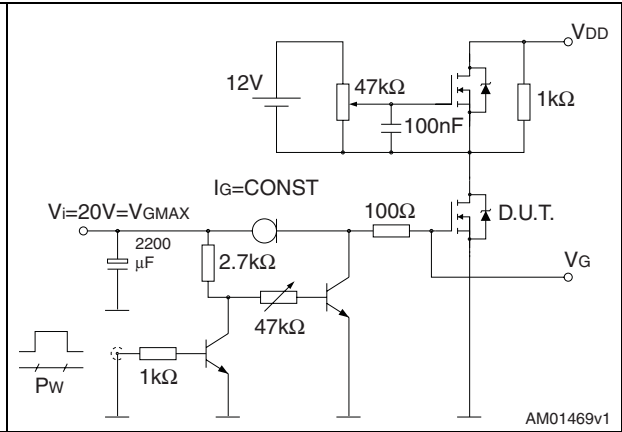
### 3 Test circuits

**Figure 19. Switching times test circuit for resistive load**



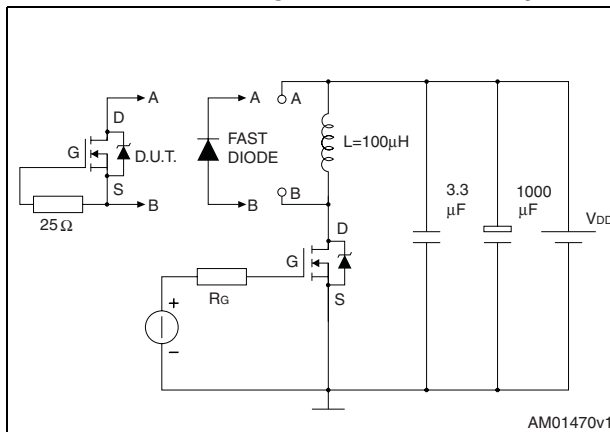
AM01468v1

**Figure 20. Gate charge test circuit**



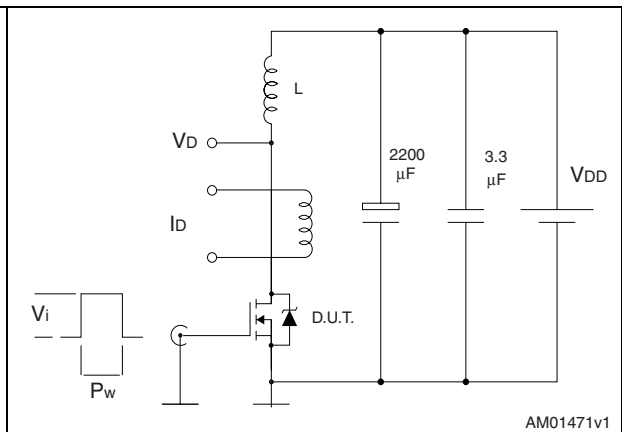
AM01469v1

**Figure 21. Test circuit for inductive load switching and diode recovery times**



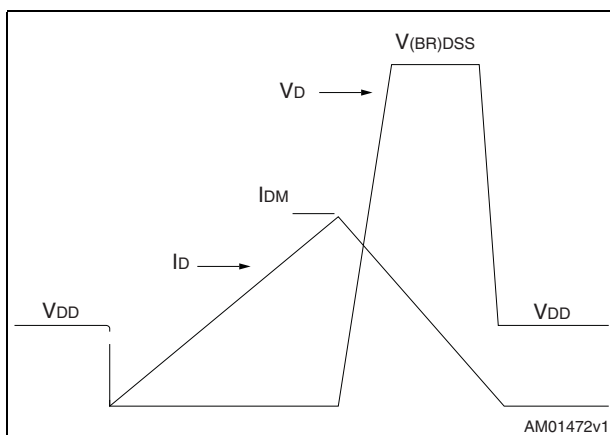
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**Figure 22. Unclamped inductive load test circuit**



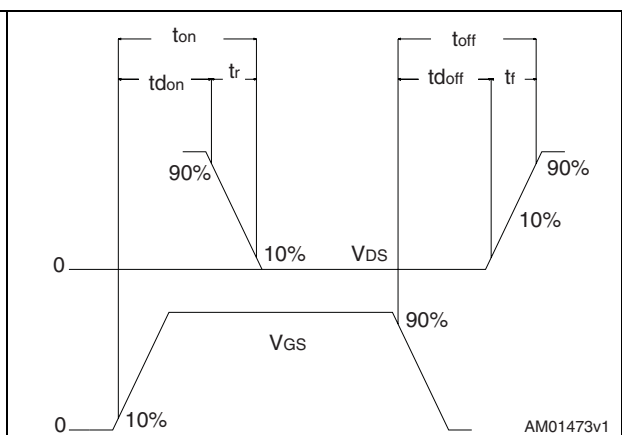
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**Figure 23. Unclamped inductive waveform**



AM01472v1

**Figure 24. Switching time waveform**



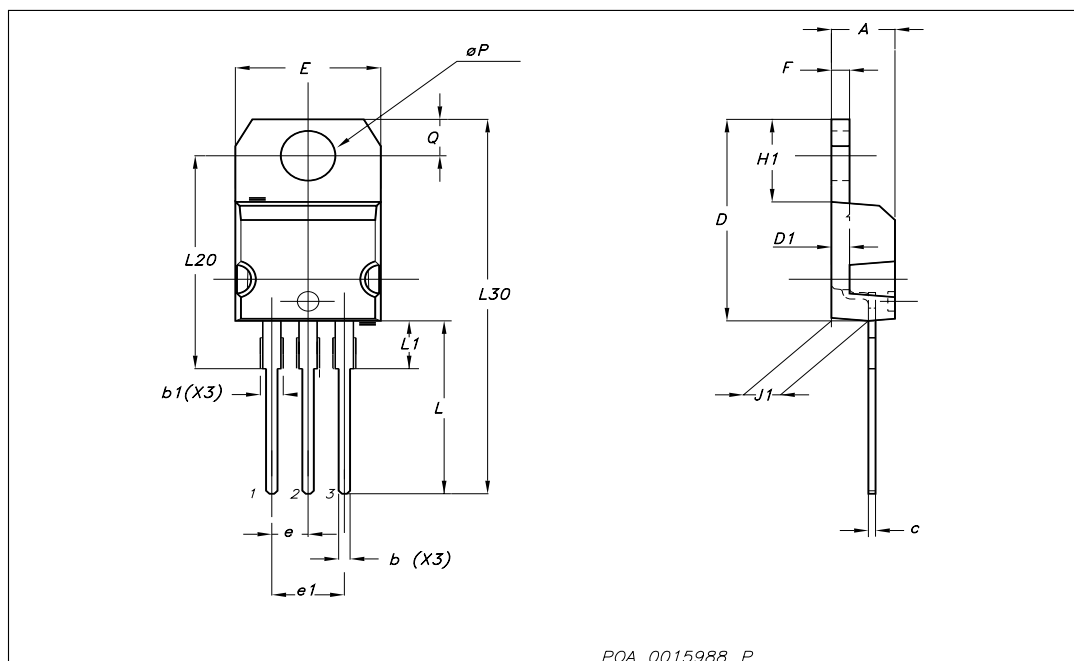
AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

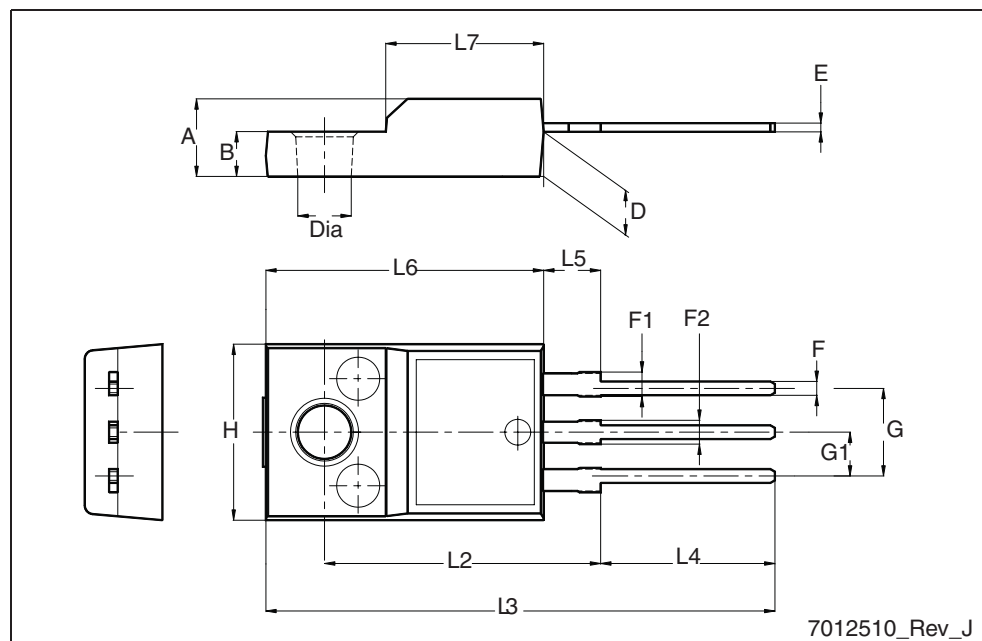
## TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



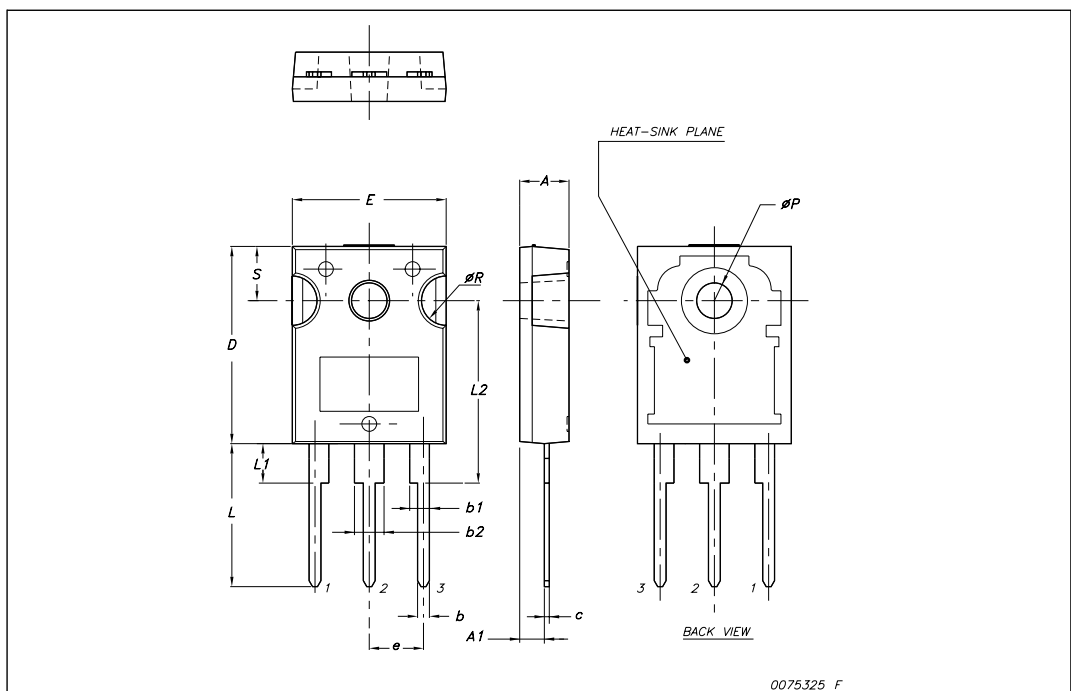
TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.5
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2



## TO-247 Mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
27-Jan-2009	1	First release

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