## RGB Encoder

## Description

The CXA2075M is an encoder IC that converts analog RGB signals to a composite video signal. This IC has various pulse generators necessary for encoding. Composite video outputs and Y/C outputs for the $S$ terminal are obtained just by inputting composite sync, subcarrier and analog RGB signals.
It is best suited to image processing of personal computers and video games.

Compared to the CXA1645M, the CXA2075M has superior points as follows:

1. The number of parts reduced (5 parts)

Clamp capacitor
Regulator capacitor resistor
Resistor for filter
2. External parts reduced by the internal TRAP
(External TRAP can be also selected)
3. Higher band of R, G, B OUT

## Features

- Single 5V power supply
- Compatible with both NTSC and PAL systems
- Built-in $75 \Omega$ drivers
(RGB output, composite video output, Y output, C output)
- Both sine wave and pulse can be input as a subcarrier.
- Built-in band-pass filter for the C signal and delay line for the $Y$ signal
- Built-in $R-Y$ and $B-Y$ modulator circuits
- Built-in PAL alternate circuit
- Burst flag generator circuit
- Half H killer circuit



## Applications

Video games and personal computers

## Structure

Bipolar silicon monolithic IC

## Absolute Maximum Ratings

- Supply voltage Vcc
- Operating temperature Topr $\quad-20$ to $+75 \quad{ }^{\circ} \mathrm{C}$
- Storage temperature Tstg -65 to $+150 \quad{ }^{\circ} \mathrm{C}$
- Allowable power dissipation
$\begin{array}{ll}\text { PD } & 780\end{array}$
- Input pin applied voltage RIN, GIN, BIN, SCIN, NPIN, SYNCIN and Vcc pins voltage or below, GND pin voltage or above


## Recommended Operating Condition

Supply voltage Vcc1, $2 \quad 5.0 \pm 0.25$
V

## Block Diagram and Pin Configuration



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Pin Description

| Pin No. | Symbol | Pin voltage | Equivalent circuit | Description |
| :---: | :---: | :---: | :---: | :---: |
| 1 | GND1 | OV | - | Ground for all circuits other than RGB, composite video and $\mathrm{Y} / \mathrm{C}$ output circuits. The leads to GND2 should be as short and wide as possible. |
| $\begin{aligned} & 2 \\ & 3 \\ & 4 \end{aligned}$ | $\begin{aligned} & \text { RIN } \\ & \text { GIN } \\ & \text { BIN } \end{aligned}$ | Black level when clamped |  | Analog RGB signal inputs. Input at $100 \%=1 \mathrm{Vp}$-p (max.). To minimize clamp error, input at as low impedance as possible. <br> ICLP turns ON only in the burst flag period. |
| 5 | NC |  |  | NO CONNECTION |
| 6 | SCIN | - |  | Subcarrier input. Input 0.4 to 5.0 V p-p sine wave or pulse. <br> Refer to Notes on Operation, Nos. 2 and 4. |
| 7 | NPIN | 1.7 V when open |  | Pin for switching between NTSC and PAL modes. <br> NTSC: Vcc, PAL: GND |
| 8 | BFOUT | $\begin{aligned} & \mathrm{H}: 3.6 \mathrm{~V} \\ & \mathrm{~L}: 3.2 \mathrm{~V} \end{aligned}$ |  | BF pulse monitoring output. Incapable of driving a $75 \Omega$ load. |


| $\begin{aligned} & \text { Pin } \\ & \text { No. } \end{aligned}$ | Symbol | Pin voltage | Equivalent circuit | Description |
| :---: | :---: | :---: | :---: | :---: |
| 9 | NC |  |  | NO CONNECTION |
| 10 | SYNCIN | 2.2 V |  | Composite sync signal input. Input TTLlevel voltages. $\begin{aligned} & L(\leq 0.8 \mathrm{~V}): \text { SYNC period } \\ & H(\geq 2.0 \mathrm{~V}) \end{aligned}$ |
| 11 | NC |  |  | NO CONNECTION |
| 12 | Vcc1 | 5.0 V | - | Power supply for all circuits other than RGB, composite video and Y/C output circuits. <br> Refer to Notes on Operation, Nos. 3 and 8. |
| 13 | NC |  |  | NO CONNECTION |
| 14 | NC |  |  | NO CONNECTION |
| 15 | COUT | 1.6 V |  | Chroma signal output. Capable of driving a $75 \Omega$ load. <br> Refer to Notes on Operation, Nos. 5 and 7. |
| 16 | YOUT | $\begin{gathered} \text { Black level } \\ 1.35 \mathrm{~V} \end{gathered}$ |  | Y signal output. Capable of driving a $75 \Omega$ load. <br> Refer to Notes on Operation, Nos. 5 and 7 . |


| $\begin{array}{\|l\|} \hline \text { Pin } \\ \text { No. } \\ \hline \end{array}$ | Symbol | Pin voltage | Equivalent circuit | Description |
| :---: | :---: | :---: | :---: | :---: |
| 17 | YTRAP | $\begin{gathered} \text { Black level } \\ 2.13 \mathrm{~V} \end{gathered}$ |  | Pin for reducing cross color caused by the subcarrier frequency component of the $Y$ signal. When the CVOUT pin is in use, connect a capacitor or a capacitor and an inductor in series between YTRAP and GND. Decide capacitance and inductance, giving consideration to cross color and the required resolution. <br> No influence on the YOUT pin. <br> Internal TRAP can be also used. <br> Refer to Notes on Operation, No. 6. |
| 18 | NC |  |  | NO CONNECTION |
| 19 | Vcc2 | 5.0 V | - | Power supply for RGB, composite video and $\mathrm{Y} / \mathrm{C}$ output circuits. Decouple this pin with a large capacitor of $10 \mu \mathrm{~F}$ or above as a high current flows. <br> Refer to Notes on Operation, Nos. 3 and 8. |
| 20 | CVOUT | Black level 0.97 V |  | Composite video signal output. Capable of driving a $75 \Omega$ load. <br> Refer to Notes on Operation, Nos. 5 and 7. |
| $\begin{aligned} & 21 \\ & 22 \\ & 23 \end{aligned}$ | $\begin{aligned} & \text { BOUT } \\ & \text { GOUT } \\ & \text { ROUT } \end{aligned}$ | Black level 1.2 V |  | Analog RGB signal outputs. Capable of driving a $75 \Omega$ load. <br> Refer to Notes on Operation, Nos. 5 and 7. |
| 24 | GND2 | OV | - | Ground for RGB, composite video and Y/C output circuits. The leads to GND1 should be as short and wide as possible. |

Electrical Characteristics $\quad\left(\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{Vcc}=5 \mathrm{~V}\right.$, See the Electrical Characteristics Measurement Circuit.)

| Item | Symbol | S1 | S2 | S3 | S4 | Measurement pin | Measurement conditions | Min. | Typ. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\begin{aligned} & \text { RIN } \\ & \text { GIN } \\ & \text { BIN } \end{aligned}$ | SCIN | NPIN | $\begin{gathered} \text { SYNC } \\ \text { IN } \end{gathered}$ |  |  |  |  |  |  |
| Current consumption 1 | Icc1 | 2.75 V | SG4 | 5V | SG5 | Icc1 | No input signal, SG5: CSYNC TTL level, <br> SG4: SIN wave 3.58 MHz $0.5 \mathrm{Vp}-\mathrm{p}$ Fig. 1 | - | 67 | - | mA |
| Current consumption 2 | Icc2 |  |  |  |  | Icc2 |  | - | 40 | - |  |
| (R, G, BOUT) |  |  |  |  |  |  |  |  |  |  |  |
| RGB output voltage | Vo (R) | SG1 |  |  | 2V | D | SG1 to SG3: DC direct coupling 3.2VDC, $1.0 \mathrm{Vp}-\mathrm{p}$ $\mathrm{f}=200 \mathrm{kHz}$ <br> Pin $9=$ Clamp voltage* Fig. 2 | 0.64 | 0.69 | 0.72 | V |
|  | Vo (G) | SG2 |  |  |  | E |  |  |  |  |  |
|  | Vo (B) | SG3 |  |  |  | F |  |  |  |  |  |
| RGB output frequency characteristics | fc (R) | SG1 |  |  | 2V | D | SG1 to SG3: DC direct coupling 3.2VDC, $1.0 \mathrm{Vp}-\mathrm{p}$ $\mathrm{f}=27 \mathrm{MHz} / 200 \mathrm{kHz}$ Pin $9=$ Clamp voltage Fig. 3 | -5 | -3.2 | - | dB |
|  | fc (G) | SG2 |  |  |  | E |  | -5 | -3.4 | - | dB |
|  | fc (B) | SG3 |  |  |  | F |  | -5 | -3.8 | - | dB |
| (YOUT) |  |  |  |  |  |  |  |  |  |  |  |
| Output sync level | Vo (YS1/2) | $\begin{gathered} \text { SG1 } \\ \text { to } \\ \text { SG3 } \end{gathered}$ | OV | 5V | SG5 | B | SG1 to SG3: 100\% color bar input, 1.0Vp-p (Max.) SG5: CSYNC TTL level Fig. 4 | 0.24 | 0.27 | 0.31 | Vp-p |
| R100\%: Y level | Vo (YR1/2) |  |  |  |  |  |  | 0.19 | 0.215 | 0.24 |  |
| G100\%: Y level | Vo (YG1/2) |  |  |  |  |  |  | 0.38 | 0.405 | 0.43 |  |
| B100\%: Y level | Vo (YB1/2) |  |  |  |  |  |  | 0.06 | 0.076 | 0.09 |  |
| White 100\%: Y level | Vo (YW1/2) |  |  |  |  |  |  | 0.63 | 0.682 | 0.79 |  |
| Output frequency characteristics | fc (Y1/2) | $\begin{gathered} \text { SG1 } \\ \text { to } \\ \text { SG3 } \end{gathered}$ | OV | 5 V | 2V |  | ```SG1 to SG3: DC direct coupling 3.2VDc, \(1.0 \mathrm{Vp}-\mathrm{p}\) \(\mathrm{f}=5 \mathrm{MHz} / 200 \mathrm{kHz}\) Pin \(9=\) Clamp voltage``` | -1 | -0.13 | - | dB |
| (CVOUT) |  |  |  |  |  |  |  |  |  |  |  |
| Output sync level | Vo (YS1/2) | $\begin{array}{\|c} \text { SG1 } \\ \text { to } \\ \text { SG3 } \end{array}$ | OV | 5V | SG5 | C | SG1 to SG3: 100\% color bar input, 1.0Vp-p (Max.) SG5: CSYNC TTL level Fig. 4 | 0.22 | 0.24 | 0.27 | Vp-p |
| R100\%: Y level | Vo (YR1/2) |  |  |  |  |  |  | 0.18 | 0.208 | 0.23 | V |
| G100\%: Y level | Vo (YG1/2) |  |  |  |  |  |  | 0.35 | 0.376 | 0.41 | V |
| B100\%: Y level | Vo (YB1/2) |  |  |  |  |  |  | 0.055 | 0.071 | 0.085 | V |
| White 100\%: Y level | Vo (YW1/2) |  |  |  |  |  |  | 0.61 | 0.66 | 0.75 | V |
| Output frequency characteristics | fc (Y1/2) | $\begin{gathered} \text { SG1 } \\ \text { to } \\ \text { SG3 } \end{gathered}$ | OV | 5 V | 2V |  | ```SG1 to SG3: DC direct coupling 3.2VDC, \(1.0 \mathrm{Vp}-\mathrm{p}\) \(\mathrm{f}=5 \mathrm{MHz} / 200 \mathrm{kHz}\) Pin \(9=\) Clamp voltage``` | -3.3 | -1.53 | - | dB |

[^0]|  |  | S1 | S2 | S3 | S4 |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Item | Symbol | RIN <br> GIN <br> BIN | SCIN | NPIN | $\begin{gathered} \text { SYNC } \\ \text { IN } \end{gathered}$ | Measure- <br> ment <br> pin | Measurement conditions | Min. | Typ. | Max. | Unit |
| (COUT) |  |  |  |  |  |  |  |  |  |  |  |
| Burst level | Vo (BN1/2) | $\begin{aligned} & \text { SG1 } \\ & \text { to } \\ & \text { SG3 } \end{aligned}$ | SG4 | 5 V | SG5 | A |  | 0.24 | 0.282 | 0.34 | Vp-p |
| R chroma ratio | R/BN1/2 |  |  |  |  |  |  | 2.8 | 3.17 | 3.6 |  |
| R phase | өR1/2 |  |  |  |  |  |  | 99 | 104 | 111 | deg |
| G chroma ratio | G/BN1/2 |  |  |  |  |  |  | 2.7 | 3.06 | 3.8 |  |
| G phase | $\theta \mathrm{G} 1 / 2$ |  |  |  |  |  |  | 232 | 238 | 246 | deg |
| B chroma ratio | B/BN1/2 |  |  |  |  |  |  | 1.8 | 2.1 | 2.35 |  |
| B phase | өB1/2 |  |  |  |  |  |  | 341 | 348 | 356 | deg |
| Burst width | tw (B) $1 / 2$ |  |  |  |  |  |  | 2.35 | 2.6 | 2.8 | $\mu \mathrm{s}$ |
| Burst position | to (B) $1 / 2$ |  |  |  |  |  |  | 0.35 | 0.68 | 0.95 | $\mu \mathrm{s}$ |
| Carrier leak | VL1/2 | $\begin{array}{\|l} \text { SG1 } \\ \text { to } \\ \text { SG3 } \end{array}$ | SG4 | 5 V | SG5 |  | SG1 to SG3: <br> No signal, <br> SG4: SIN wave, <br> 3.58 MHz <br> $0.5 \mathrm{Vp}-\mathrm{p}$ <br> SG5: CSYNC <br> TTL level <br> 3.58 MHz component measured. Fig. 6 | - | 6 | 29 | mVp-p |


Electrical Characteristics Measurement Circuit


## Measuring Signals and Output Waveforms



Fig. 1



BOUT
Fig. 2


Fig. $3 \quad \mathrm{fc}=20 \log \frac{\mathrm{Vo}(27 \mathrm{MHz})}{\mathrm{Vo}(200 \mathrm{kHz})}$



Fig. 4

$f=3.58 \mathrm{MHz}$

$\begin{aligned} R / B N & =\frac{V_{0(C R)}}{V_{0}(B N)} \\ G / B N & =\frac{V_{0(C G)}}{V_{0}(B N)} \\ B / B N & =\frac{V_{0(C B)}}{V_{0}(B N)}\end{aligned}$

Fig. 5

Fig. 6

## Application Circuit (NTSC internal TRAP mode)



## Application Circuit (NTSC external TRAP mode)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

## Application Circuit (PAL internal TRAP mode)



## Application Circuit (PAL external TRAP mode)



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## Description of Operation

Analog RGB signals input from Pins 2, 3 and 4 are clamped in the clamping circuit and output from Pins 23, 22 and 21 , respectively.

The matrix circuit performs operations on each input signal, generating luminance signal $Y$ and color difference signals $R-Y$ and $B-Y$. The $Y$ signal enters the delay line to adjust delay time with the chroma signal C. Then, after addition of the CSYNC signal input from Pin 10, the Y signal is output from Pin 16.

A subcarrier input from Pin 6 is input to the phase shifter, where its phase is sfited $90^{\circ}$. Then, the subcarrier is input to the modulators and modulated by the $\mathrm{R}-\mathrm{Y}$ signal and the $\mathrm{B}-\mathrm{Y}$ signal. The modulated subcarriers are mixed, sent to the band-pass filter to eliminate higher harmonic components and finally output from Pin 15 as the $C$ signal. At the same time, $Y$ and $C$ signals are mixed and output from Pin 20 as the composite video signal.

## Burst Signal

The CXA2075M generates burst signals at the timing shown below according to the composite sync signal input.


## Notes on Operation

Be careful of the following when using the CXA2075M.

1. Be sure that analog RGB signals are input at $1.0 \mathrm{Vp}-\mathrm{p}$ maximum and have low enough impedance. High impedance may affect color saturation, hue, etc. Inputting RGB signals in excess of $1.3 \mathrm{Vp}-\mathrm{p}$ may disable the clamp operation.
2. The SC input (Pin 6) can be either a sine wave or a pulse in the range from 0.4 to $5.0 \mathrm{Vp}-\mathrm{p}$.

However, when a pulse is input, its phase may be shifted several degrees from that of the sine wave input. In the IC, the SC input is biased to $1 / 2 \mathrm{Vcc}$. Accordingly, when a $5.0 \mathrm{Vp}-\mathrm{p}$ pulse is input and the duty factor deviates from 50\%, High- and Low-level pulse voltages may exceed Vcc and GND in the IC, which causes subcarrier distortion. In such a case, be very careful that the duty factor keeps to $50 \%$.
3. When designing a printed circuit board pattern, pay careful attention to the routing of the Vcc and GND leads. To decouple the Vcc pin, use tantalum, ceramic or other capacitors with good frequency characteristics. Ground the capacitors by connections shown below as closely to each IC pin as possible. Try to design the leads as short and wide as possible.

```
Vcc1... GND1
Vcc2... GND2
```

Design the pattern so that Vcc is connected to GND via a capacitor at the shortest distance.
4. SC and SYNC input pulses

Attach a resistor and a capacitor to eliminate high-frequency components of SC (Fig. A) and SYNC (Fig. B) before input.


Fig. A


Fig. $B$

Be careful not to input pulses containing high-frequency components. Otherwise, high-frequency components may flow into Vcc, GND and peripheral parts, resulting in malfunctions.
5. Connecting an external resistor to the $75 \Omega$ driver output pin

A capacitance of several dozen picofarads at each pin may start oscillation. To prevent oscillation, design the pattern so that a $75 \Omega$ resistor is mounted near the pin (see Fig. C).


* Make these leads short.

Fig. C

When any of the $75 \Omega$ driver output pins is not in use, leave it unconnected and design the pattern so that no parasitic capacitance is generated on the printed circuit board.
6. YTRAP pin (Pin 17)

There are the following three means of reducing cross color generated by subcarrier frequency components contained in the $Y$ signal.
(1) Install a capacitor of 30 to $68 p F$ between YTRAP and GND. Decide the capacitance by conducting image evaluation, etc., giving consideration to both cross color and resolution.
Relations between capacitance and picture quality are as follows:

| Capacitance | $30 \mathrm{pF} \longleftrightarrow$ 68pF |
| :---: | :---: |
| Cross color <br> Resolution | Large $\longleftrightarrow$ Small <br> High $\longleftrightarrow$ Low |


(2) Connect a capacitor $C$ and an inductor $L$ in series between YTRAP and GND. When the subcarrier frequency is $f 0$, the values $C$ and $L$ are determined by the equation $f_{0}=\frac{1}{2 \pi \sqrt{L C}}$. Decide the values in image evaluation, etc., giving consideration to both cross color and resolution.
Relations between inductor values and picture quality are as follows:

| Inductor value | Small $\longleftrightarrow$ Large |
| :---: | :---: |
| Cross color <br> Resolution | Large $\longleftrightarrow$ Small <br> High $\longleftrightarrow$ Low |



For instance, $\mathrm{L}=68 \mu \mathrm{H}$ and $\mathrm{C}=28 \mathrm{pF}$ are recommended for NTSC. It is necessary to select an inductor L with a sufficiently small DC resistance. Method (2) is more useful for achieving a higher resoluation than method (1). When an even higher resolution is necessary, use of the $S$ terminal (YOUT and COUT) is recommended.
(3) TRAP built in the IC can be used. Connect a resistor which determines to between YTRAP (Pin 17) and Vcc. Refer to Application Circuit. Be very careful of frequency characteristics and picture quality, and then use them.

| NTSC mode | $\mathrm{R}=3.32 \mathrm{k} \Omega$ |
| :--- | :--- |
| PAL mode | $\mathrm{R}=2.61 \mathrm{k} \Omega$ |


7. Driving COUT (Pin 15), YOUT (Pin 16), CVOUT (Pin 20), and B.G.R OUT (Pins 21, 22 and 23) outputs In Pin Description, "Capable of driving a $75 \Omega$ load" means that the pin can drive a capacitor $+75 \Omega+75 \Omega$ load shown in the figure below. In other words, the pin is capable of driving a $150 \Omega$ load in AC.

8. This IC employs a number of $75 \Omega$ driver pins, so oscillation is likely to occur when measures described in Nos. 3 and 5 are not taken thoroughly. Be very careful of oscillation in printed circuit board design and carry out thorough investigations in the actual driving condition.

24PIN SOP (PLASTIC)



PACKAGE STRUCTURE

| SONY CODE | SOP-24P-L01 |
| :--- | :---: |
| EIAJ CODE | *SOP024-P-0300-A |
| JEDEC CODE | - |


| MOLDING COMPOUND | EPOXY/PHENOL RESIN |
| :--- | :--- |
| LEAD TREATMENT | SOLDER PLATING |
| LEAD MATERIAL | COPPER ALLOY / 42ALLOY |
| PACKAGE WEIGHT | 0.3 g |


[^0]:    * Clamp voltage: voltage appearing at Pin 9 when CSYNC is input.

