Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 20<mark>10</mark> Renesas Electronics Corporation

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MOS FIELD EFFECT POWER TRANSISTOR **2SK1852**

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK1852 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

• Low On-state Resistance

RDS(on) \leq 0.15 Ω (VGS = 10 V, ID = 5.0 A) RDS(on) \leq 0.2 Ω (VGS = 4 V, ID = 5.0 A)

- Low Ciss Ciss = 1 250 pF TYP.
- Built-in G-S Gate Protection Diode

QUALITY GRADE

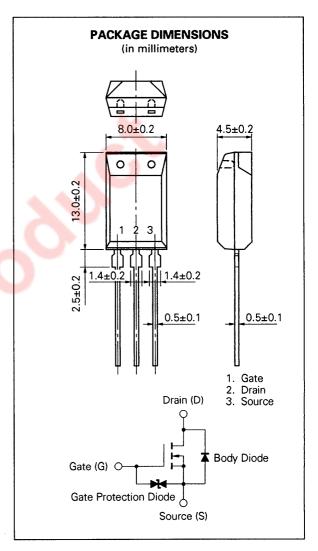
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS

Drain to Source Voltage	Voss	100	V
Gate to Source Voltage	VGSS(AC)	±20	V
Gate to Source Voltage	Vgss(DC)	+20, -10	٧
Drain Current (DC)	ID(DC)	±10	Α
Drain Current (pulse)	D(pulse)*	±40	Α
Total Power Dissipation	(Ta = 25 °C) PT	1.8	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
	_		

* PW \leq 10 μ s, Duty Cycle \leq 1 %

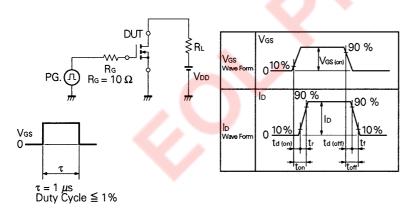




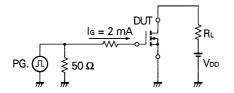
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

CHADACTEDICTIC	CVAADO	AAINI	77/7	1447/		TEGT CONDITIONS	
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Drain to Source On-state Resistance	RDS(on)		0.12	0.15	Ω	Vgs = 10 V, lp = 5 A	
Drain to Source On-state Resistance	Ros(on)		0.15	0.2	Ω	Vgs = 4 V, lp = 5 A	
Gate to Source Cutoff Voltage	VGS(off)	1.0		2.5	V	Vps = 10 V, lp = 1 mA	
Forward Transfer Admittance	y fs	5.5			S	Vps = 10 V, lp = 5 A	
Drain Leakage Current	Ioss			10	μА	Vps = 100 V, Vgs = 0	
Gate to Source Leakage Current	lgss			±10	μА	$V_{GS} = \pm 20 \text{ V, } V_{DS} = 0$	
Input Capacitance	Ciss		1 250		pF	V _{DS} = 10 V V _{GS} = 0	
Output Capacitance	Coss		320		pF		
Reverse Transfer Capacitance	Crss		45		pF	f = 1 MHz	
Turn-On Delay Time	td(on)		15		ns	$V_{GS(on)}=10 \text{ V}$ $V_{DD}=50 \text{ V}$ $I_{D}=5 \text{ A, Rg}=10 \Omega$ $R_{L}=10 \Omega$	
Rise Time	tr		60		ns		
Turn-Off Delay Time	td(off)		130		ns		
Fall Time	tr		70		ns		
Total Gate Charge	QG		27	4	nC	Vgs = 10 V lb = 10 A	
Gate to Source Charge	Qgs		4		nC		
Gate to Drain Charge	QGD		6		nC	V 08 = 00 V	
Diode Forward Voltage	V _F (S-D)		1.0		٧	Vgs = 0, Ip = 10 A	
Reverse Recovery Time	trr		150		ns	I _F = 10 A, V _{GS} = 0 di/dt = 50 A/μs	
Reverse Recovery Charge	Qrr		300		nC		

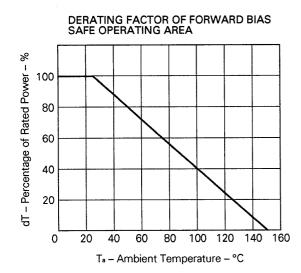
Test Circuit 1: Switching Time

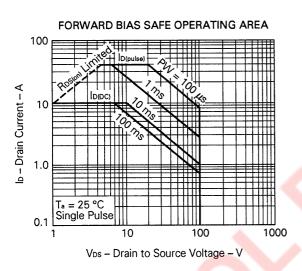


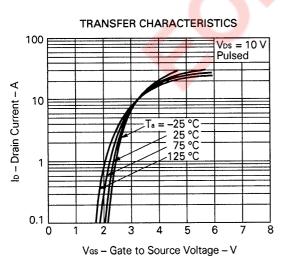
Test Circuit 2: Gate Charge

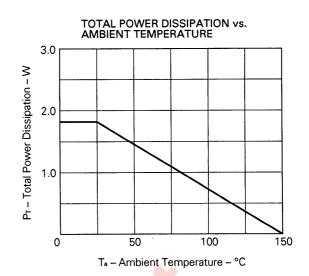


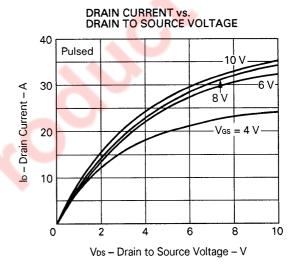
TYPICAL CHARACTERISTICS (Ta = 25 °C)

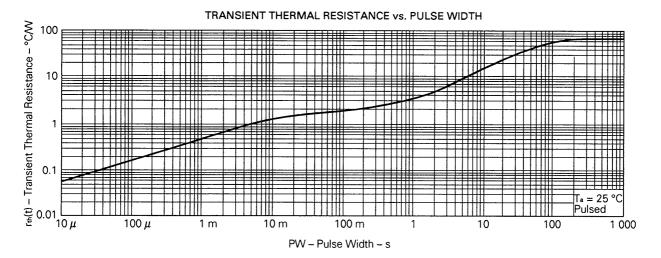


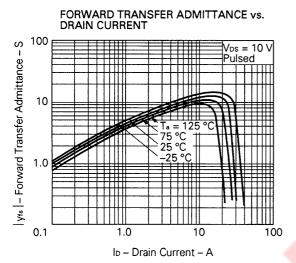


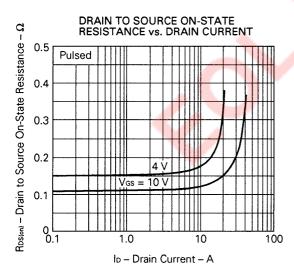


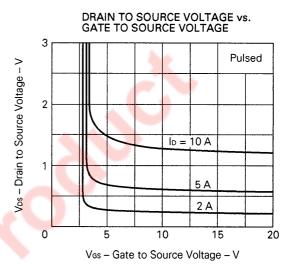


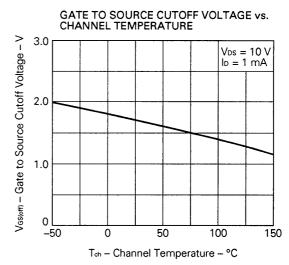


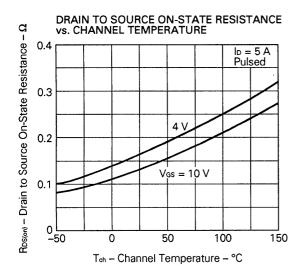


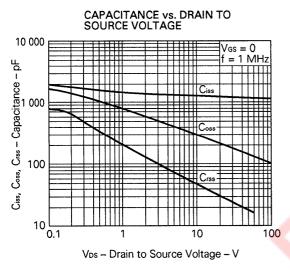


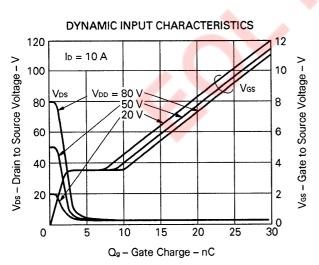


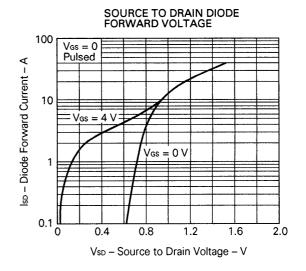


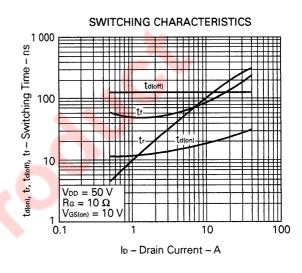


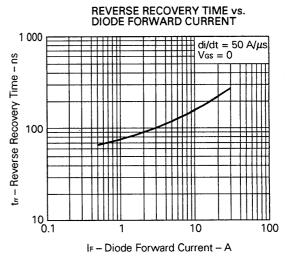












Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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