

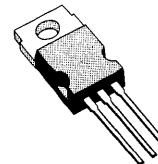
**N - CHANNEL ENHANCEMENT MODE
POWER MOS TRANSISTOR**

PRELIMINARY DATA

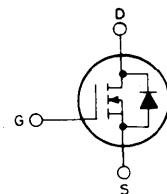
TYPE	V _{DSS}	R _{DS(on)}	I _D
STVHD90	50 V	0.023 Ω	52 A

- VERY HIGH DENSITY
- VERY LOW R_{DS} (on)
- VERY HIGH CURRENT
- HIGH TRANSCONDUCTANCE/C_{rss} RATIO
- LOW DRIVE ENERGY
- ULTRA FAST SWITCHING

N - channel enhancement mode very high density POWER MOS transistors. Easy drive and low on voltage make this device ideal for automotive and industrial applications requiring high current and low on-losses. Typical uses are actuators lamp and motor control in the automotive and industrial environments. It can also be used in DC/DC converters.



TO-220

 INTERNAL SCHEMATIC
DIAGRAM

ABSOLUTE MAXIMUM RATINGS

V _{DS}	Drain-source voltage (V _{GS} = 0)	50	V
V _{GS}	Gate-source voltage	±20	V
I _D	Drain current (cont.) at T _c = 25°C	52	A
I _D	Drain current (cont.) at T _c = 125°C	32	A
I _{DM} (*)	Drain current (pulsed)	200	A
I _{DLM}	Drain inductive current clamped	200	A
P _{tot}	Total dissipation at T _c < 25°C	125	W
	Derating factor	1	W/°C
T _{stg}	Storage temperature	-65 to 150	°C
T _j	Max. operating junction temperature	150	°C

(*) Pulse width limited by safe operating area

THERMAL DATA

$R_{\text{thj} - \text{case}}$	Thermal resistance junction-case	max	1	$^{\circ}\text{C}/\text{W}$
T_L	Maximum lead temperature for soldering purpose		275	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_{\text{case}} = 25^{\circ}\text{C}$ unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$	$V_{GS} = 0$	50			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$			250		μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{DS} = \text{Max Rating} \times 0.8$	$T_c = 125^{\circ}\text{C}$	1000	1000		μA

ON (*)

$V_{GS\text{ (th)}}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 250 \mu\text{A}$	2		4	V
$R_{DS\text{ (on)}}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$	$I_D = 30 \text{ A}$			23	$\text{m}\Omega$

DYNAMIC

g_{fs}	Forward transconductance	$V_{DS} = 25 \text{ V}$	$I_D = 30 \text{ A}$		30		mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$	$f = 1 \text{ MHz}$		2500 850 120	3000 1000 150	pF pF pF

SWITCHING

$t_d\text{ (on)}$ t_r $t_d\text{ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	$V_{DD} = 40 \text{ V}$ $V_i = 50 \text{ V}$ (see test circuit)	$I_D = 25 \text{ A}$ $R_i = 50 \Omega$		40 100 250 170	ns ns ns ns
Q_g	Total Gate Charge	$V_{DD} = 25 \text{ V}$ $V_{GS} = 10 \text{ V}$	$I_D = 30 \text{ A}$		56	nC

ELECTRICAL CHARACTERISTICS (Continued)

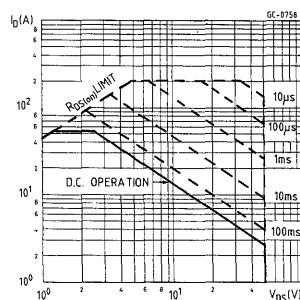
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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SOURCE DRAIN DIODE

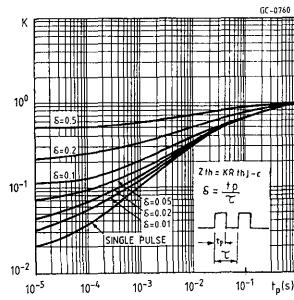
I _{SD} I _{SDM} (*)	Source-drain current Source-drain current (pulsed)			52 200	A A
V _{SD}	Forward on voltage	I _{SD} = 52 A V _{GS} = 0		1.5	V
t _{rr}	Reverse recovery time	I _{SD} = 52 A di/dt = 100 A/μs V _{GS} = 0	70		ns
Q _{rr}	Reverse recovery charge		110		μC

(•) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%

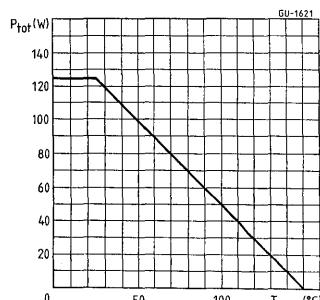
Safe operating areas



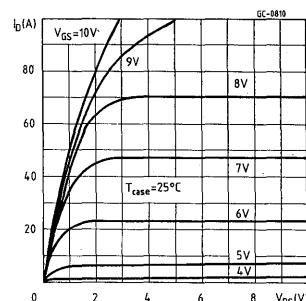
Thermal impedance



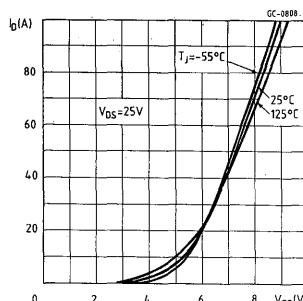
Derating curve



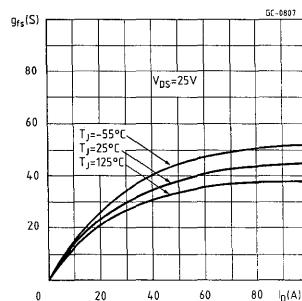
Output characteristics



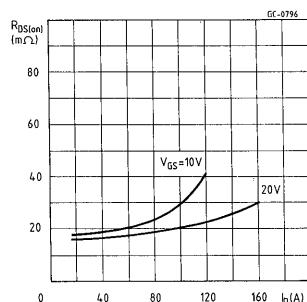
Transfer characteristics



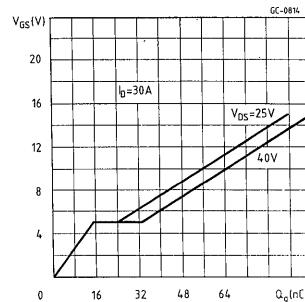
Transconductance



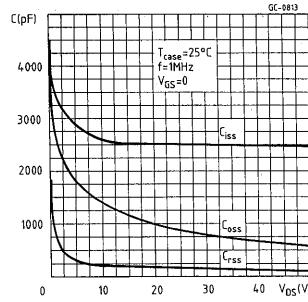
Static drain-source on resistance



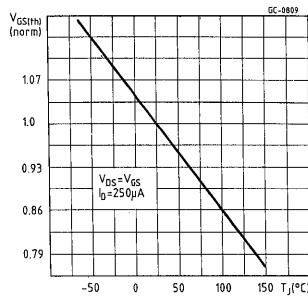
Gate charge vs gate-source voltage



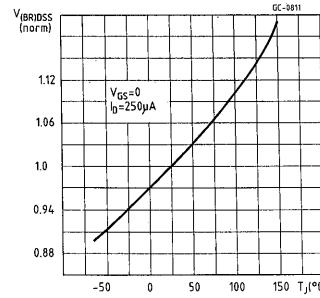
Capacitance variation



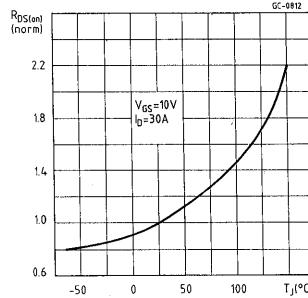
Normalized gate threshold voltage vs temperature



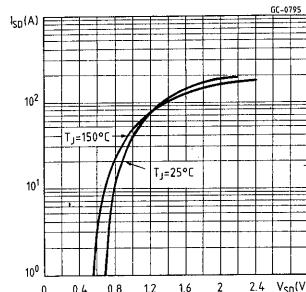
Normalized breakdown voltage vs temperature



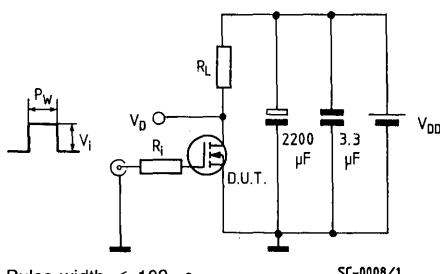
Normalized on resistance vs temperature



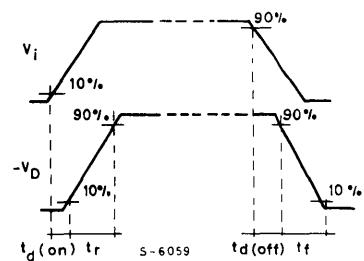
Static drain diode forward characteristics



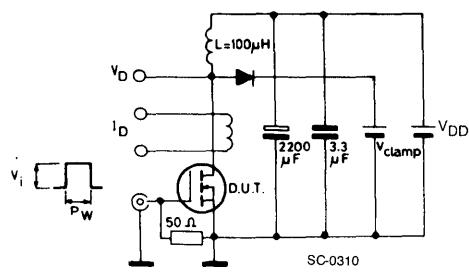
Switching times test circuit for resistive load



Switching time waveforms for resistive load

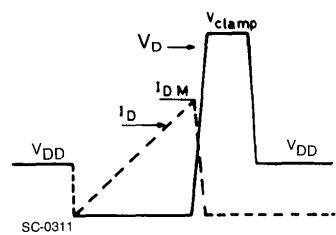


Clamped inductive load test circuit

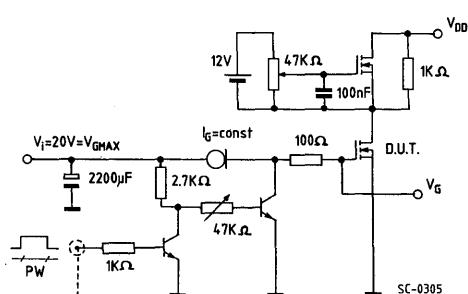


$V_i = 12 \text{ V}$ - Pulse width: adjusted to obtain specified I_{DM} , $V_{\text{clamp}} = 0.75 V_{(\text{BR}) \text{ DSS}}$.

Clamped inductive waveforms



Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit