

MOS FIELD EFFECT POWER TRANSISTOR

2SK1292

SWITCHING

N-CHANNEL POWER MOS FET

INDUSTRIAL USE

DESCRIPTION

The 2SK1292 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} \leq 0.08 \Omega$ ($V_{GS} = 10 \text{ V}$, $I_D = 10 \text{ A}$)
 $R_{DS(on)} \leq 0.1 \Omega$ ($V_{GS} = 4 \text{ V}$, $I_D = 10 \text{ A}$)
- Low C_{iss} $C_{iss} = 2\ 200 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diode

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

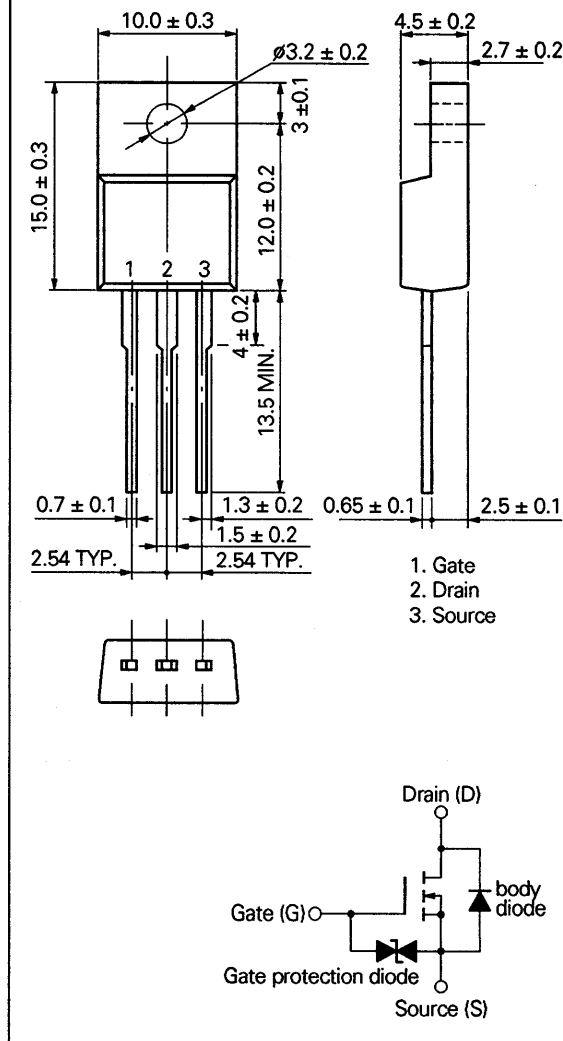
ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DSS}	100	V
Gate to Source Voltage	$V_{GSS(AC)}$	± 20	V
Drain Current (DC)	$I_D(DC)$	± 20	A
Drain Current (pulse)	$I_D(pulse)^*$	± 80	A
Total Power Dissipation ($T_c = 25^\circ\text{C}$)	P_{T1}	35	W
Total Power Dissipation ($T_a = 25^\circ\text{C}$)	P_{T2}	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

PACKAGE DIMENSIONS

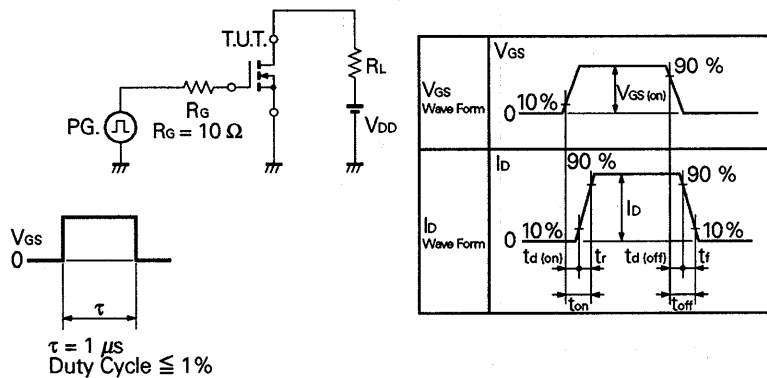
(in millimeters)



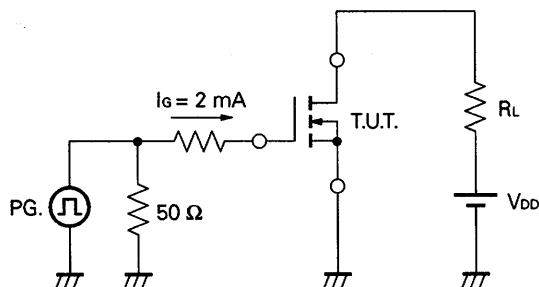
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		0.07	0.08	Ω	V _{GS} = 10 V, I _D = 10 A
Drain to Source On-state Resistance	R _{DS(on)}		0.08	0.1	Ω	V _{GS} = 4.0 V, I _D = 10 A
Gate to Source Cutoff Voltage	V _{GS(off)}	1.0		2.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	12			S	V _{DS} = 10 V, I _D = 10 A
Drain Leakage Current	I _{DSS}			10	μA	V _{DS} = 100 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0
Input Capacitance	C _{iss}		2 200		pF	V _{DS} = 10 V
Output Capacitance	C _{oss}		550		pF	V _{GS} = 0
Reverse Transfer Capacitance	C _{res}		90		pF	f = 1 MHz
Turn-On Delay Time	t _{d(on)}		25		ns	V _{GS(on)} = 10 V V _{DD} = 50 V I _D = 15 A, R _G = 10 Ω R _L = 3.3 Ω
Rise Time	t _r		160		ns	
Turn-Off Delay Time	t _{d(off)}		200		ns	
Fall Time	t _f		150		ns	
Total Gate Charge	Q _G		50		nC	V _{GS} = 10 V I _D = 30 A V _{DD} = 80 V
Gate to Source Charge	Q _{GS}		10		nC	
Gate to Drain Charge	Q _{GD}		10		nC	
Diode Forward Voltage	V _{SD}		1.1		V	I _{SD} = 20 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		200		ns	I _F = 30 A, V _{GS} = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Q _{rr}		550		nC	

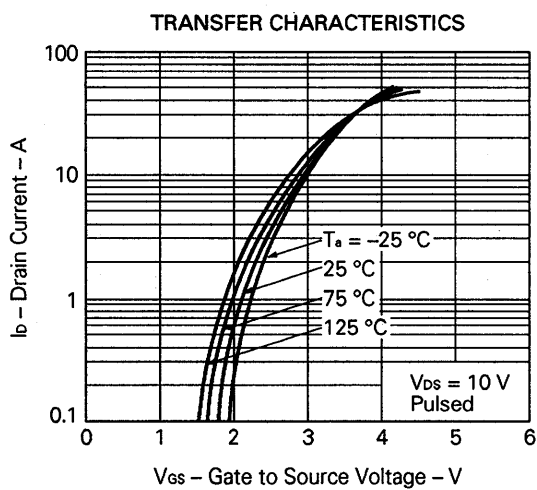
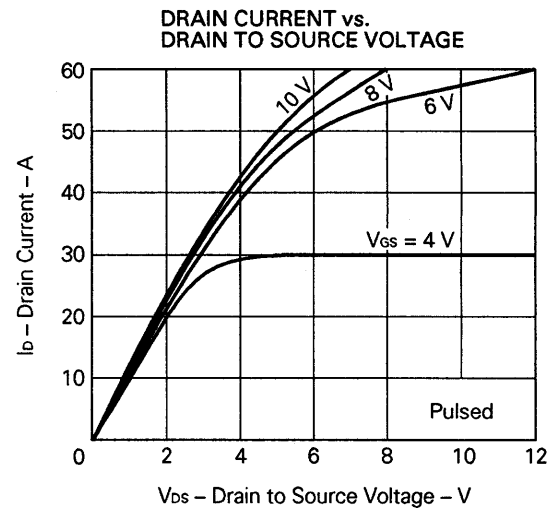
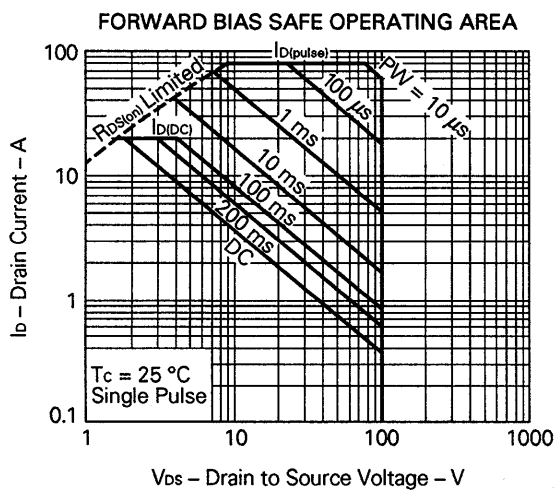
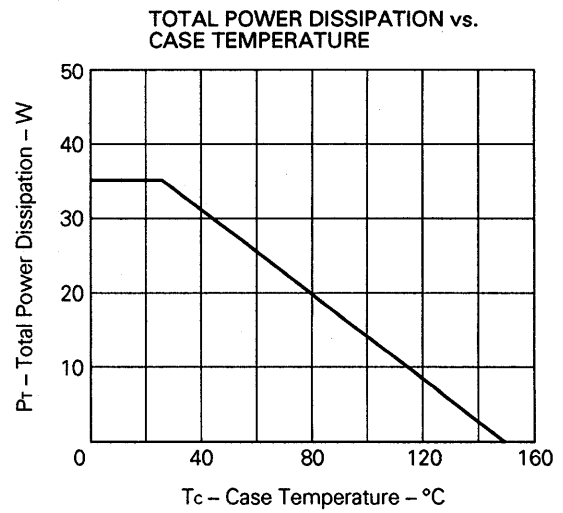
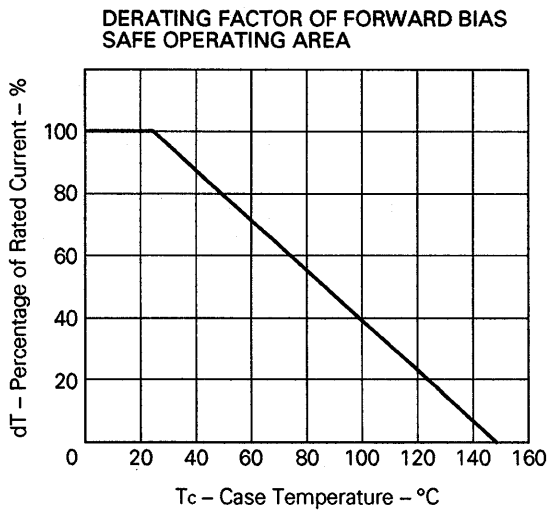
Test Circuit 1: Switching Time

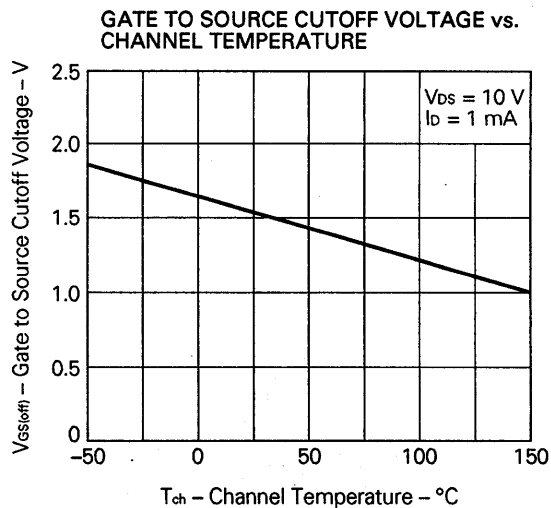
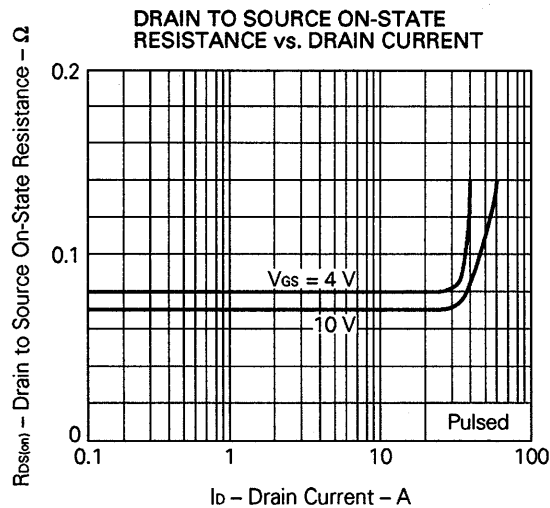
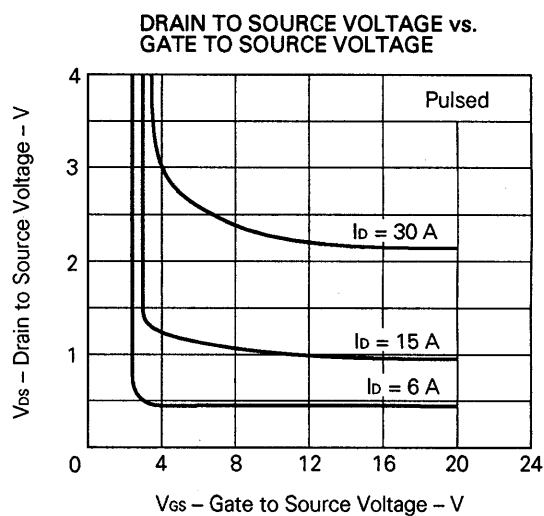
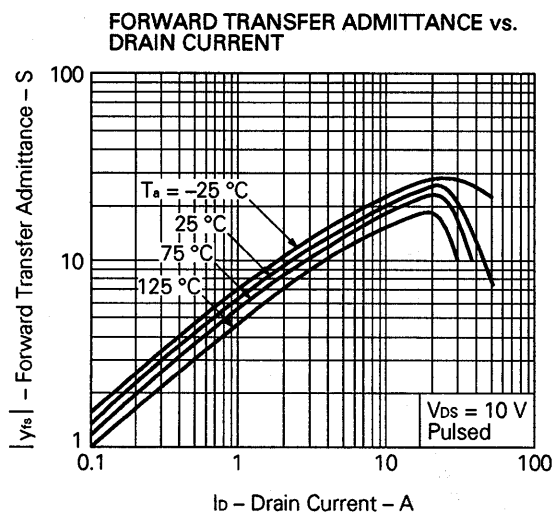
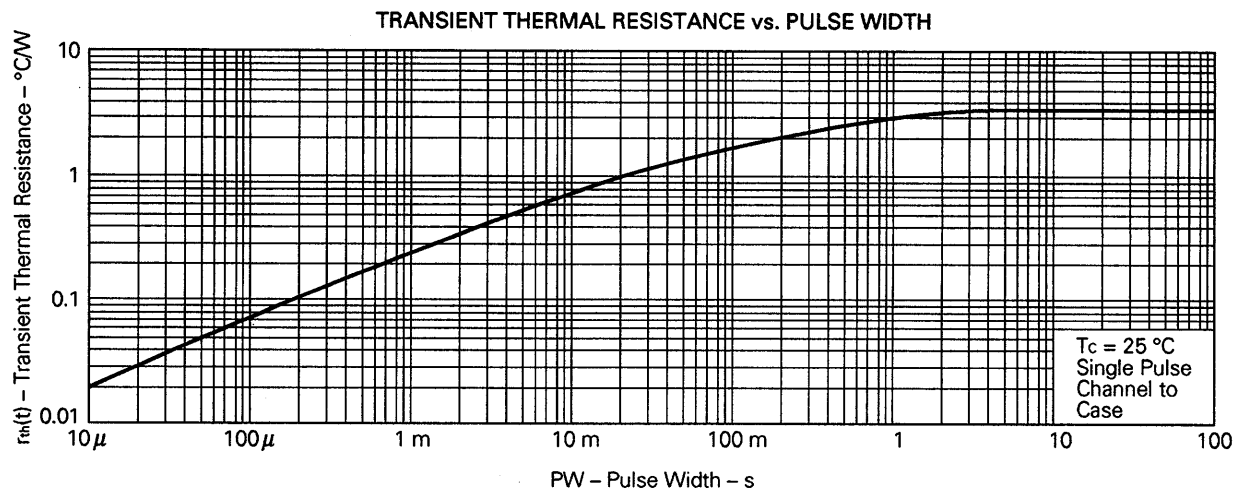


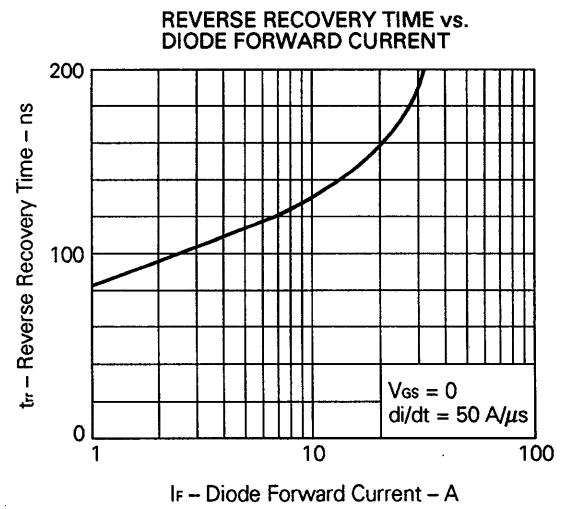
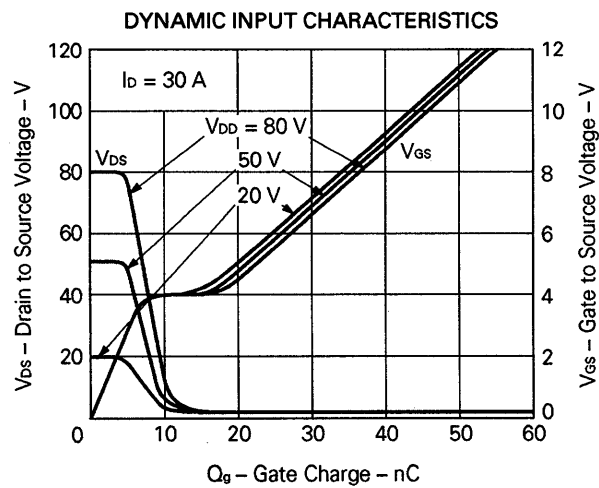
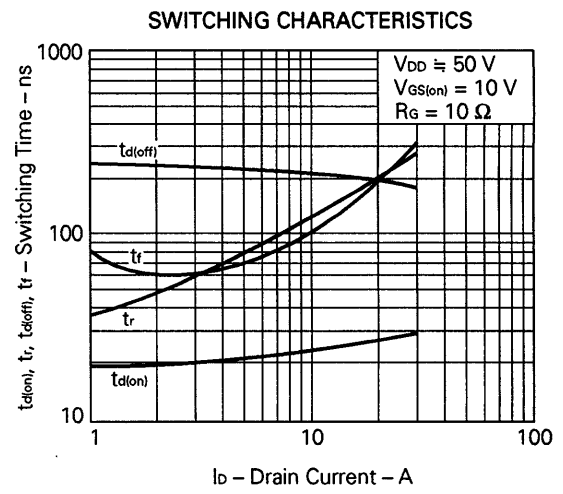
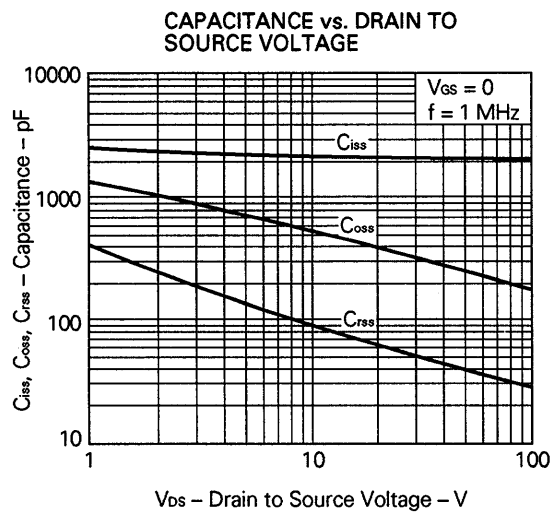
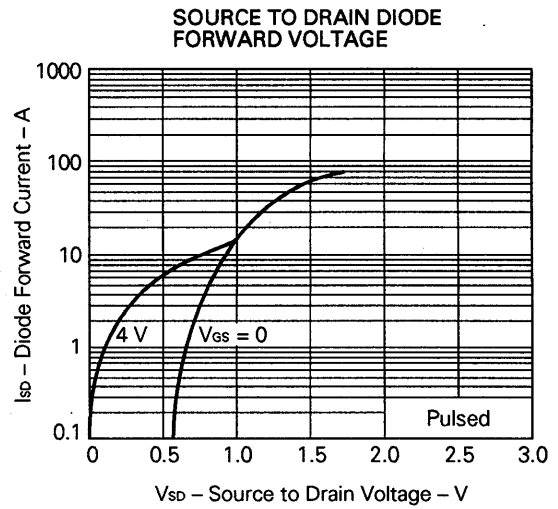
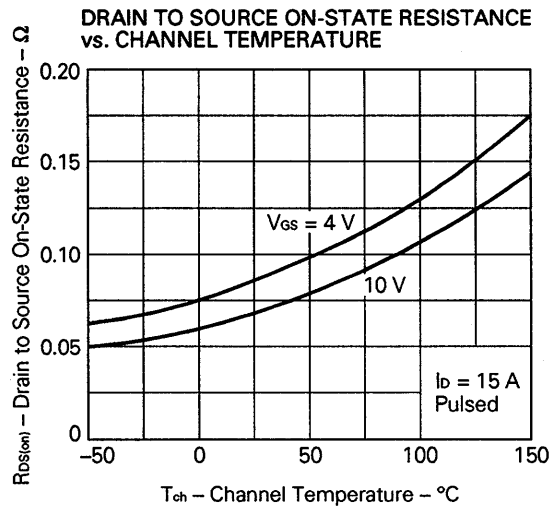
Test Circuit 2: Gate Charge



TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)







Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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