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# **PHD3055E**

## N-channel TrenchMOS standard level FET

Rev. 07 — 26 February 2010

**Product data sheet** 

### 1. Product profile

#### 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

#### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

#### 1.3 Applications

■ DC-to-DC convertors

Switched-mode power supplies

#### 1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{\text{DS}}$	drain-source voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}$	-	-	60	V
$I_D$	drain current	$T_{mb} = 25 ^{\circ}\text{C}; V_{GS} = 10 \text{V};$ see <u>Figure 1</u> and <u>3</u>	-	-	10.3	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>	-	-	33	W
Dynamic	characteristics					
$Q_{GD}$	gate-drain charge	$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A};$ $V_{DS} = 44 \text{ V}; T_j = 25 \text{ °C};$ see Figure 12	-	3.2	-	nC
Static ch	naracteristics					
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 5.5 \text{ A};$ $T_j = 25 \text{ °C};$ see Figure 10 and 11	-	120	150	mΩ



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## 2. Pinning information

Table 2. Pinning information

	_				
Pin	Symbol	Description		Simplified outline	Graphic symbol
1	G	gate			
2	D	drain	[1]	mb	D
3	S	source			$G \longrightarrow A$
mb	D	mounting base; connected to drain		1 3	mbb076 S
				SOT428 (DPAK)	

<sup>[1]</sup> It is not possible to make connection to pin 2

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHD3055E	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

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## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	60	V
$V_{DGR}$	drain-gate voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}; R_{GS} = 20 \text{ k}\Omega$	-	60	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; see <u>Figure 1</u>	-	7.3	Α
		$V_{GS} = 10 \text{ V}; T_{mb} = 25 \text{ °C}; \text{ see } \frac{\text{Figure 1}}{\text{A}} \text{ and } \frac{3}{\text{A}}$	-	10.3	Α
I <sub>DM</sub>	peak drain current	$t_p \le 10 \ \mu s$ ; pulsed; $T_{mb} = 25 \ ^{\circ}C$ ; see Figure 3	-	41	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>	-	33	W
T <sub>stg</sub>	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
Source-di	ain diode				
Is	source current	T <sub>mb</sub> = 25 °C	-	10.3	Α
I <sub>SM</sub>	peak source current	$t_p \le 10 \ \mu s$ ; pulsed; $T_{mb} = 25 \ ^{\circ}C$	-	41	Α
Avalanch	ruggedness				
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $I_D$ = 3.3 A; $V_{sup}$ ≤ 25 V; $R_{GS}$ = 50 Ω; unclamped; $t_p$ = 0.22 ms	-	25	mJ
I <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche current	$V_{GS}$ = 10 V; $V_{sup} \le$ 25 V; $R_{GS}$ = 50 $\Omega$ ; $T_{j(init)}$ = 25 °C; unclamped; see <u>Figure 4</u>	-	10.3	Α

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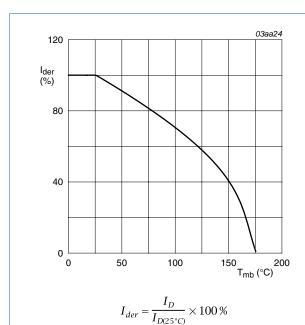


Fig 1. Normalized continuous drain current as a function of mounting base temperature

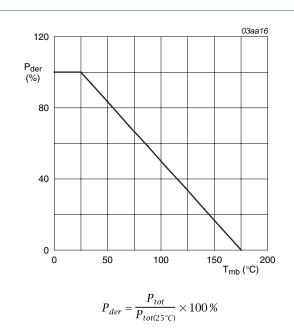
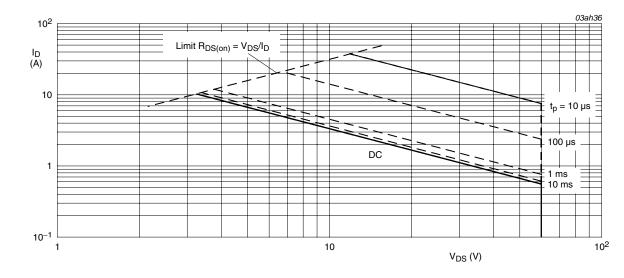


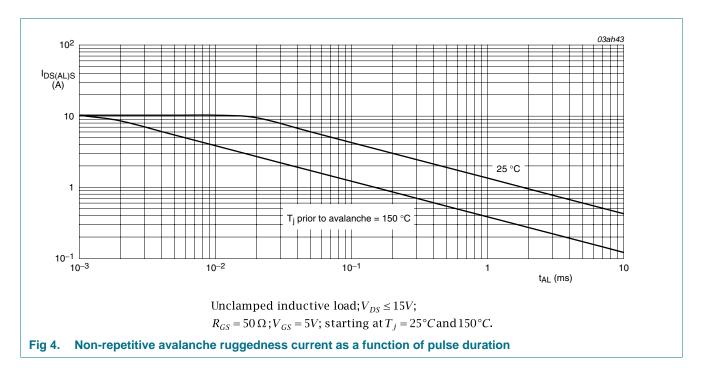
Fig 2. Normalized total power dissipation as a function of mounting base temperature



 $T_{mb} = 25$ °C;  $I_{DM}$  is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

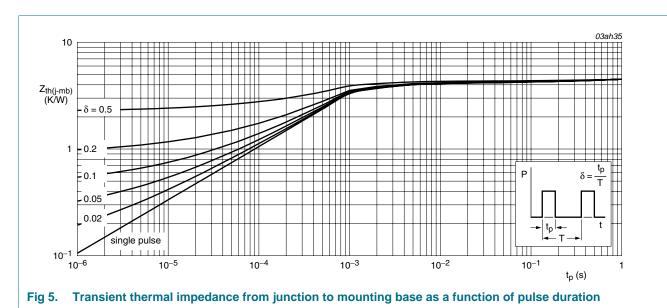
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### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	see Figure 5	-	-	4.5	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	SOT428 minimum footprint; mounted on a PCB	-	75	-	K/W
		SOT404minimum footprint; mounted on a PCB	-	50	-	K/W



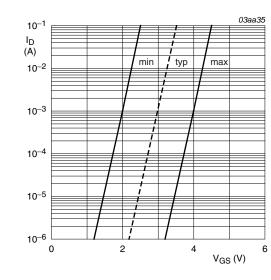
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### 6. Characteristics

Table 6. Characteristics

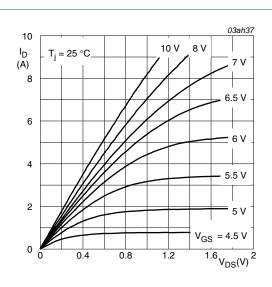
Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
V <sub>(BR)DSS</sub>	drain-source	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ °C}$	55	-	-	V
	breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = 175$ °C; see Figure 9	1	-	-	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = -55$ °C; see <u>Figure 9</u>	-	-	6	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = 25$ °C; see Figure 9	2	3	4	V
I <sub>DSS</sub>	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ °C}$	-	-	500	μΑ
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.05	10	μΑ
I <sub>GSS</sub>	gate leakage current	$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nA
DOON	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 5.5 A; T <sub>j</sub> = 175 °C; see <u>Figure 10</u> and <u>11</u>	-	250	315	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 5.5 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see Figure 10 and 11	-	120	150	mΩ
Dynamic	characteristics					
Q <sub>G(tot)</sub>	total gate charge	$I_D = 10 \text{ A}; V_{DS} = 44 \text{ V}; V_{GS} = 10 \text{ V};$	-	5.8	-	nC
$Q_{GS}$	gate-source charge	$T_j = 25$ °C; see <u>Figure 12</u>	-	1.5	-	nC
$Q_{GD}$	gate-drain charge		-	3.2	-	nC
C <sub>iss</sub>	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	190	250	pF
C <sub>oss</sub>	output capacitance	$T_j = 25$ °C; see <u>Figure 13</u>	-	55	80	pF
C <sub>rss</sub>	reverse transfer capacitance		-	40	50	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 2.7 \Omega; V_{GS} = 10 \text{ V};$	-	3	10	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 5.6 \Omega; T_j = 25 \text{ °C}$	-	26	35	ns
d(off)	turn-off delay time		-	8	15	ns
t <sub>f</sub>	fall time		-	10	20	ns
Source-d	rain diode					
$V_{SD}$	source-drain voltage	$I_S = 10 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ °C}$ ; see Figure 14	-	1.1	1.5	V
t <sub>rr</sub>	reverse recovery time	$I_S = 10 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	-	32	-	ns
Q <sub>r</sub>	recovered charge	$V_{DS} = 25 \text{ V}; T_j = 25 \text{ °C}$	-	50	-	nC

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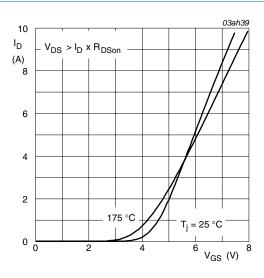
 $T_{j} = 25 \,^{\circ}C; V_{DS} = 5V$ 

Fig 6. Sub-threshold drain current as a function of gate-source voltage



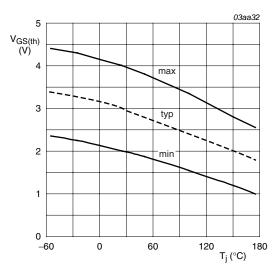
 $T_j = 25^{\circ}C$ 

Fig 7. Output characteristics: drain current as a function of drain-source voltage; typical values



 $T_j = 25$ °C and 175°C;  $V_{DS} > I_D \times R_{DSon}$ 

Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values



 $I_D = 1 \, mA; V_{DS} = V_{GS}$ 

Fig 9. Gate-source threshold voltage as a function of junction temperature

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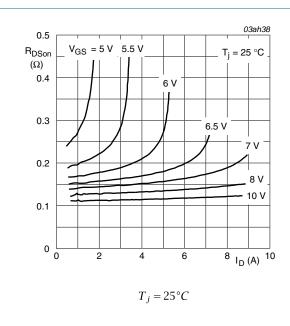


Fig 10. Drain-source on-state resistance as a function of drain current; typical values

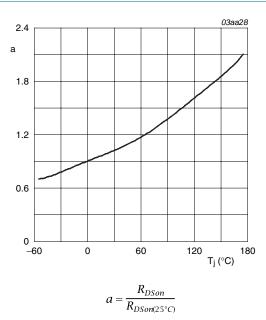
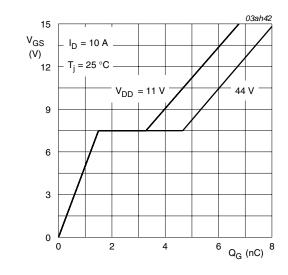


Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature



 $I_D = 10A; V_{DD} = 11V \text{ and } 44V$ 

Fig 12. Gate-source voltage as a function of gate charge; typical values

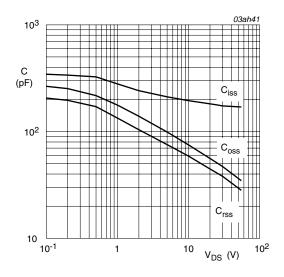


Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

 $V_{GS} = 0V; f = 1MHz$ 

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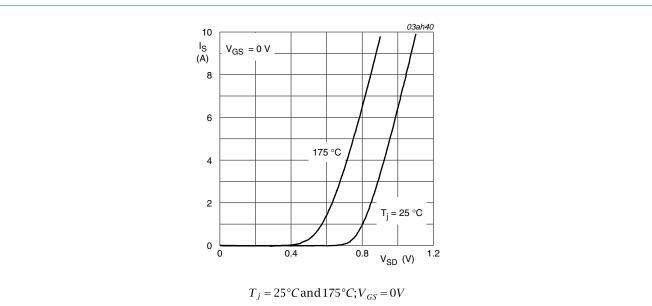


Fig 14. Source current as a function of source-drain voltage; typical values

### 7. Package outline

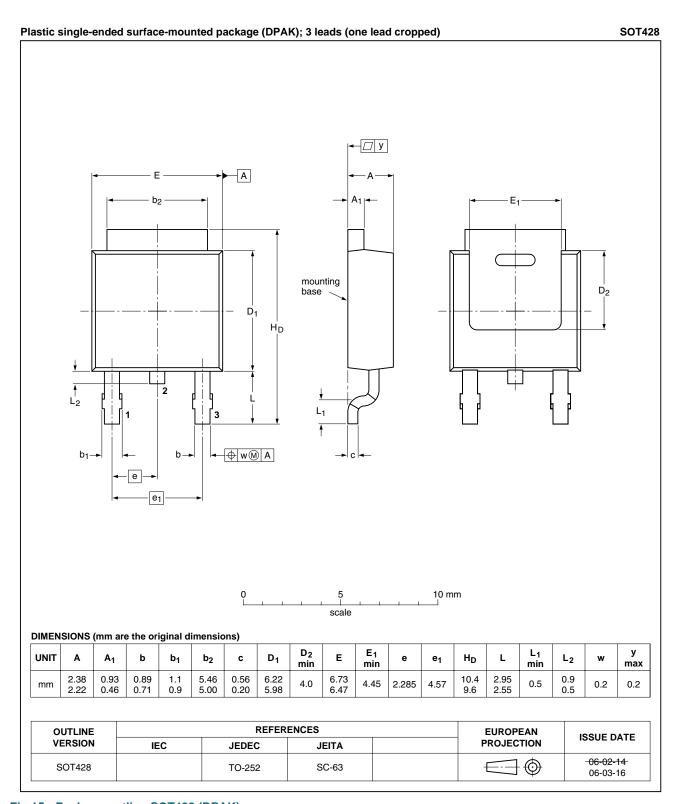


Fig 15. Package outline SOT428 (DPAK)

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## 8. Revision history

#### Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHD3055E_7	20100226	Product data sheet	-	PHP_PHD3055E-06
Modifications:	guidelines  Legal texts	of this data sheet has be of NXP Semiconductors. have been adapted to the or PHD3055E separated to	e new company name w	nere appropriate.
PHP_PHD3055E-06 (9397 750 09354)	20020325	Product data	-	-

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### 9. Legal information

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Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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