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FDD86102

N-Channel Shielded Gate PowerTrench[®] MOSFET

100 V, 36 A, 24 mΩ

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 24 mΩ at $V_{GS} = 10$ V, $I_D = 8$ A
- Max $r_{DS(on)}$ = 38 mΩ at $V_{GS} = 6$ V, $I_D = 6$ A
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- Very low Q_g and Q_{gd} compared to competing trench technologies
- Fast switching speed
- 100% UIL tested
- RoHS Compliant

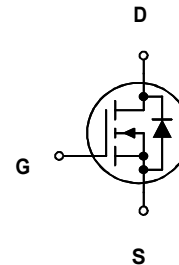
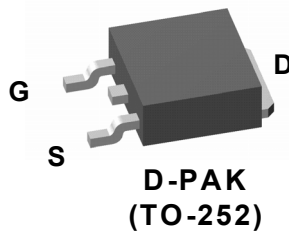


General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench[®] process that incorporates Shielded Gate technology. This process has been optimized for $r_{DS(on)}$, switching performance and ruggedness.

Application

- DC - DC Conversion



MOSFET Maximum Ratings $T_C = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous $T_C = 25$ °C	36	A
	-Continuous $T_A = 25$ °C (Note 1a)	8	
	-Pulsed (Note 4)	75	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	121	mJ
P_D	Power Dissipation $T_C = 25$ °C	62	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	3.1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD86102	FDD86102	D-PAK(TO-252)	13 "	16 mm	2500 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		67		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2	3.1	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-8.5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 8\text{ A}$		19	24	m Ω
		$V_{GS} = 6\text{ V}, I_D = 6\text{ A}$		26	38	
		$V_{GS} = 10\text{ V}, I_D = 8\text{ A}, T_J = 125\text{ }^\circ\text{C}$		33	44	
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 8\text{ A}$		21		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		780	1035	pF
C_{oss}	Output Capacitance			180	240	pF
C_{riss}	Reverse Transfer Capacitance			15	25	pF
R_g	Gate Resistance			0.4		Ω

Switching Characteristics

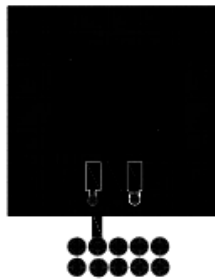
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_D = 8\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		7.6	15	ns	
t_r	Rise Time			3	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			13.4	24	ns	
t_f	Fall Time			2.9	10	ns	
Q_g	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$		13.4	19	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to } 5\text{ V}$	$V_{DD} = 50\text{ V},$ $I_D = 8\text{ A}$		7.6	11	nC
Q_{gs}	Gate to Source Gate Charge				4.0		nC
Q_{gd}	Gate to Drain "Miller" Charge				3.7		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 8\text{ A}$ (Note 2)		0.8	1.3	V
		$V_{GS} = 0\text{ V}, I_S = 2.6\text{ A}$ (Note 2)		0.7	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 8\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		43	68	ns
Q_{rr}	Reverse Recovery Charge			43	68	nC

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. $40\text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper.



b. $96\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < $300\text{ }\mu\text{s}$, Duty cycle < 2.0%.

3. E_{AS} 121 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$, $L = 3\text{ mH}$, $I_{AS} = 9\text{ A}$, $V_{DD} = 100\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 30\text{ A}$.

4. Pulsed Drain current is tested at $300\text{ }\mu\text{s}$ with 2% duty cycle. For repetitive pulses, the pulse width is limited by the maximum junction temperature.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

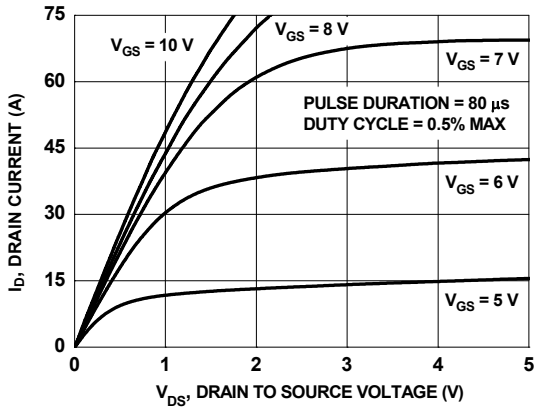


Figure 1. On-Region Characteristics

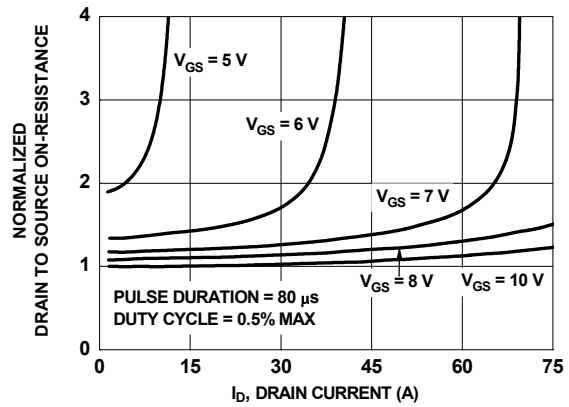


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

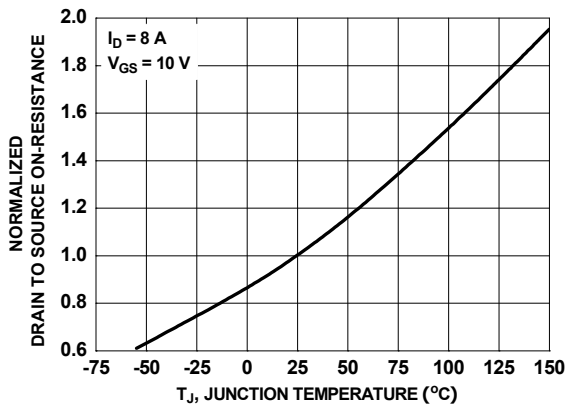


Figure 3. Normalized On-Resistance vs Junction Temperature

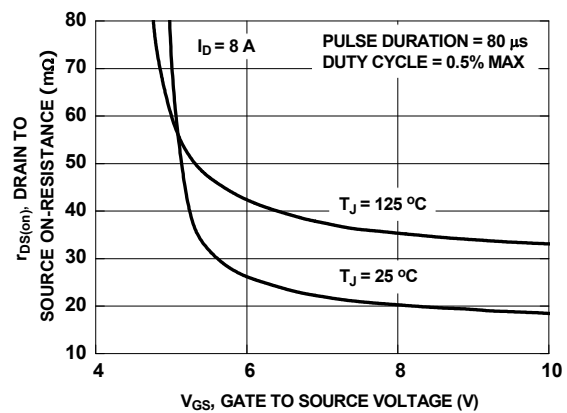


Figure 4. On-Resistance vs Gate to Source Voltage

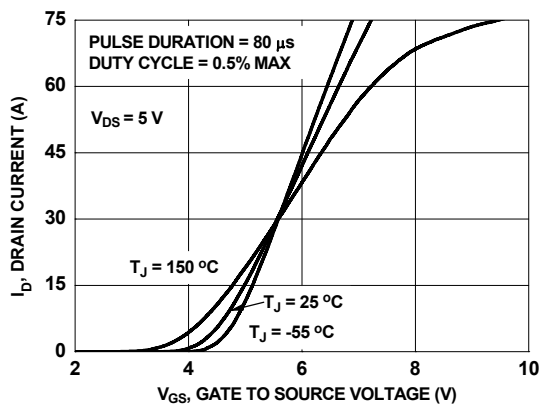


Figure 5. Transfer Characteristics

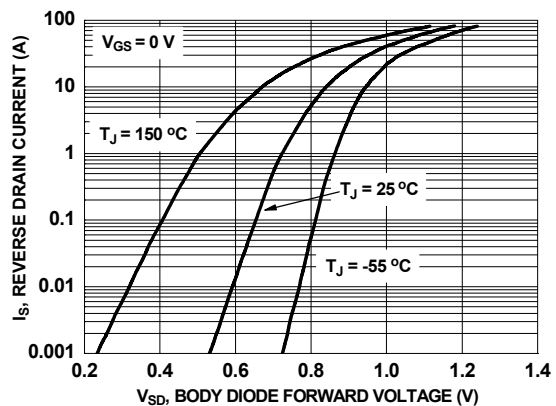


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

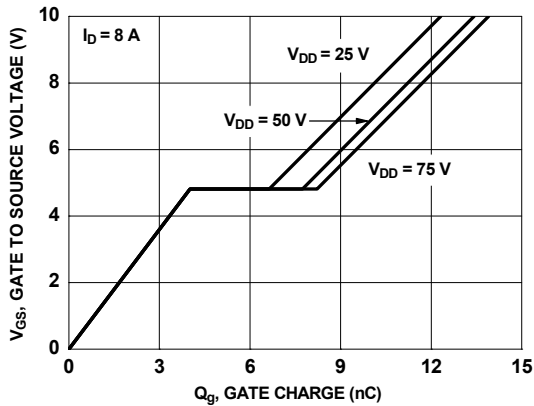


Figure 7. Gate Charge Characteristics

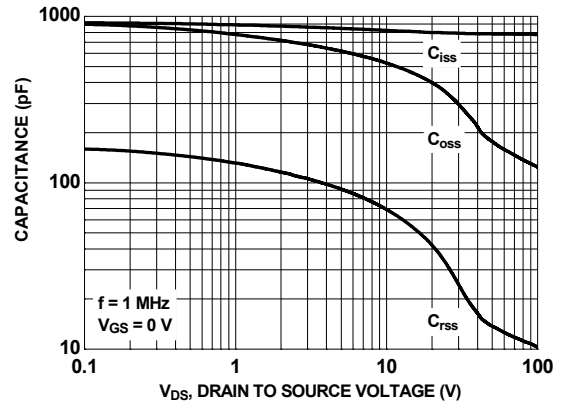


Figure 8. Capacitance vs Drain to Source Voltage

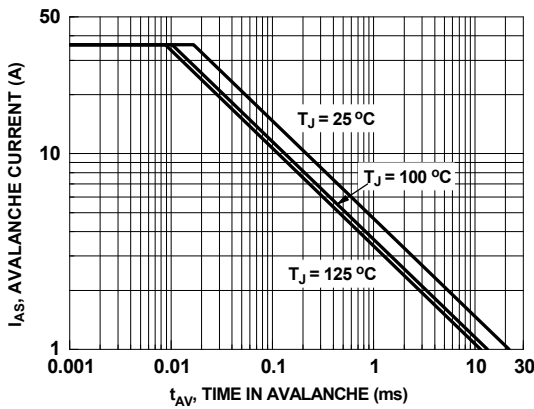


Figure 9. Unclamped Inductive Switching Capability

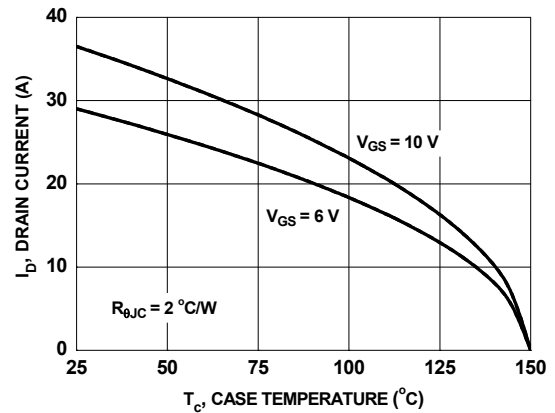


Figure 10. Maximum Continuous Drain Current vs Case Temperature

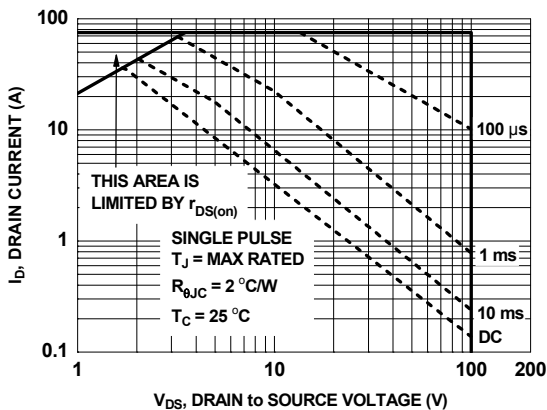


Figure 11. Forward Bias Safe Operating Area

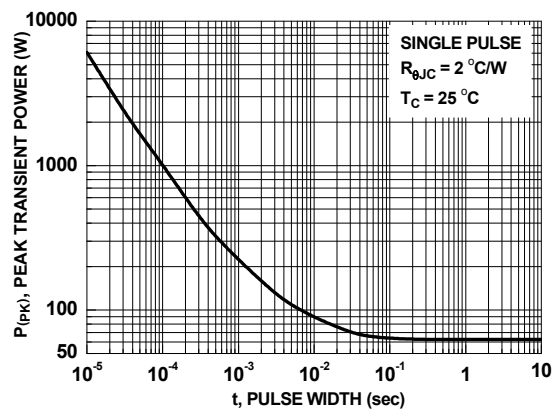


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

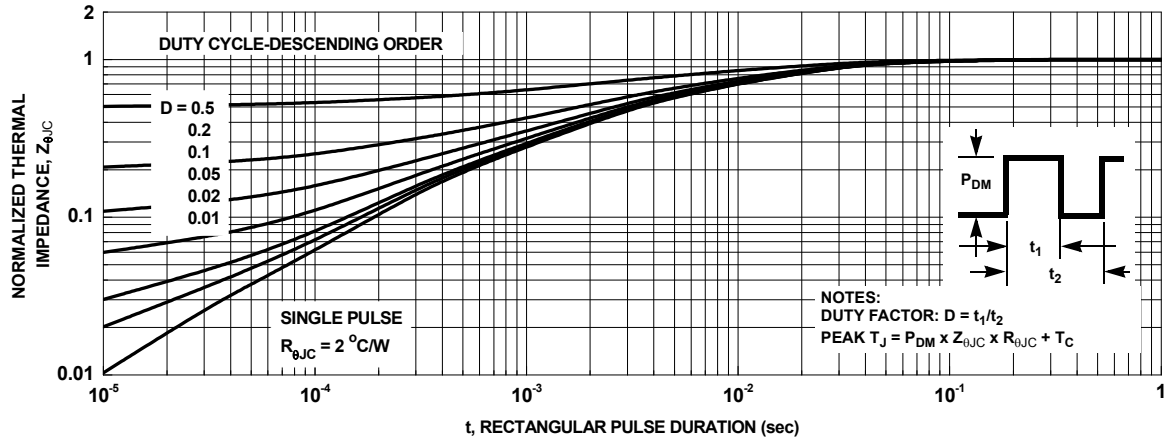


Figure 13. Junction-to-Case Transient Thermal Response Curve



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.

E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS

F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.

G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.

H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



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