N-Channel 40-V (D-S) Temperature Sensing MOSFET

CHARACTERISTICS

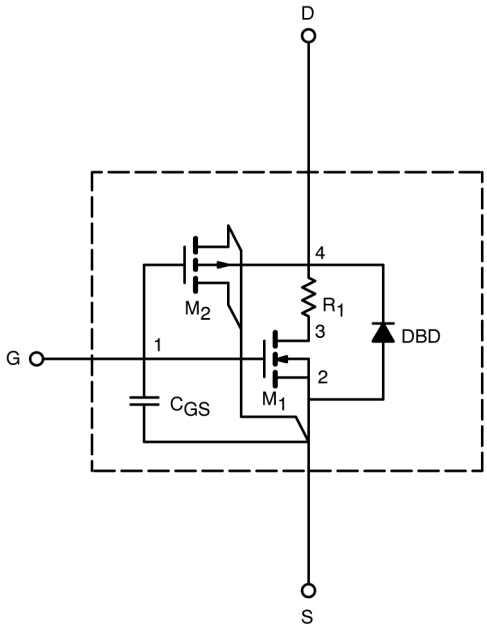
- N-Channel Vertical DMOS
- Macro Model (Model Subcircuit Schematic)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model schematic is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-to-5V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)				
Parameter	**Symbol**	**Test Conditions**	**Typical**	**Unit**
Static				
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 µA	1.	V
Zero Gate Voltage Drain Current	I_{Dss}	V_{DS} = 35 V, V_{GS} = 0 V	0.001	µA
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A	0.008	Ω
		V_{GS} = 4.5 V, I_D = 20 A	0.012	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 20 A	36	S
Diode Forward Voltage[a]	V_{SD}	I_F = I_S = 1.25 A, V_{GS} = 0 V	0.91	V
Dynamic				
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1865	pf
Output Capacitance	C_{oss}		564	
Reverse Transfer Capacitance	C_{rss}		180	
Total Gate Charge[b]	Q_g	V_{DS} = 20 V, V_{GS} = 10 V, I_D = 25 A	43	nC
Gate-Source Charge[b]	Q_{gs}		6	
Gate-Drain Charge[b]	Q_{gd}		11	
Turn-On Delay Time[b, c]	$t_{d(on)}$	V_{DD} = 20 V, R_L = 0.8 Ω I_D ≅ 25 A, V_{GEN} = 10 V, R_G = 2.5 Ω	11.5	ns
Rise Time[b, c]	t_r		12.6	
Turn-Off Delay Time[b, c]	$t_{d(off)}$		37	
Fall Time[b, c]	t_f		9.5	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = A, di/dt = 100 A/µs		

Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Independent of operating temperature.
c. Include only parasitic components presented in the model circuit

COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)