



MC34050 MC34051

Dual EIA-422/423 Transceivers

The MC34050/51 are dual transceivers which comply with EIA Standards EIA-422 (Balanced line) and EIA-423 (Unbalanced line). Each device contains two drivers and two receivers.

The MC34050 has a DRIVER ENABLE (for both drivers) and a RECEIVER ENABLE (for both receivers). Connecting the two ENABLES together provides Driver-to-Receiver switching from a single line.

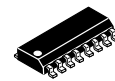
The MC34051 has a DRIVER ENABLE for each driver. The two receivers are permanently enabled.

The Driver inputs, Receiver outputs, and Enable inputs are 74LS TTL compatible.

- Two Independent Drivers and Receivers Per Package
- 3-State Outputs
- Single 5.0 V Supply
- Internal Hysteresis (50 mV Typical) on Receivers
- Receivers Provide Fail-Safe Function. Output Stays High if Inputs are Open, Shorted (floating), or Terminated (floating)
- Receivers May Be Used in EIA-422 or 423 Systems
- Drivers Meet Full EIA-422 Standards

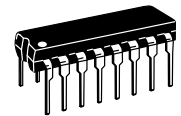
DUAL EIA-422/423 TRANSCEIVERS

SEMICONDUCTOR TECHNICAL DATA

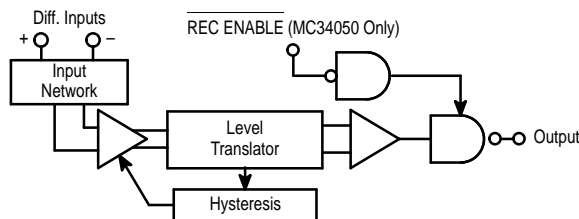


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

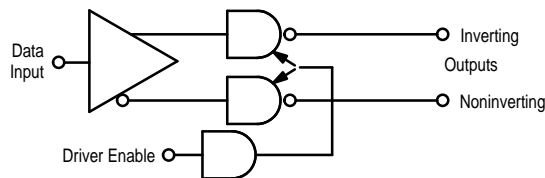
P SUFFIX
PLASTIC PACKAGE
CASE 648



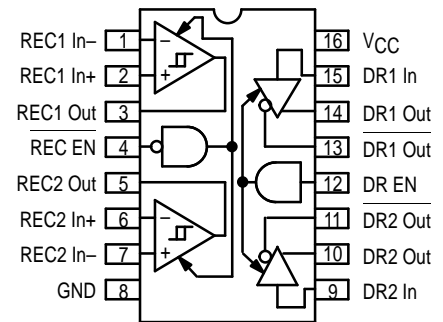
Receiver Block Diagram



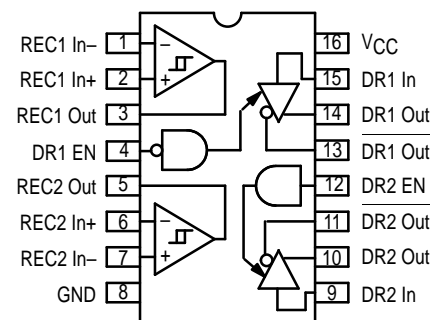
Driver Block Diagram



PIN CONNECTIONS



(MC34050)



(MC34051)

TRUTH TABLE

| Driver | | | | Receiver | | |
|--------|----|----------|-------------|-----------------|----|--------|
| Data | EN | Inv. Out | Noninv. Out | Input | EN | Output |
| L | H | H | L | > + 0.2 V Diff. | L | H |
| H | H | L | H | < - 0.2 V Diff. | L | L |
| X | L | Z | Z | X | H | Z |

ORDERING INFORMATION

| Device | Operating Temperature Range | Package |
|----------|--|-------------|
| MC34050D | $T_A = 0^\circ \text{ to } +70^\circ \text{C}$ | SO-16 |
| MC34050P | | Plastic DIP |
| MC34051P | | Plastic DIP |
| MC34051D | | SO-16 |

MC34050 MC34051

MAXIMUM RATINGS

| Rating | Value | Units |
|---|--------------|--------------------|
| Power Supply Voltage (V_{CC}) | 7.0 | Vdc |
| Input Common Mode Voltage (Receivers) | ± 25 | Vdc |
| Input Differential Voltage (Receivers) | ± 25 | Vdc |
| Output Sink Current (Receivers) | 50 | mA |
| Enable Input Voltage (Drivers and Receivers) | 5.5 | Vdc |
| Input Voltage (Drivers) | 5.5 | Vdc |
| Applied Output Voltage (3-State mode) – Receivers | -1.0 to +7.0 | Vdc |
| Applied Output Voltage (3-State mode) – Drivers | -1.0 to +7.0 | Vdc |
| Junction Temperature | -65 to +150 | $^{\circ}\text{C}$ |
| Storage Temperature | -65 to +150 | $^{\circ}\text{C}$ |

Devices should not be operated at these values.
The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

| Characteristic | Min | Typ | Max | Unit |
|--|-------|------|-------|--------------------|
| Power Supply Voltage | +4.75 | +5.0 | +5.25 | Vdc |
| Input Common Mode Voltage (Receivers) | -7.0 | - | +7.0 | Vdc |
| Input Differential Voltage (Receivers) | -6.0 | - | +6.0 | Vdc |
| Enable Input Voltage (Drivers and Receivers) | 0 | - | +5.25 | Vdc |
| Input Voltage (Drivers) | 0 | - | +5.25 | Vdc |
| Ambient Temperature Range | 0 | - | +70 | $^{\circ}\text{C}$ |

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for $4.75 < V_{CC} < 5.25$ V, and $0^{\circ} < T_A < 70^{\circ}\text{C}$).

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|--------------|--------------|--------|--------------|---------------|
| DRIVERS | | | | | |
| Input Voltage – Low | V_{ILD} | - | - | 0.8 | Vdc |
| Input Voltage – High | V_{IHD} | 2.0 | - | - | Vdc |
| Input Current @ $V_{IL} = 0.4$ V | I_{ILD} | -360 | - | - | μA |
| Input Current @ $V_{IH} = 2.7$ V $V_{IH} = 5.25$ V | I_{IHD} | - | - | +20 +100 | μA |
| Input Clamp Voltage ($I_{IK} = -18$ mA) | V_{IKD} | -1.5 | - | - | Vdc |
| Output Voltage – Low ($I_{OL} = 20$ mA) | V_{OLD} | - | - | 0.5 | Vdc |
| Output Voltage – High ($I_{OH} = -20$ mA) | V_{OHD} | 2.5 | - | - | Vdc |
| Output Offset Voltage Difference (Note 1) | V_{OSD} | -0.4 | - | +0.4 | Vdc |
| Output Differential Voltage (Note 1) | V_T | 2.0 | - | - | Vdc |
| Output Differential Voltage Difference (Note 1) | V_{TD} | -0.4 | - | +0.4 | Vdc |
| Short Circuit Current ($V_{CC} = 5.25$ V) (From High Output, Note 2) | I_{OSD} | -150 | - | -30 | mA |
| Output Leakage Current – Hi-Z State ($V_{out} = 0.5$ V, DR EN = 0.8 V) ($V_{out} = 2.7$ V, DR EN = 0.8 V) | I_{OZD} | -100 -100 | - - | +100 +100 | μA |
| Output Leakage – Power Off ($V_{out} = -0.25$ V, $V_{CC} = 0$ V) ($V_{out} = 6.0$ V, $V_{CC} = 0$ V) | $I_{O(off)}$ | -100 - | - - | - +100 | μA |

NOTES: 1. See EIA Standard EIA-422 and Figure 1 for exact test conditions.
2. Only one output in a package should be shorted at a time, for no longer than 1 second.

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ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for $4.75 < V_{CC} < 5.25$ V, and $0^\circ < T_A < 70^\circ$ C).

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|------------------------|--------------|--------|--------------|---------|
| RECEIVERS | | | | | |
| Differential Input Threshold Voltage (Note 3) (-7.0 V $< V_{ICM} < 7.0$, $V_{out} \geq 2.7$ V) (-7.0 V $< V_{ICM} < 7.0$, $V_{out} \leq 0.45$ V) | V_{THR} | – –0.2 | – – | +0.2 – | Vdc |
| Input Bias Current ($0 \leq V_{CC} \leq 5.25$ V, $V_{in} = 15$ V) ($0 \leq V_{CC} \leq 5.25$ V, $V_{in} = -15$ V) | I_{IBR} | – –2.8 | – – | +2.3 – | mA |
| Input Balance and Output Level ($-7.0 \leq V_{ICM} \leq 7.0$ V) ($V_{ID} = 0.4$ V, $I_O = -400$ μ A) ($V_{ID} = -0.4$ V, $I_O = 8.0$ mA) | V_{OHR} V_{OLR} | 2.7 – | – – | – 0.45 | Vdc |
| Output Leakage Current – 3-State (Pin 4 = 2.0 V, MC34050 only) ($V_{ID} = 3.0$ V, $V_O = 0.4$ V) ($V_{ID} = -3.0$ V, $V_O = 2.4$ V) | I_{OZR} | –100 –100 | – – | +100 +100 | μ A |
| Output Short Circuit Current (Note 2, $V_{CC} = 5.25$ V) ($V_{ID} = 3.0$ V, MC34050 Pin 4 = 0.4 V, $V_O = 0$ V) | I_{OSR} | –85 | – | –15 | mA |

ENABLES

| | | | | | |
|---|--------------------------|--------------|--------|-------------|---------|
| Input Voltage – Low | V_{ILE} | – | – | 0.8 | Vdc |
| Input Voltage – High | V_{IHE} | 2.0 | – | – | Vdc |
| Input Current @ $V_{IL} = 0.4$ V (Receiver EN) (Driver EN) | I_{ILER} I_{ILED} | –100 –360 | – – | – – | μ A |
| Input Current @ $V_{IH} = 2.7$ V $V_{IH} = 5.25$ V | I_{IHE} | – – | – – | +20 +100 | μ A |
| Input Clamp Voltage ($I_{IK} = -18$ mA) | V_{IKE} | –1.5 | – | – | Vdc |

POWER SUPPLY

| | | | | | |
|--|----------|---|----|----|----|
| Power Supply Current @ $V_{CC} = 5.25$ V | I_{CC} | – | 55 | 80 | mA |
|--|----------|---|----|----|----|

NOTES: 2. Only one output in a package should be shorted at a time, for no longer than 1 second.
3. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.

DRIVER SWITCHING CHARACTERISTICS ($V_{CC} = 5.0$ V, $T_A = 25^\circ$ C, see Figure 2).

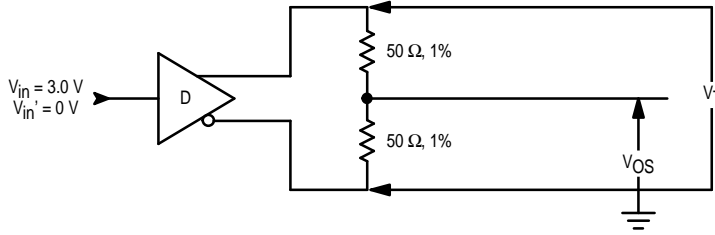
| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|------------|-----|-----|-----|------|
| Propagation Delay | | | | | ns |
| Data Input to Output High-to-Low | t_{PHLD} | – | – | 20 | |
| Data Input to Output Low-to-High | t_{PLHD} | – | – | 20 | |
| Output Skew ($ t_{PHL} - t_{PLH} $ each driver) | t_{SKD} | – | – | 8 | |
| Enable Input to Output | | | | | |
| $C_L = 10$ pF, $R_L = 75$ Ω to Gnd | t_{PHZD} | – | – | 30 | |
| $C_L = 10$ pF, $R_L = 180$ Ω to V_{CC} | t_{PLZD} | – | – | 35 | |
| $C_L = 30$ pF, $R_L = 75$ Ω to Gnd | t_{PZHD} | – | – | 40 | |
| $C_L = 30$ pF, $R_L = 180$ Ω to V_{CC} | t_{PZLD} | – | – | 45 | |
| Maximum Data Input Transition Time (10% to 90%) | t_{TRD} | – | 50 | – | ns |

RECEIVER SWITCHING CHARACTERISTICS ($V_{CC} = 5.0$ V, $T_A = 25^\circ$ C, see Figure 3).

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|------------|-----|-----|-----|------|
| Propagation Delay | | | | | ns |
| Differential Input to Output – High-to-Low | t_{PHLR} | – | – | 30 | |
| Differential Input to Output – Low-to-High | t_{PLHR} | – | – | 30 | |
| Enable Input – Output Low to 3-State | t_{PLZR} | – | – | 35 | |
| Enable Input – Output High to 3-State | t_{PHZR} | – | – | 35 | |
| Enable Input – Output 3-State to High | t_{PZHR} | – | – | 30 | |
| Enable Input – Output 3-State to Low | t_{PZLR} | – | – | 30 | |

} MC34050 Only

Figure 1. Driver Output Test Circuit

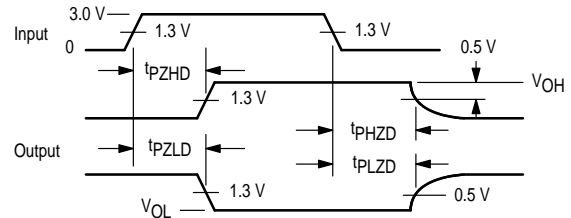
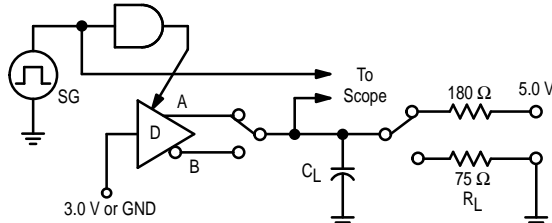
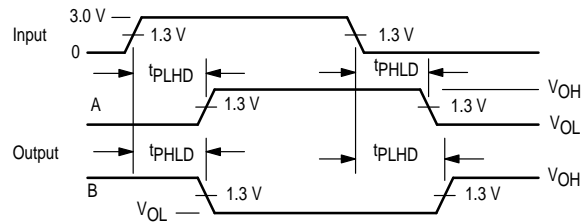
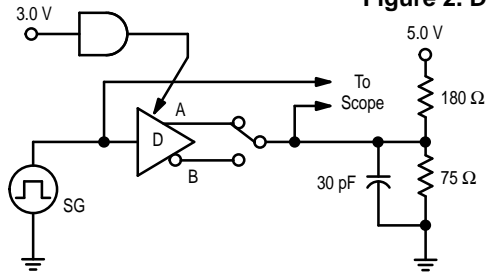


$$V_{OSD} = |V_{OS} - V_{OS}'|;$$

$$V_{ODD} = ||V_T| - |V_T'|$$

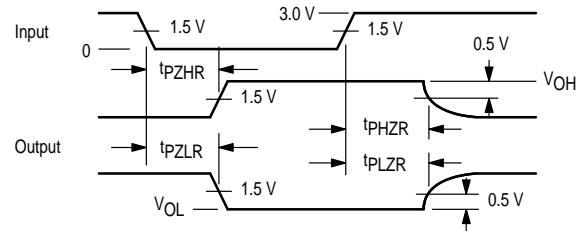
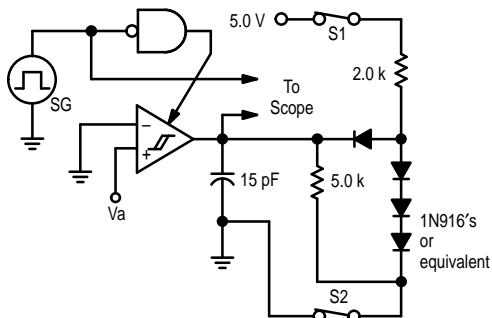
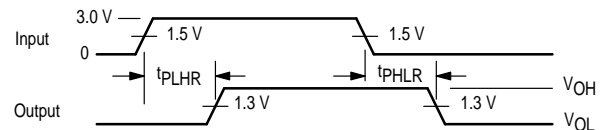
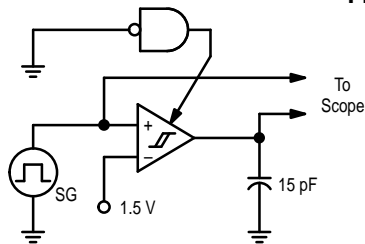
Circuit per EIA-422-A, Dec. 1978

Figure 2. Driver Switching Test Circuits



SG: 1.0 MHz, 50% duty cycle, $t_R, t_F = 6.0$ ns (10% to 90%)
 $R_L = 75 \Omega$ to GND for $t_{PZH D}$ and $t_{PHZ D}$; 180Ω to V_{CC} for $t_{PZL D}$ and $t_{PHL D}$;
 $C_L = 10$ pF for $t_{PHZ D}$ and $t_{PZL D}$; 30 pF for $t_{PZH D}$ and $t_{PZL D}$.

Figure 3. Receiver Switching Test Circuits



MC34050 Only

SG: 1.0 MHz, 50% duty cycle, $t_R, t_F = 6.0$ ns (10% to 90%)
 $V_a = +1.5$ V for t_{PHZ} , t_{PZH} ; $V_a = -1.5$ V for t_{PLZ} , t_{PL} .
 S_1, S_2 closed for t_{PHZ} , t_{PLZ} ; S_1 open, S_2 closed for t_{PZH} ; S_1 closed, S_2 open for t_{PL} .

Figure 4. Driver Input Characteristics

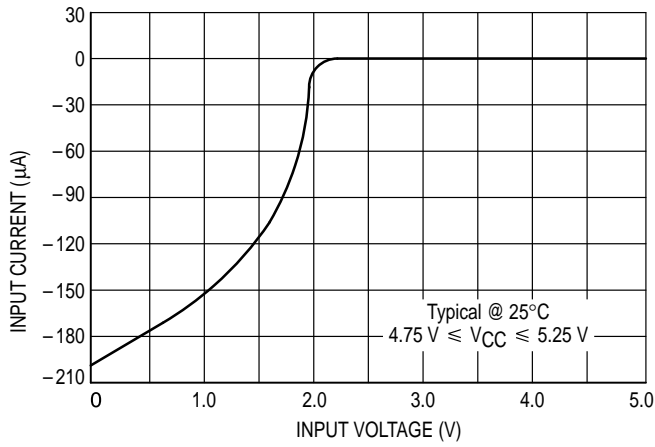


Figure 5. Driver Differential Output Characteristics

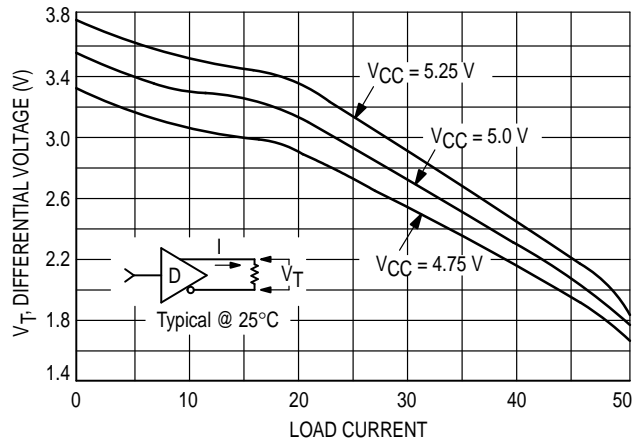


Figure 6. Driver Output Voltage

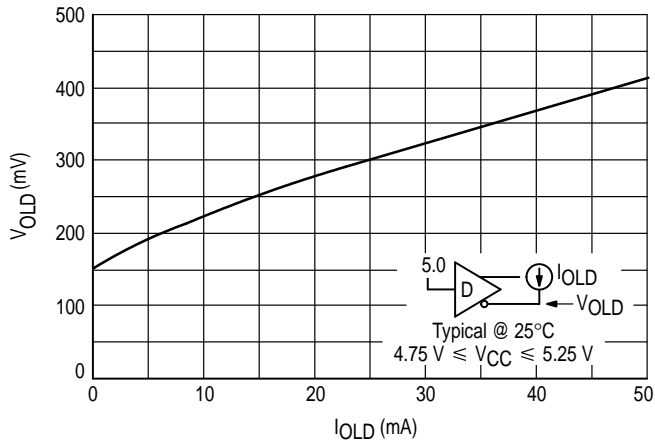


Figure 7. Driver Output Voltage

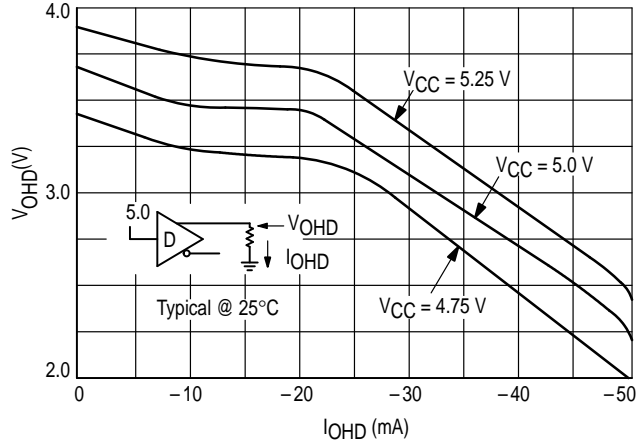


Figure 8. Receiver Output Voltage

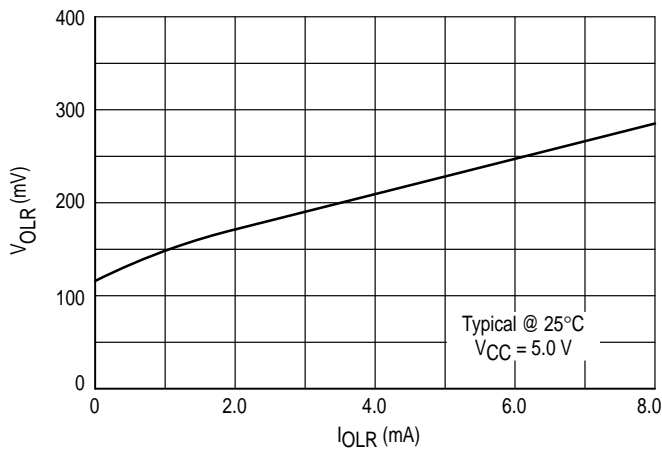


Figure 9. Receiver Output Voltage

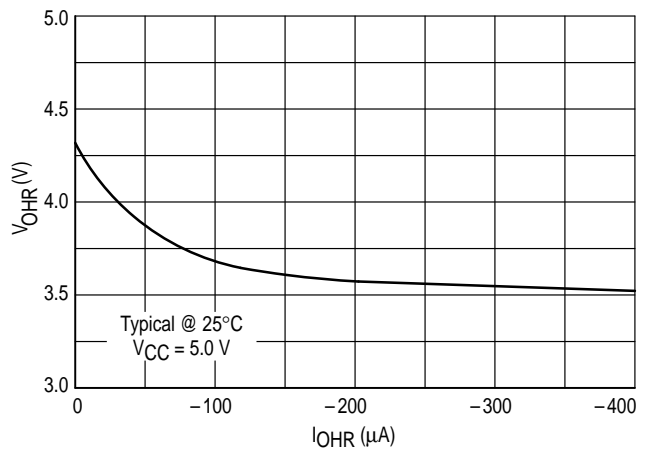


Figure 10. Receiver Input Characteristics

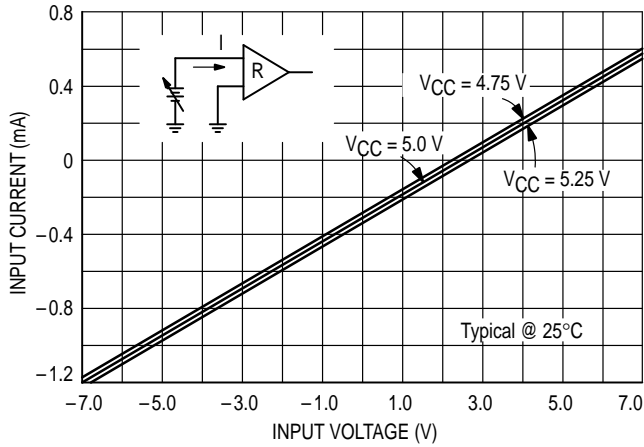


Figure 11. Enable Input Characteristics

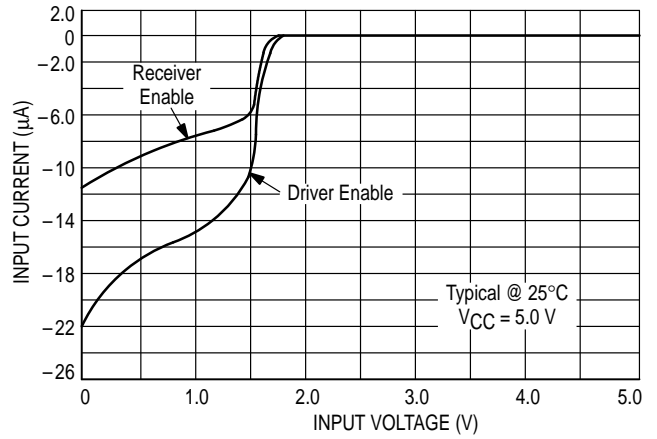


Figure 12. Receiver Input Characteristics

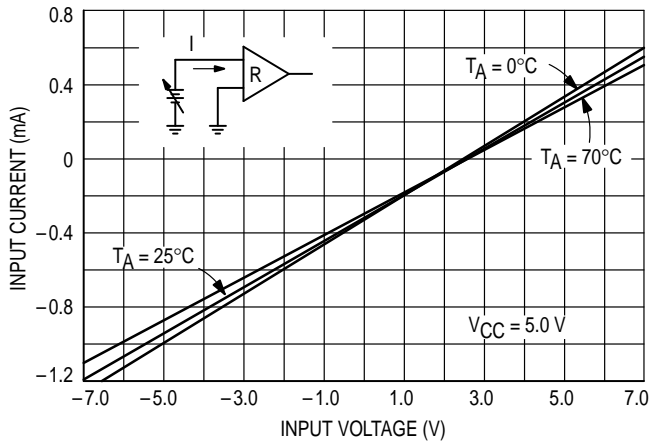


Figure 13. Receiver Output Leakage

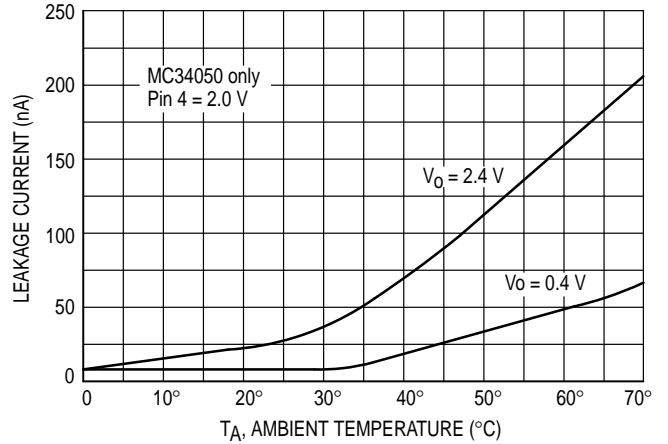


Figure 14. Driver Output Voltage

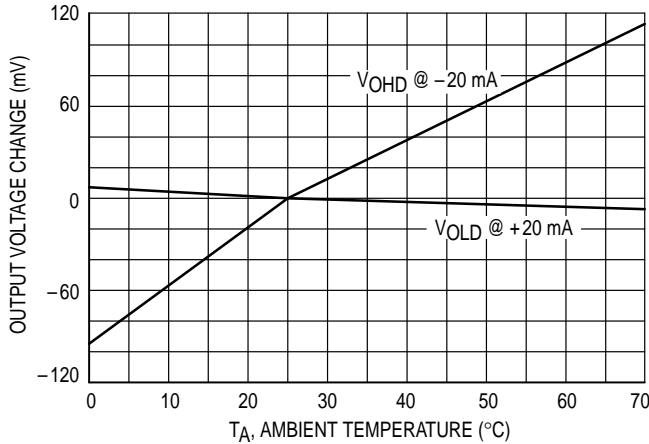
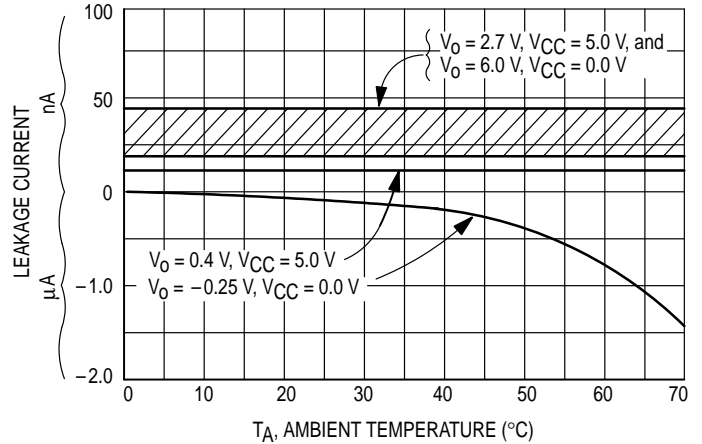


Figure 15. Driver Output Leakage



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Figure 16. EIA-422 Application

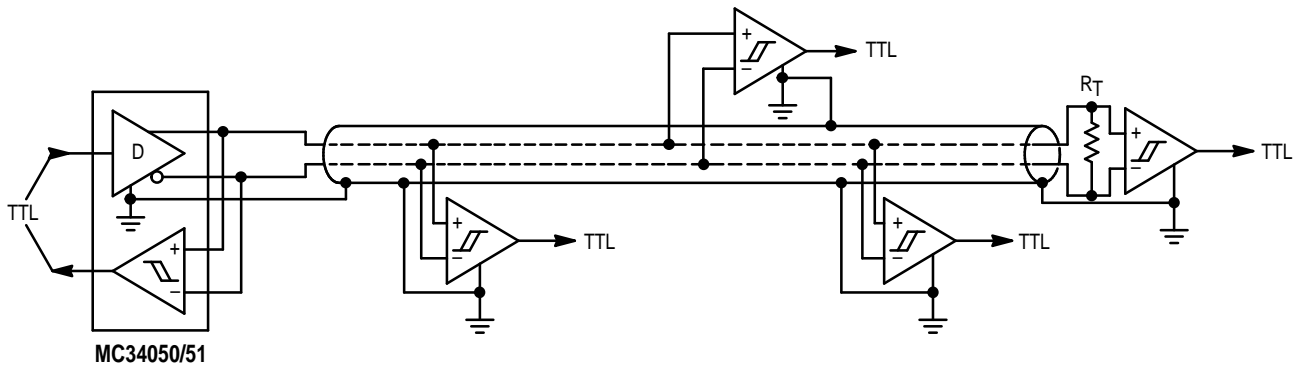
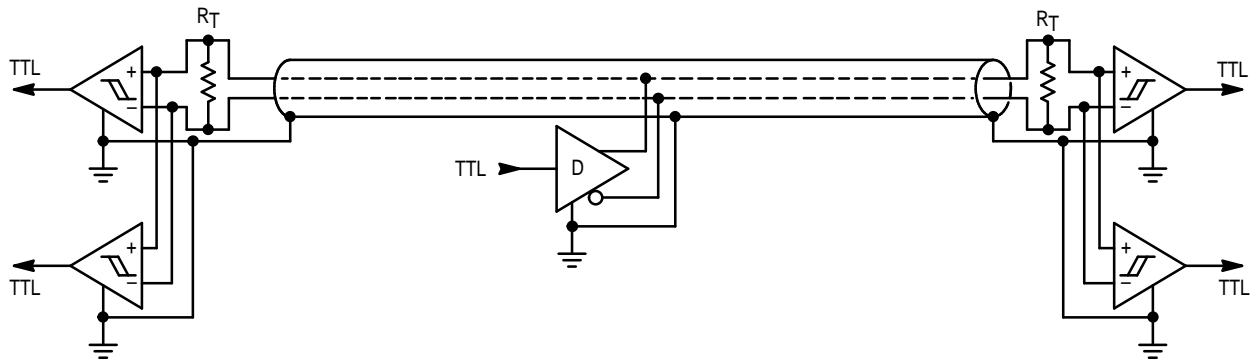


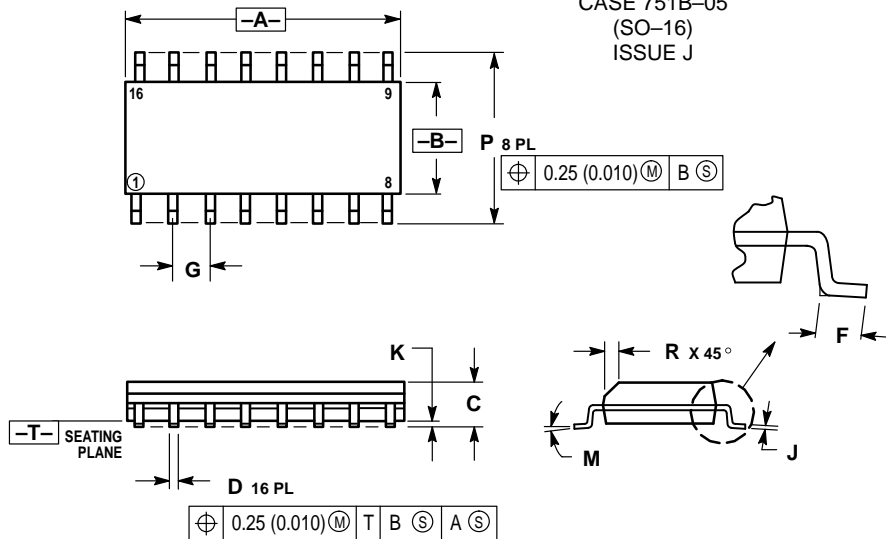
Figure 17. EIA-423 Application



MC34050 MC34051

OUTLINE DIMENSIONS

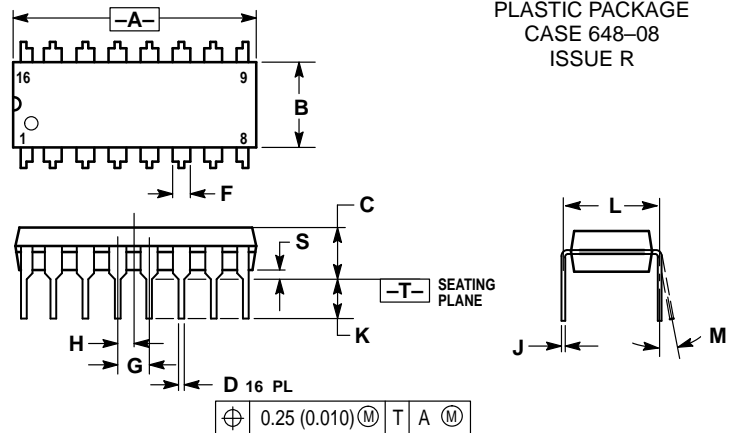
D SUFFIX PLASTIC PACKAGE CASE 751B-05 (SO-16) ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

P SUFFIX PLASTIC PACKAGE CASE 648-08 ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

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