# Burst Triple Mode PWM Controller with Integrated HV Start-up Device for Zero Power Monitor Application

## General Description

The R7780 is a high-performance current mode PWM controller with integrated HV start-up device inside. During start-up, a current source through integrated HV device to charge VDD capacitor for quick start-up while it dissipates no loss in normal operation.

The R7780 provides the users a superior AC/DC power application of higher efficiency, few external component counts, and low cost solution. It features frequency jitter, Under Voltage LockOut (UVLO), Leading Edge Blanking (LEB), internal slope compensation in the tiny SOP-7 package. It offers complete protection coverage with Over Temperature Protection (OTP), Over Load Protection (OLP) and Over Voltage Protection (OVP).

Moreover, it also provides a special interface for zero power application when the converter is in sleeping mode. EN/DIS pin receives ON/OFF signal from secondary scalar controller. During turning off, the controller will be shutdown completely with pretty low power consumption.

## Ordering Information

R7780 □□

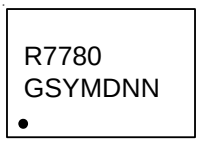
- Package Type
  S : SOP-7
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

## Marking Information




R7780GS : Product Number

YMDNN : Date Code

## Features

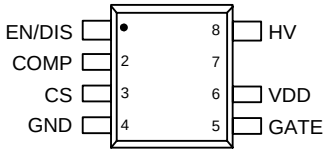
- **Integrated HV Start-up Device**
- **Enable/Disable Function**
- **UVLO: 9V/16.5V**
- **Current Mode Control**
- **Built-in 65kHz Operation Frequency**
- **Built-in Jittering Frequency**
- **Internal PWM Leading Edge Blanking**
- **Internal Slope Compensation**
- **Compensated Burst Triple Mode PWM**
- **Cycle-by-Cycle Current Limit**
- **Internal Auto Recovery OVP**
- **Internal Auto Recovery OLP**
- **Internal Auto Recovery OTP**
- **CS Pin Open Protection**
- **Secondary Rectifier Short Protection**
- **Soft Driving for Reducing EMI Noise**
- **High Noise Immunity**
- **RoHS Compliant and Halogen Free**

## Applications

- **Switching AC/DC Adaptor**
- **TV and Monitor Application**
- **Low Standby Power Home Appliance**

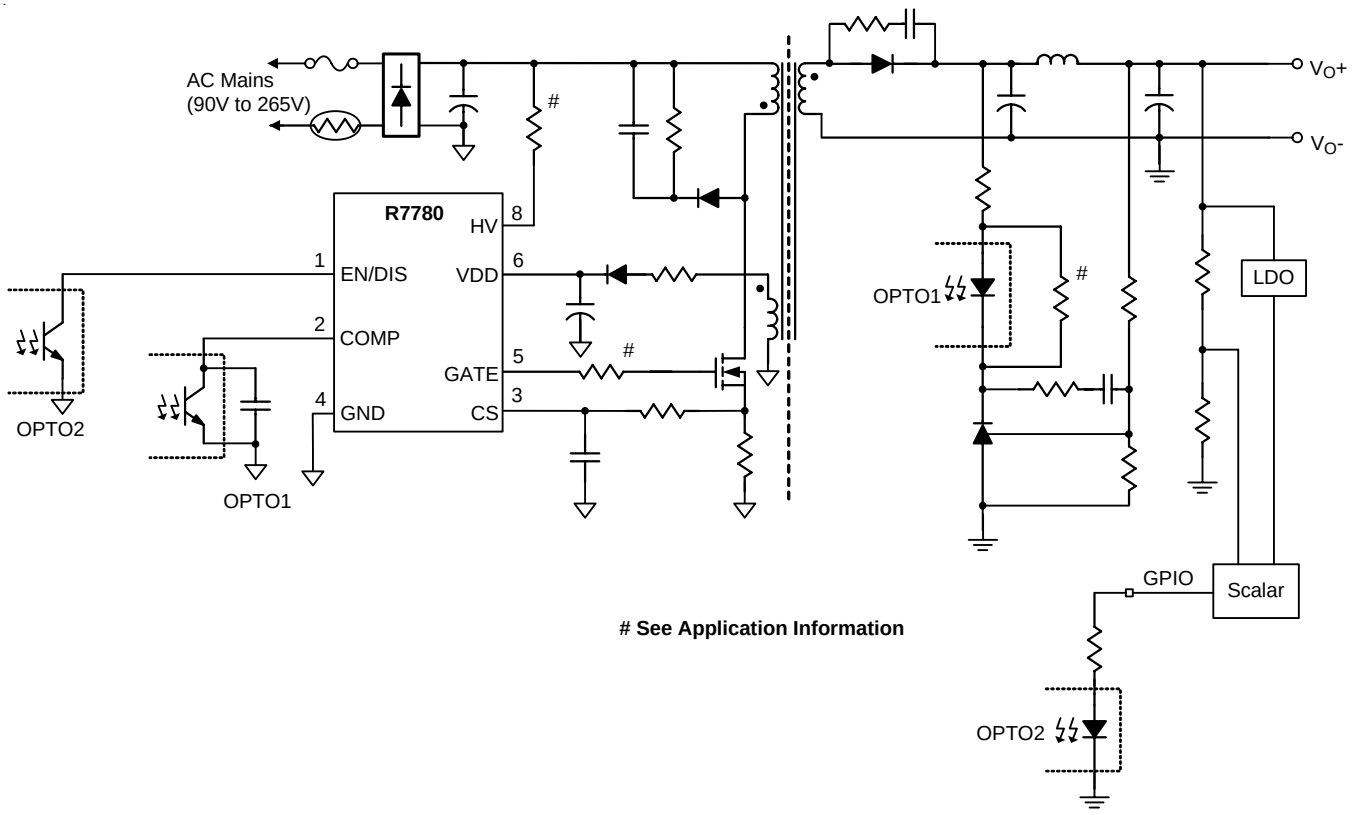
## Pin Configurations

(TOP VIEW)




SOP-7

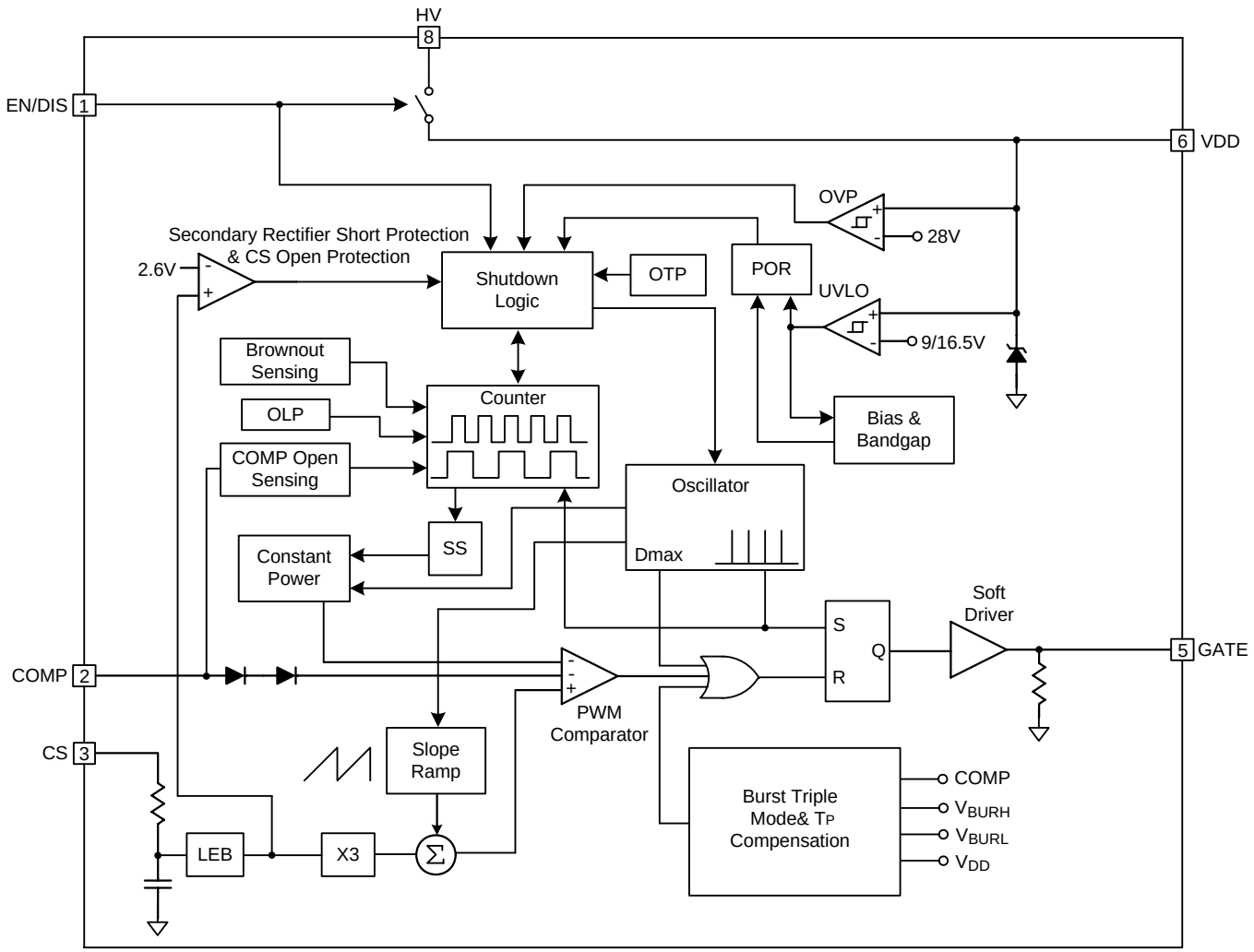
## Typical Application Circuit




## Functional Pin Description

| Pin No. | Pin Name | Pin Description |
|---|---|---|
| 1 | EN/DIS | Enable/Disable Function. |
| 2 | COMP | Voltage Feedback. By connecting an opto-coupler to close control loop and achieve the regulation. |
| 3 | CS | Current Sensing. |
| 4 | GND | Ground. |
| 5 | GATE | Gate Drive Output to Drive the External MOSFET. |
| 6 | VDD | Power Supply Pin. |
| 7 | NC | No Internal Connection. |
| 8 | HV | 700V High Voltage Device for Start-up. |

## Function Block Diagram



## Absolute Maximum Ratings (Note 1)

- HV Pin ---------- –0.3V to 700V
- Supply Input Voltage, $V_{DD}$ ---------- –0.3V to 30V
- GATE Pin ---------- –0.3V to 20V
- EN/DIS, COMP, CS Pin ---------- –0.3V to 6.5V
- Power Dissipation, $P_D$ @ $T_A$ = 85°C
  SOP-7 ---------- 0.625W
- Package Thermal Resistance (Note 2)
  SOP-7, $\theta_{JA}$ ---------- 160°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  Human Body Mode (Except HV pin) ---------- 6kV
  Machine Mode ---------- 200V

## Recommended Operating Conditions (Note 4)

- Supply Input Voltage, $V_{DD}$ ---------- 12V to 25V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

## Electrical Characteristics

($V_{DD}$ = 15V, $T_A$ = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **HV Section** | | | | | | |
| HV Start-up Current | $I_{JEFT\_ST}$ | $V_{DD} < V_{TH\_ON}$ , HV = 500V | 1 | -- | -- | mA |
| Off State Leakage Current | | $V_{DD} = V_{TH\_OFF}$, HV = 500V | -- | -- | 25 | μA |
| **VDD Section** | | | | | | |
| On Threshold Voltage | $V_{TH\_ON}$ | | 15.5 | 16.5 | 17.5 | V |
| Off Threshold Voltage | $V_{TH\_OFF}$ | | 8 | 9 | 10 | V |
| $V_{DD}$ Zener Clamp Voltage | $V_Z$ | | 30 | -- | -- | V |
| Operating Current | $I_{DD\_OP}$ | $V_{DD}$ = 15V, 65kHz<br>COMP pin , GATE pin open | -- | 550 | 1000 | μA |
| VDD Holdup Mode End Point | $V_{DD\_HIGH}$ | $V_{COMP}$ < 1.6V | -- | 10.5 | -- | V |
| VDD Holdup Mode Entry Point | $V_{DD\_LOW}$ | $V_{COMP}$ < 1.6V | -- | 10 | -- | V |
| $V_{DD}$ Over Voltage Protection Level | $V_{OVP}$ | | 27 | 28 | 29 | V |

*To be continued*

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Oscillator Section** | | | | | | |
| Normal PWM Frequency | $f_{OSC}$ | | 60 | 65 | 70 | kHz |
| Maximum Duty Cycle | $D_{MAX}$ | | 70 | 75 | 80 | % |
| PWM Frequency Jitter Range | $\Delta f$ | | -- | ±7 | -- | % |
| PWM Frequency Jitter Period | $T_{JIT}$ | For 65kHz | -- | 4 | -- | ms |
| Frequency Variation Versus $V_{DD}$ | $f_{DV}$ | $V_{DD}$ = 12V to 25V | -- | -- | 2 | % |
| Frequency Variation Versus Temperature | $f_{DT}$ | $T_A$ = –30°C to 105°C (Note 5) | -- | -- | 5 | % |
| **COMP Input Section** | | | | | | |
| Open-Loop Voltage | $V_{COMP\_OP}$ | COMP pin open | 5.5 | 5.75 | 6 | V |
| COMP Open 56ms Protection | $V_{COMP\_56}$ | | 5.25 | -- | -- | V |
| COMP Open-Loop Protection Delay Time | $t_{OLP}$ | | -- | 56 | -- | ms |
| Short Circuit COMP Current | $I_{ZERO}$ | $V_{COMP}$ = 0V | -- | 272 | 400 | μA |
| **Current-Sense Section** | | | | | | |
| Initial Current Limit Offset | $V_{CSTH}$ | | 0.67 | 0.7 | 0.73 | V |
| Leading Edge Blanking Time | $t_{LEB}$ | (Note 6) | 150 | 250 | 350 | ns |
| Internal Propagation Delay Time | $t_{PD}$ | (Note 6) | -- | 100 | -- | ns |
| Minimum On Time | $t_{ON\ (MIN)}$ | | 250 | 350 | 450 | ns |
| **GATE Section** | | | | | | |
| Gate Output Clamping Voltage | $V_{CLAMP}$ | $V_{DD}$ = 25V | -- | 14 | -- | V |
| Rising Time | $t_R$ | $V_{DD}$ = 15V, $C_L$ = 1nF | -- | 125 | -- | ns |
| Falling Time | $t_F$ | $V_{DD}$ = 15V, $C_L$ = 1nF | -- | 45 | -- | ns |
| **EN/DIS Interface Section** | | | | | | |
| EN Threshold Voltage | $V_{EN}$ | | 0.8 | 1.05 | 1.3 | V |
| EN/DIS Pin Max Clamping Current | | | -- | -- | 30 | μA |

**Note 1.** Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

**Note 2.** $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

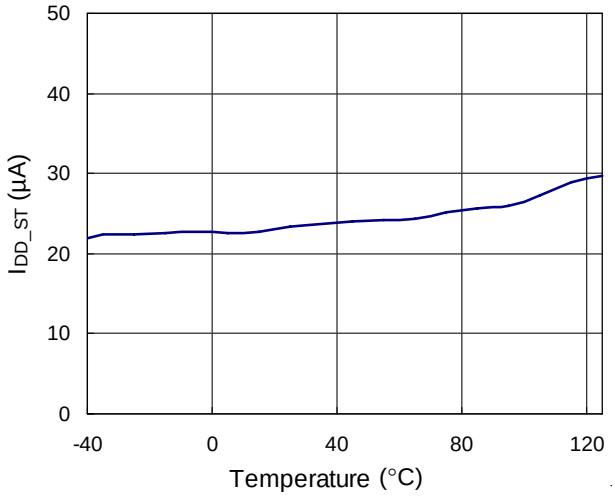
**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Note 5.** Guaranteed by design.

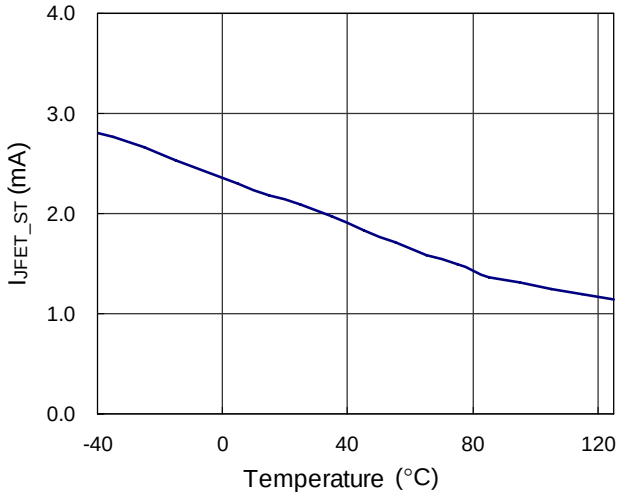
**Note 6.** Leading edge blanking time and internal propagation delay time are guaranteed by design.

## Typical Operating Characteristics

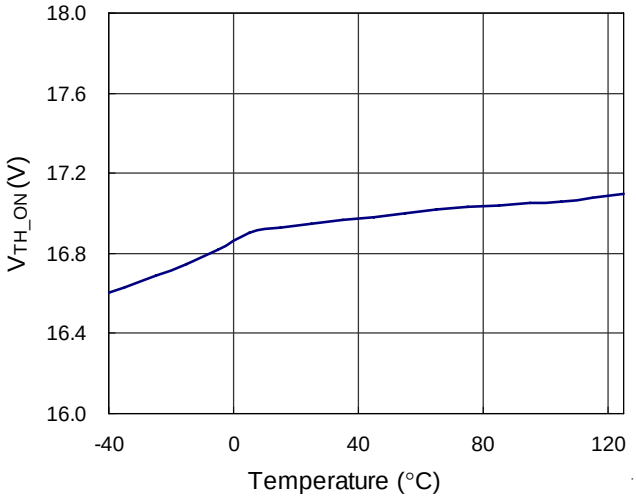
**Start-up Current ($I_{DD\_ST}$) vs. Temperature**



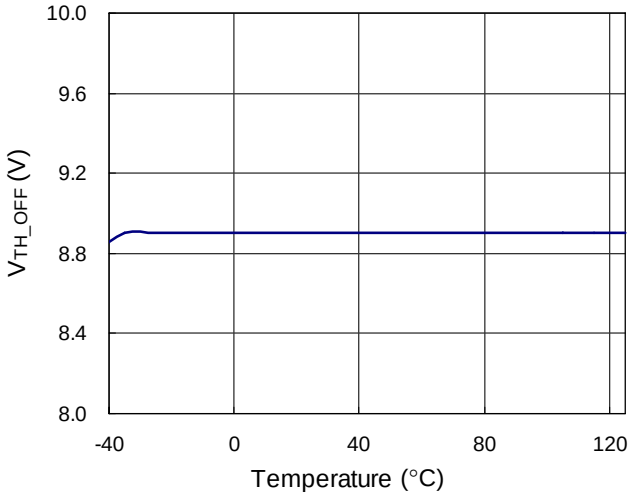

**HV Start-up Current ($I_{JFET\_ST}$) vs. Temperature**



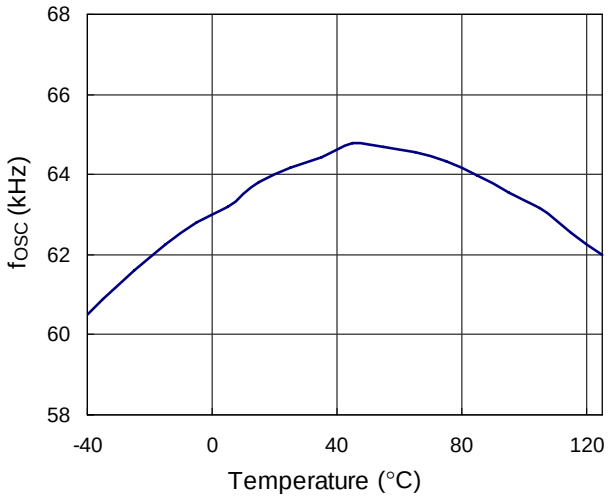

**On Threshold Voltage ($V_{TH\_ON}$) vs. Temperature**



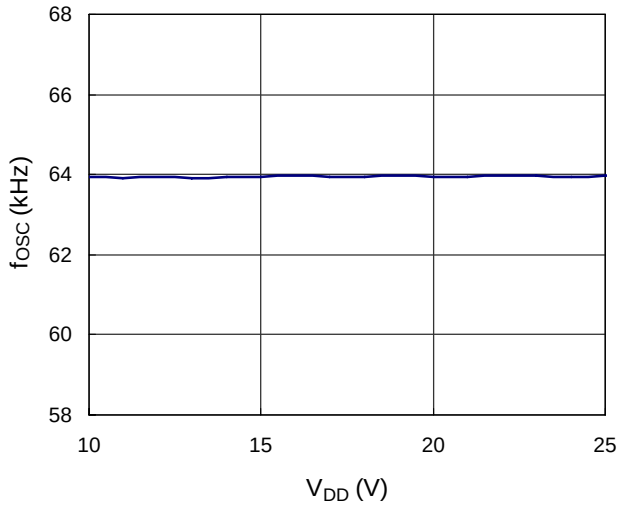

**Off Threshold Voltage ($V_{TH\_OFF}$) vs. Temperature**



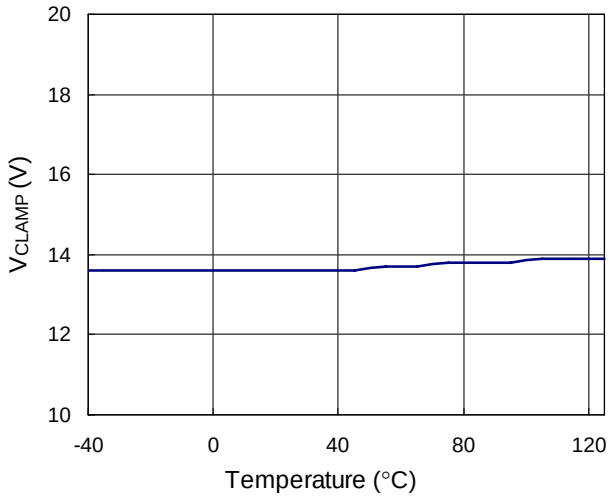

**Normal PWM Frequency ($f_{OSC}$) vs. Temperature**



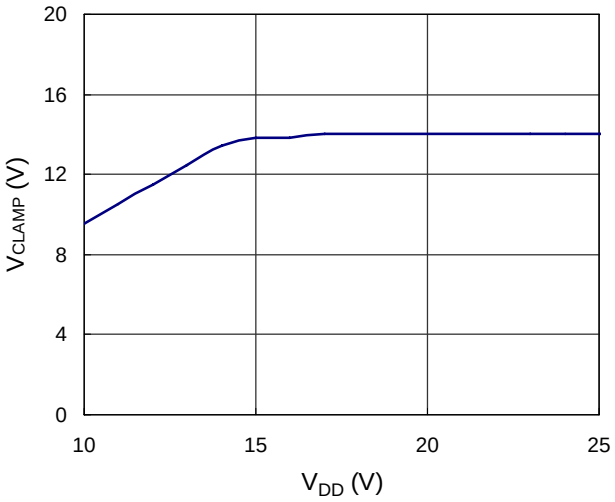

**Normal PWM Frequency ($f_{OSC}$) vs. $V_{DD}$**



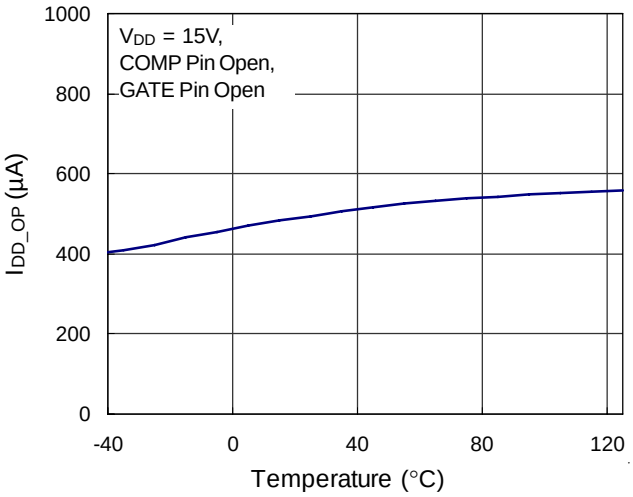
### Gate Output Clamping Voltage ($V_{CLAMP}$) vs. Temperature



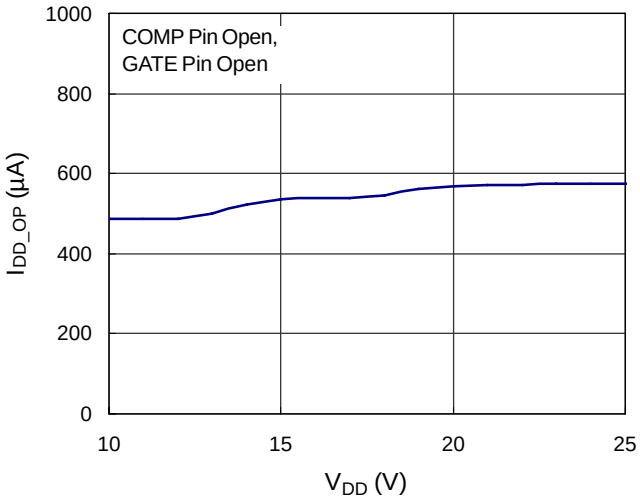

### Gate Output Clamping Voltage ($V_{CLAMP}$) vs. $V_{DD}$



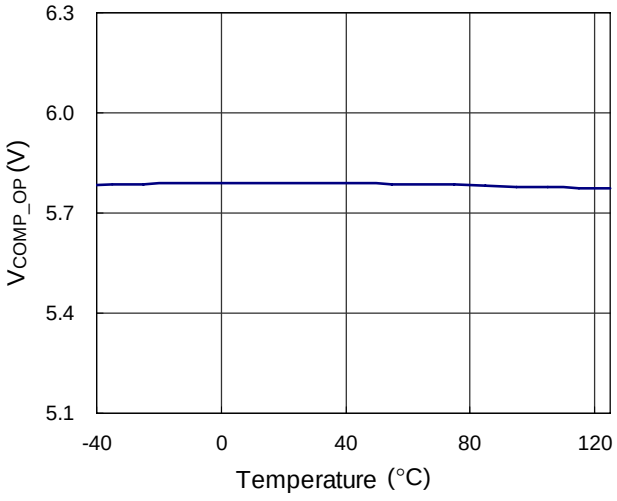

### Operating Current ($I_{DD\_OP}$) vs. Temperature



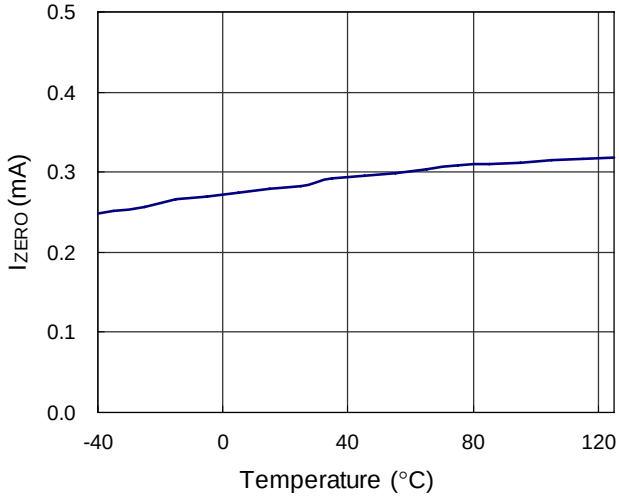

### Operating Current ($I_{DD\_OP}$) vs. $V_{DD}$



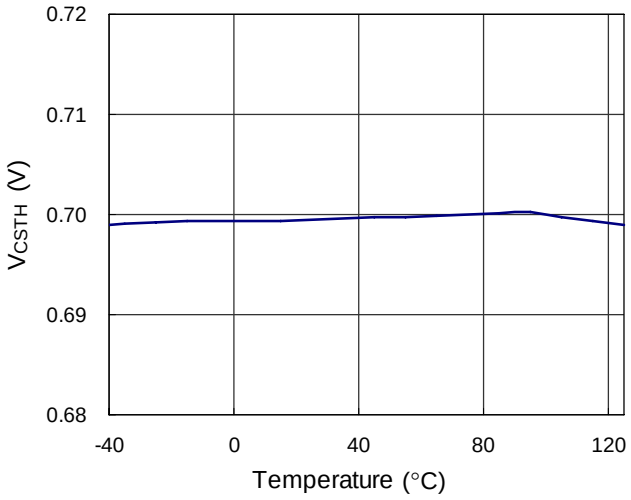

### Open-Loop Voltage ($V_{COMP\_OP}$) vs. Temperature



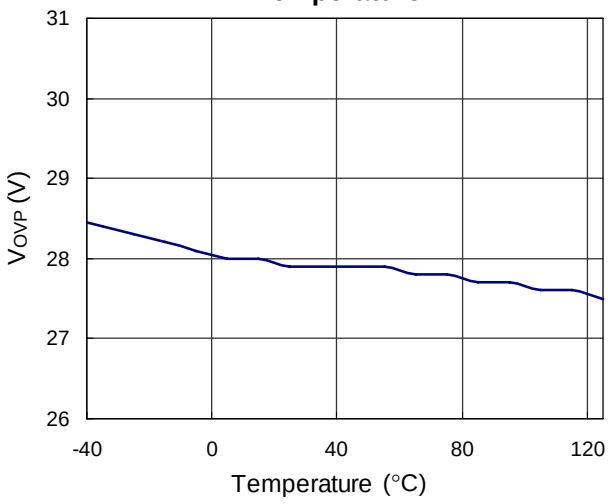

### Short Circuit COMP Current ($I_{ZERO}$) vs. Temperature



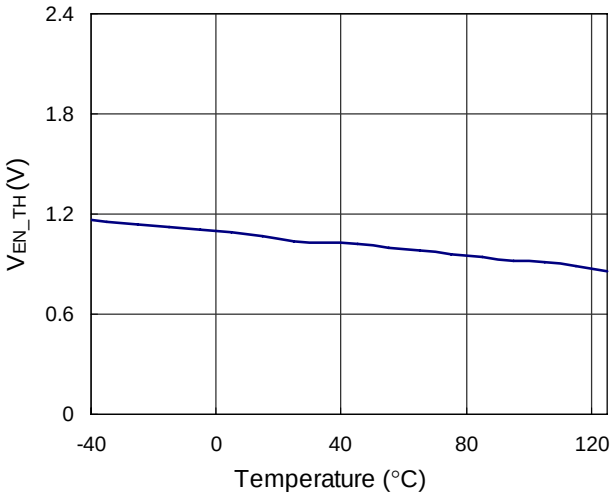
### Initial Current Limit Offset ($V_{CSTH}$) vs. Temperature



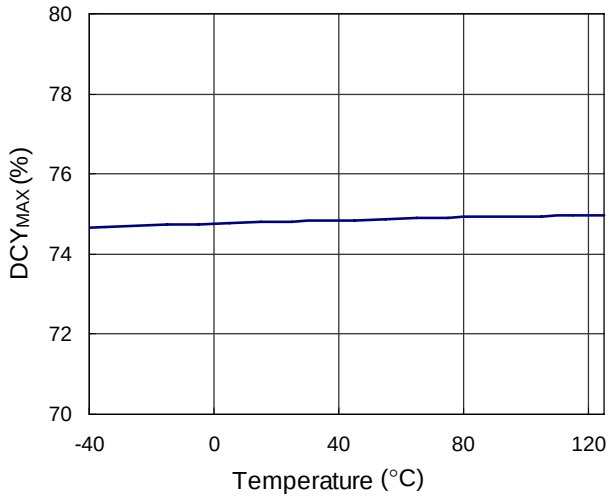

### $V_{DD}$ Over Voltage Protection Level ($V_{OVP}$) vs. Temperature




### Enable Threshold Voltage ($V_{EN\_TH}$) vs. Temperature




### Maximum Duty Cycle ($DCY_{MAX}$) vs. Temperature



## Application Information

The R7780 is specially designed for advanced monitor application. The proprietary ON/OFF control pin completely shuts down the controller after receiving downstream scalar signal from secondary side. (It achieves almost zero power under sleeping mode.)

### HV Start-up Device

An in-house design 700V start-up device is integrated in the controller to further minimized loss and enhance performance. The HV start-up device will be turned on during start-up and be pulled low during normal operation. It guarantees fast start-up time and no power loss in this path after start-up.

#A 10kΩ resistor is recommended to be connected in series with HV pin.

### Burst Triple Mode

The R7780 applies Burst Triple Mode for light load operation, because it's reliable, simple and no patent infringement issues. Refer to Figure 1 for details.

- **PWM Mode**

  For most of load, the circuit will run at traditional PWM current mode.

  #It's highly recommended to add a resistor in parallel with the photo-coupler. To provide sufficient bias current to make TL-431 regulate properly, 1.2kΩ resistor is suggested.

- **Burst Mode**

  During light load, switching loss will dominate the power efficiency calculation. This mode can reduce the switching loss. When the output load gets light, the feedback signal drops and touches $V_{BURL}$. Clock signal will be blanked and system ceases switching. After $V_{OUT}$ drops and feedback signal goes back to $V_{BURH}$, the system will restart switching again. The burst mode entry points of high and low line are compensated to reduce audio noise at high line and get better efficiency at low line. This kind of operation, is shown in the timing diagram of Figure 1.

- **VDD Holdup Mode**

  Under light load or load transient moment, feedback signal will drop and touch $V_{BURL}$. Then PWM signal will be blanked and system ceases to switch. $V_{DD}$ could drop down to turn off threshold voltage. To avoid this, when $V_{DD}$ drops to a setting threshold, 10V, the hysteresis comparator will bypass PWM and burst mode loop and force switching at a very low level to supply energy to VDD pin. VDD holdup mode is also improved to hold up $V_{DD}$ by less switching cycles. It's not likely for $V_{DD}$ to touch UVLO turn off threshold during any light load condition. This will also makes bias winding design and transient design easier.

  Furthermore, VDD holdup mode is only designed to prevent $V_{DD}$ from touching turn off threshold voltage under light load or load transient moment. Relative to burst mode, switching loss will increase on the system at VDD holdup mode, so it is highly recommended that the system should avoid operating at this mode during light load or no load condition, normally.

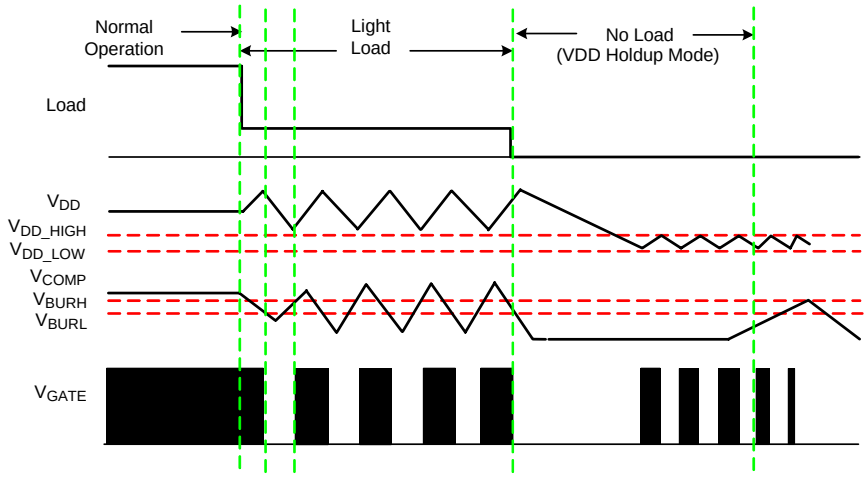



Figure 1. Burst Triple Mode

### Oscillator

To guarantee precise frequency, it is trimmed to 5% tolerance. It also generates slope compensation saw-tooth, 75% maximum duty cycle pulse and overload protection slope. It typically operates at built-in 65kHz center frequency and features frequency jittering function. Its jittering depth is 7% with about 4ms envelope frequency at 65kHz.

### Gate Driver

A totem pole gate driver is fine tuned to meet both EMI and efficiency requirement in low power application. An internal pull low circuit is activated after pretty low $V_{DD}$ to prevent external MOSFET from accidental turning-on during UVLO.

#Typical application circuits are suggested adding at least 10Ω GATE pin resistor to alleviate ringing spike of gate drive loop.

### Tight Current Limit Tolerance

Generally, the saw current limit is applied to low cost flyback controller because of simple design. However, saw current limit is hard to test in mass production. Therefore, it's generally "guarantee by design". The variation of process and package will make its tolerance wider. It will leads to 20% to 30% variation when doing OLP test at certain line voltage. This will cause yield loss in power supply mass production. Through well foundry control, design and test/trim mode in final test, the R7780 current limit tolerance is tight enough to make design and mass production easier.

### EN/DIS Pin

The R7780 features an enable/disable circuit. If the voltage on EN/DIS pin is greater than enable threshold voltage or EN/DIS pin is floating, the controller is enabled and switching will occur. If the voltage on the EN/DIS pin falls below enable threshold voltage, the controller will be shut down and consume almost zero power.

When the voltage of EN/DIS pin exceeds 1.2V or EN/DIS pin is floating, the system will be start-up. When the voltage of EN/DIS pin falls below 0.8V, the system will be shut down. For low standby power application, it's important to make current in this path as small as possible.

The deglitch delay time of the disable function is about 20μs. The internal bias current of EN/DIS is 2μA. For low power consumption, it's a high impedance pin. Therefore, proper layout is necessary for noise immunity. If capacitor is unavoidable, capacitor value should be carefully calculated and not to influence system operation.

### Protection

The R7780 provides fruitful protection functions that intend to protect system from being damaged. All the protection functions can be listed as below.

- **Cycle-by-Cycle Current Limit**

  This is a basic but very useful function and it can be implemented easily in current mode controller.

- **Over Load Protection**

  Long time cycle-by-cycle current limit will lead to system thermal stress. To further protect system, system will be shut down after about 56ms. After shutdown, system will resume and behave as hiccup. Through our proprietary prolong turn off period as hiccup, the power loss and thermal during OLP will be averaged to an acceptable level over the ON/OFF cycle of the IC. This will last until fault is removed.

- **Over Voltage Protection**

  Output voltage can be roughly sensed by VDD pin. If the sensed voltage reaches 28V threshold, system will be shut down after 20μs deglitch delay. This will last until fault is removed.

- **Over Temperature Protection**

  Internal 110/140°C hysteresis comparator will provide Over Temperature Protection (OTP) for controller itself. It's not suggested to use the function as precise OTP. OTP will not shut down system. It stops the system from switching until the temperature is under 110°C. Meanwhile , if $V_{DD}$ touches $V_{DD}$ turn off threshold voltage, system will hiccup.

- **Feedback Open and Opto short**

  This will trigger OVP or 56ms delay protection. It depends on which one occurs first.

### CS Pin Open Protection

When CS pin is opened, the system will be shut down and into auto recovery after couples of cycle. It could pass CS pin open test easier.

### Secondary Rectifier Short Protection

As shown in Figure 2. The current spike during secondary rectifier short test is extremely high because of saturated main transformer. Meanwhile, the transformer acts like a leakage inductance. During high line, the current in power FET is sometimes too high to wait for a 56ms OLP delay time. To offer better and easier protection design, the R7780 shuts down the controller after couples of cycles before fuse is blown up.

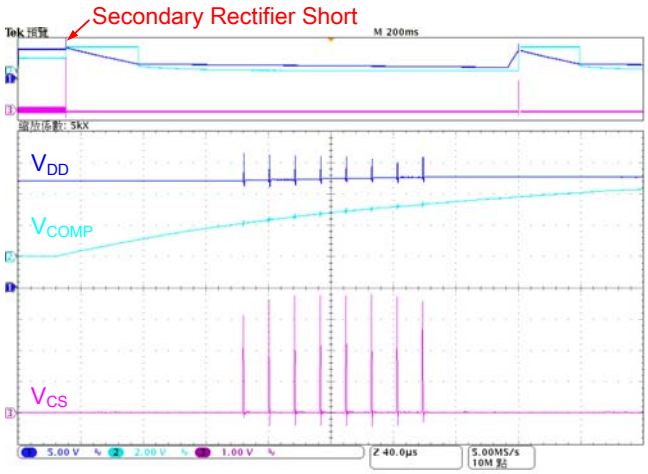



Figure 2. Secondary Rectifier Short Protection

### Negative Voltage Spike on Each Pin

Negative voltage (< -0.3V) on each pin will cause substrate injection. It leads to controller damage or circuit false trigger. Generally, it happens at CS pin due to negative spike because of improper layout or inductive current sense resistor. Therefore, it is highly recommended to add a R-C filter to avoid CS pin damage, as shown in Figure 3. Proper layout and careful circuit design should be done to guarantee yield rate in mass production.

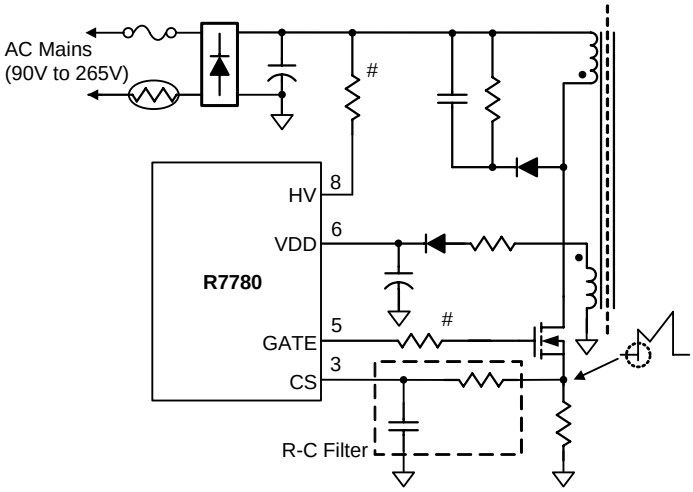



Figure 3. R-C Filter on CS Pin

### Layout Considerations

A proper PCB layout can abate unknown noise interference and EMI issue in the switching power supply. Please refer to the guidelines when you want to design PCB layout for switching power supply:

- The current path(1) from bulk capacitor, transformer, MOSFET, Rcs return to bulk capacitor is a huge high frequency current loop. The path(2) from gate pin, MOSFET, Rcs return to bulk capacitor is also a huge high frequency current loop. They must be as short as possible to decrease noise coupling and kept a space to other low voltage traces, such as IC control circuit paths, especially. Besides, the path(3) between MOSFET ground(b) and IC ground(d) is recommend to be as short as possible, too.
- The path(4) from RCD snubber circuit to MOSFET is a high switching loop. Keep it as small as possible.
- The path(5) from bulk capacitor to HV pin is a high voltage loop. It is highly recommended that EN/DIS control paths will be kept as far as possible from path (1), path(2), path(3) and path(4).
- It is good for reducing noise, output ripple and EMI issue to separate ground traces of bulk capacitor(a), MOSFET(b), auxiliary winding(c) and IC control circuit (d). Finally, connect them together on bulk capacitor ground(a). The areas of these ground traces should be kept large.

- Placing bypass capacitor for abating noise on IC is highly recommended. The bypass capacitor should be placed as close to controller as possible.
- To minimize reflected trace inductance and EMI minimize the area of the loop connecting the secondary winding, the output diode, and the output filter capacitor. In addition, apply sufficient copper area at the anode and cathode terminal of the diode for heatsinking. Apply a larger area at the quiet cathode terminal. A large anode area can increase high-frequency radiated EMI.

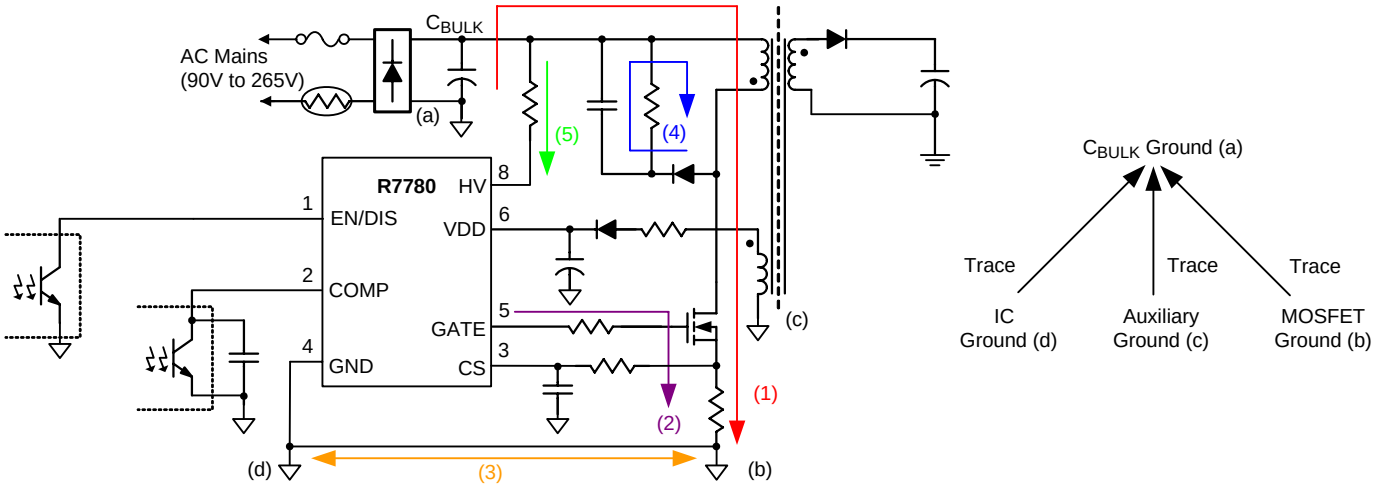
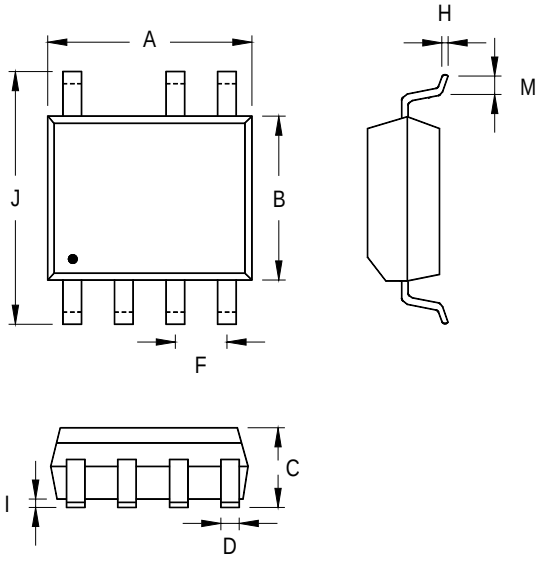



Figure 4. PCB Layout Guide

## Outline Dimension




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 4.801 | 5.004 | 0.189 | 0.197 |
| B | 3.810 | 3.988 | 0.150 | 0.157 |
| C | 1.346 | 1.753 | 0.053 | 0.069 |
| D | 0.330 | 0.508 | 0.013 | 0.020 |
| F | 1.194 | 1.346 | 0.047 | 0.053 |
| H | 0.170 | 0.254 | 0.007 | 0.010 |
| I | 0.050 | 0.254 | 0.002 | 0.010 |
| J | 5.791 | 6.200 | 0.228 | 0.244 |
| M | 0.400 | 1.270 | 0.016 | 0.050 |

**7-Lead SOP Plastic Package**

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