

## 200V P-CHANNEL MOSFET

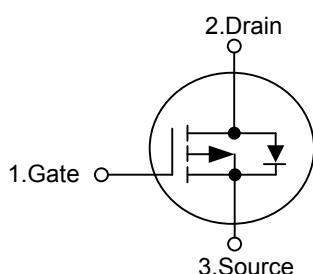
## ■ DESCRIPTION

The **7P20** uses advanced proprietary, planar stripe, DMOS technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with low gate voltages. This device is suitable for use as a load switch or in PWM applications. They are also well suited for high efficiency switching DC/DC converters.

## ■ FEATURES

- \*  $R_{DS(ON)} \leq 0.69\Omega @ V_{GS} = -10\text{ V}$
- \* Ultra low gate charge ( typical 19 nC )
- \* Low reverse transfer capacitance (  $C_{RSS} = \text{typical } 25\text{ pF}$  )
- \* Fast switching capability
- \* Avalanche energy specified
- \* Improved dv/dt capability, high ruggedness

## ■ SYMBOL



## ■ ORDERING INFORMATION

Ordering Number			Package	Pin Assignment			Packing
Normal	Lead Free	Halogen Free		1	2	3	
7P20-TN3-R	7P20L-TN3-R	7P20G-TN3-R	TO-252	G	D	S	Tape Reel

7P20L-TN3-R 	(1)R: Tape Reel (2)TN3: TO-252 (3)G: Halogen Free, L: Lead Free, Blank: Pb/Sn
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■ ABSOLUTE MAXIMUM RATINGS ( $T_c = 25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	$V_{DSS}$	-200	V
Gate-Source Voltage	$V_{GSS}$	$\pm 30$	V
Continuous Drain Current	$I_D$	-5.7	A
Pulsed Drain Current (Note 2)	$I_{DM}$	-22.8	A
Avalanche Current (Note 2)	$I_{AR}$	-5.7	A
Single Pulsed Avalanche Energy (Note 3)	$E_{AS}$	570	mJ
Repetitive Avalanche Energy (Note 2)	$E_{AR}$	5.5	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	-5.5	V/ns
Power Dissipation	$T_a = 25^\circ\text{C}$ $T_c = 25^\circ\text{C}$	2.5	W
		55	
Junction Temperature	$T_J$	+150	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-55 ~ +150	$^\circ\text{C}$

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Pulse width limited by  $T_{J(\text{MAX})}$

3.  $L=26.3\text{mH}$ ,  $I_{AS}=-5.7\text{A}$ ,  $V_{DD}=-50\text{V}$ ,  $R_G=25\Omega$

4.  $I_{SD} \leq -7.3\text{A}$ ,  $di/dt \leq 300\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$

■ THERMAL DATA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Junction-to-Ambient	$\theta_{JA}$			110	$^\circ\text{C}/\text{W}$
Junction-to-Case	$\theta_{JC}$			2.27	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS ( $T_c=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0\text{ V}$ , $I_D=-250\text{ }\mu\text{A}$	-200			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	$I_D=-250\mu\text{A}$ , Referenced to $25^\circ\text{C}$		-0.1		$\text{V}/^\circ\text{C}$
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=-200\text{V}$ , $V_{GS}=0\text{V}$			-1	$\mu\text{A}$
Gate-Source Leakage Current	$I_{GSS}$	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 30\text{V}$			$\pm 100$	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(\text{TH})}$	$V_{DS}=V_{GS}$ , $I_D=-250\mu\text{A}$	-3.0		-5.0	V
Static Drain-Source On-Resistance	$R_{DS(\text{ON})}$	$V_{GS}=-10\text{V}$ , $I_D=-2.85\text{A}$		0.54	0.69	$\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=-40\text{V}$ , $I_D=-2.85\text{A}$ (Note 1)		3.7		S
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	$C_{ISS}$	$V_{DS}=-25\text{V}$ , $V_{GS}=0\text{V}$ , $f=1.0\text{MHz}$		590	770	pF
Output Capacitance	$C_{OSS}$			140	180	pF
Reverse Transfer Capacitance	$C_{RSS}$			25	35	pF
<b>SWITCHING PARAMETERS</b>						
Total Gate Charge	$Q_G$	$V_{DS}=-160\text{V}$ , $V_{GS}=-10\text{V}$ , $I_D=-7.3\text{A}$ (Note 1, 2)		19	25	nC
Gate Source Charge	$Q_{GS}$			4.6		nC
Gate Drain Charge	$Q_{GD}$			9.5		nC
Turn-ON Delay Time	$t_{D(\text{ON})}$	$V_{DD}=-100\text{V}$ , $I_D=-7.3\text{A}$ , $R_G=25\Omega$ (Note 1, 2)		15	40	ns
Turn-ON Rise Time	$t_R$			110	230	ns
Turn-OFF Delay Time	$t_{D(\text{OFF})}$			30	70	ns
Turn-OFF Fall-Time	$t_F$			42	90	ns

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Diode Forward Voltage	$V_{SD}$	$I_S = -5.7A, V_{GS} = 0V$			-5.0	V
Maximum Body-Diode Continuous Current	$I_S$				-5.7	A
Maximum Pulsed Drain-Source Diode Forward Current	$I_{SM}$				-22.8	A
Body Diode Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0V, I_S = -7.30 A$		180		ns
Body Diode Reverse Recovery Charge	$Q_{RR}$	$dI_F/dt = 100A/s$ (Note 1)		1.07		$\mu C$

Note: 1. Pulse Test : Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$

2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

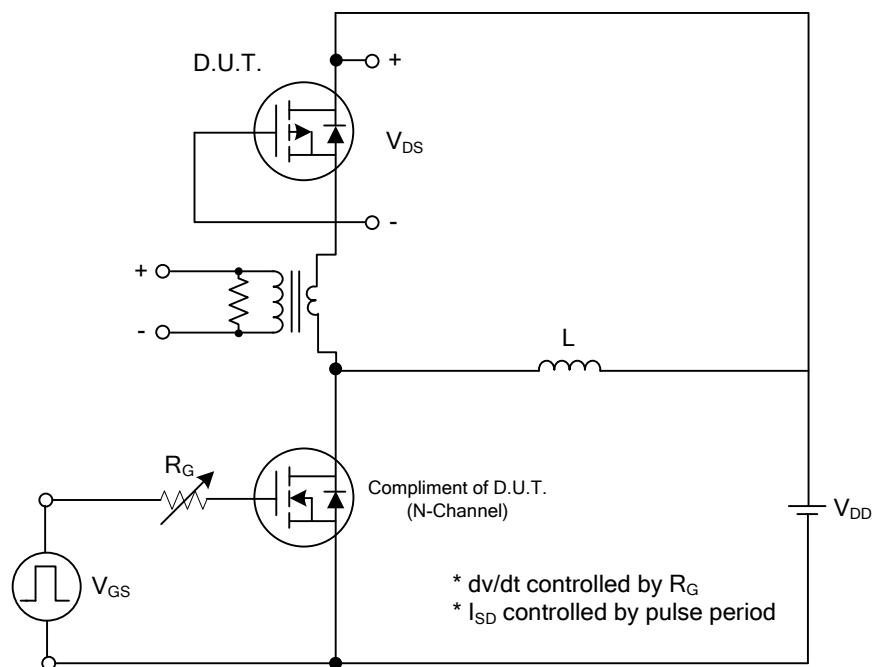


Fig. 1A Peak Diode Recovery  $dv/dt$  Test Circuit

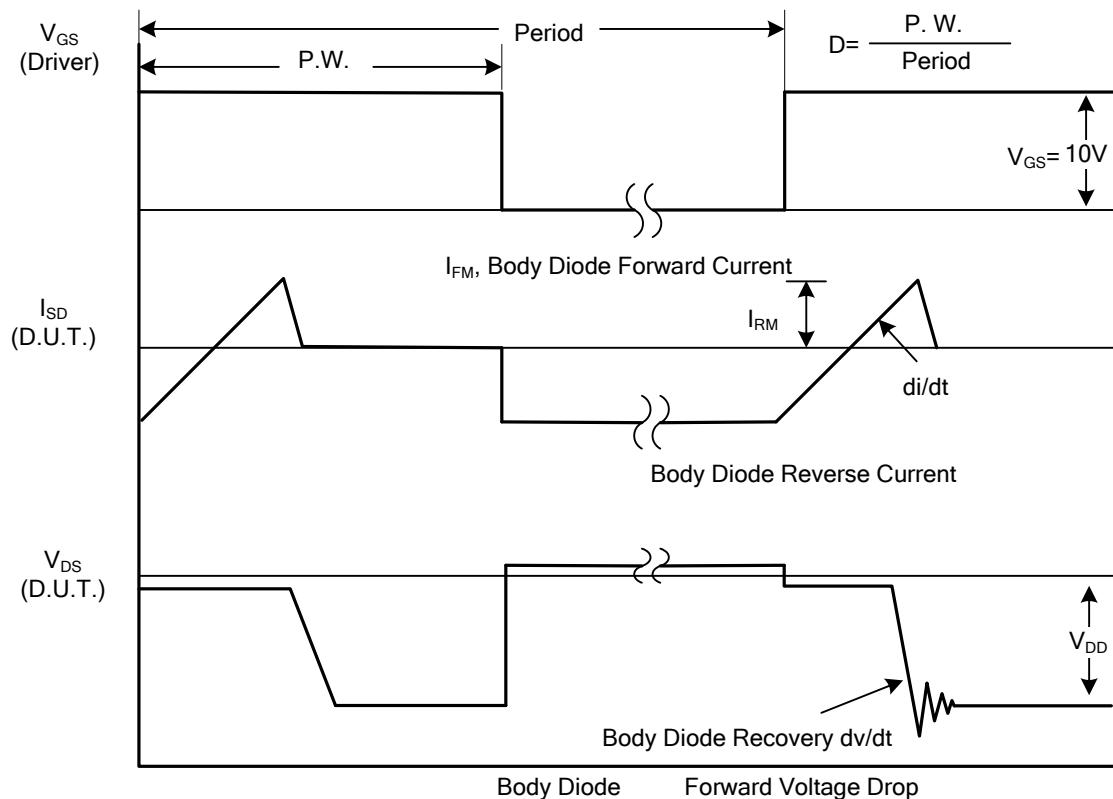


Fig. 1B Peak Diode Recovery  $dv/dt$  Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

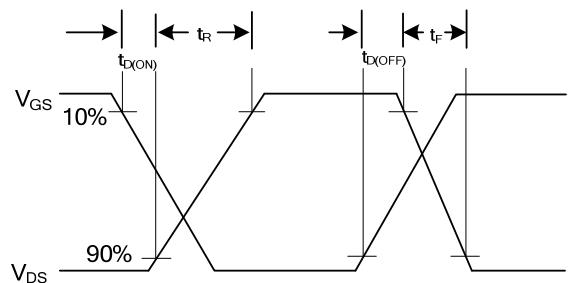
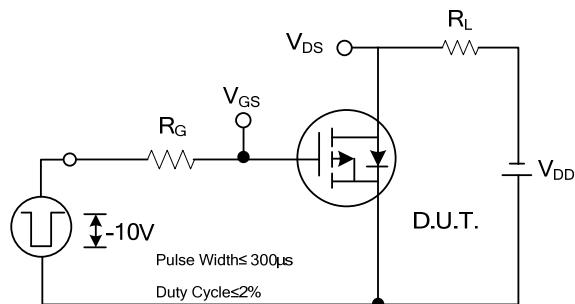


Fig. 2A Switching Test Circuit

Fig. 2B Switching Waveforms

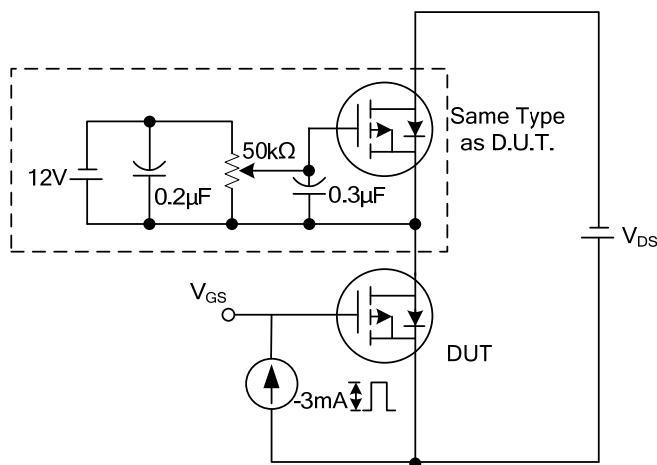


Fig. 3A Gate Charge Test Circuit

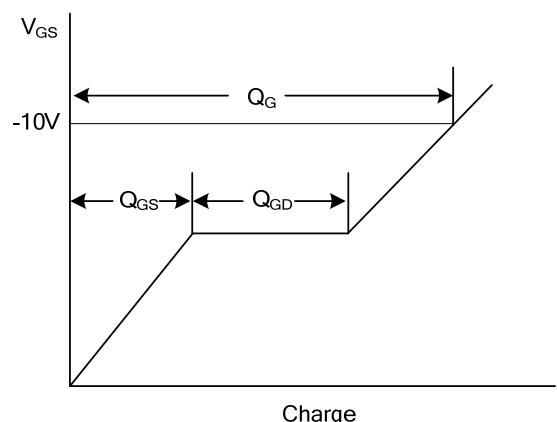


Fig. 3B Gate Charge Waveform

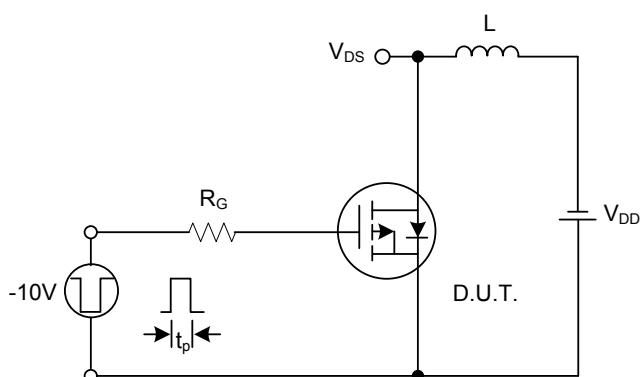


Fig. 4A Unclamped Inductive Switching Test Circuit

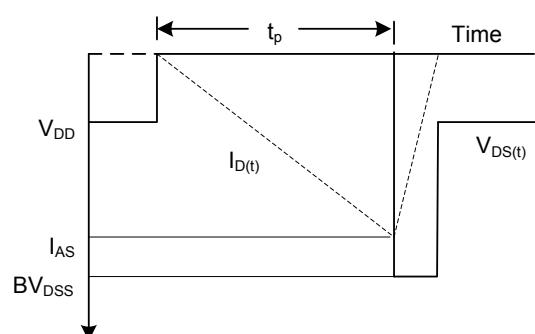


Fig. 4B Unclamped Inductive Switching Waveforms

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