

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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MOS FIELD EFFECT TRANSISTOR

μ PA2755AGR

SWITCHING

N-CHANNEL POWER MOS FET

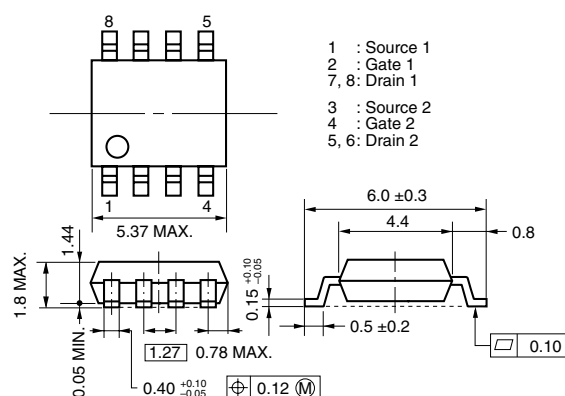
DESCRIPTION

The μ PA2755AGR is Dual N-channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

FEATURES

- Dual chip type
- Low on-state resistance
 $R_{DS(on)1} = 18 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 4.0 \text{ A)}$
 $R_{DS(on)2} = 29 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 4.0 \text{ A)}$
- Low input capacitance
 $C_{iss} = 650 \text{ pF TYP.}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit: mm)

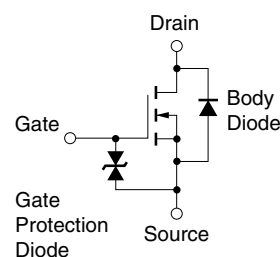


ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 8.0	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 32	A
Total Power Dissipation (1 unit) ^{Note2}	P_T	1.7	W
Total Power Dissipation (2 units) ^{Note2}	P_T	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \text{ to } +150$	$^\circ\text{C}$
Single Avalanche Current ^{Note3}	I_{AS}	8	A
Single Avalanche Energy ^{Note3}	E_{AS}	6.4	mJ

EQUIVALENT CIRCUIT

(1/2 circuit)



Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Mounted on ceramic substrate of $2000 \text{ mm}^2 \times 2.2 \text{ mm}$

3. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 15 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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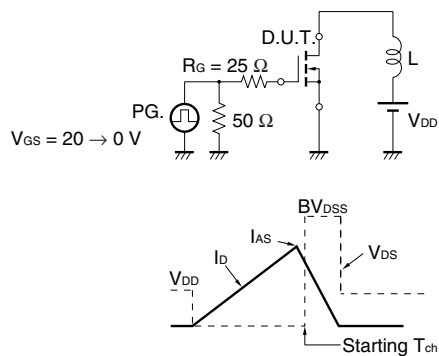
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ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

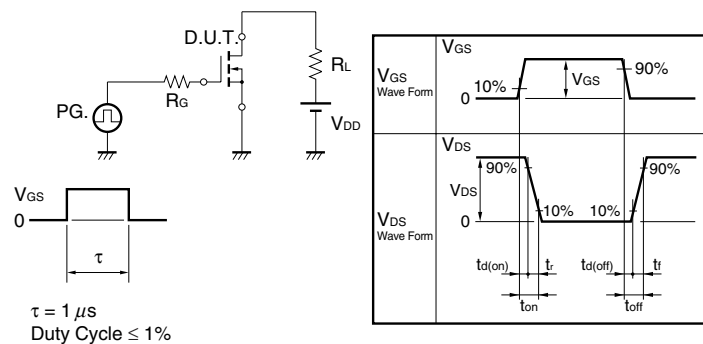
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±18 V, V _{DS} = 0 V			±10	μA
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5		2.5	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = 10 V, I _D = 4.0 A	2.8	5.7		S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)1}	V _{GS} = 10 V, I _D = 4.0 A		14	18	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 4.0 A		21	29	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		650		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		150		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		98		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 4.0 A		12		ns
Rise Time	t _r	V _{GS} = 10 V		16		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		38		ns
Fall Time	t _f			8.0		ns
Total Gate Charge	Q _G	V _{DD} = 24 V		13		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		2.2		nC
Gate to Drain Charge	Q _{GD}	I _D = 8.0 A		3.8		nC
Body Diode Forward Voltage ^{Note}	V _{F(S-D)}	I _F = 8.0 A, V _{GS} = 0 V		0.84		V
Reverse Recovery Time	t _{rr}	I _F = 8.0 A, V _{GS} = 0 V		17		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		8.2		nC

Note Pulsed

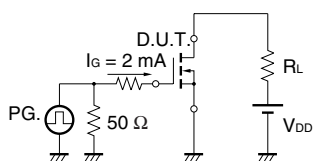
TEST CIRCUIT 1 AVALANCHE CAPABILITY



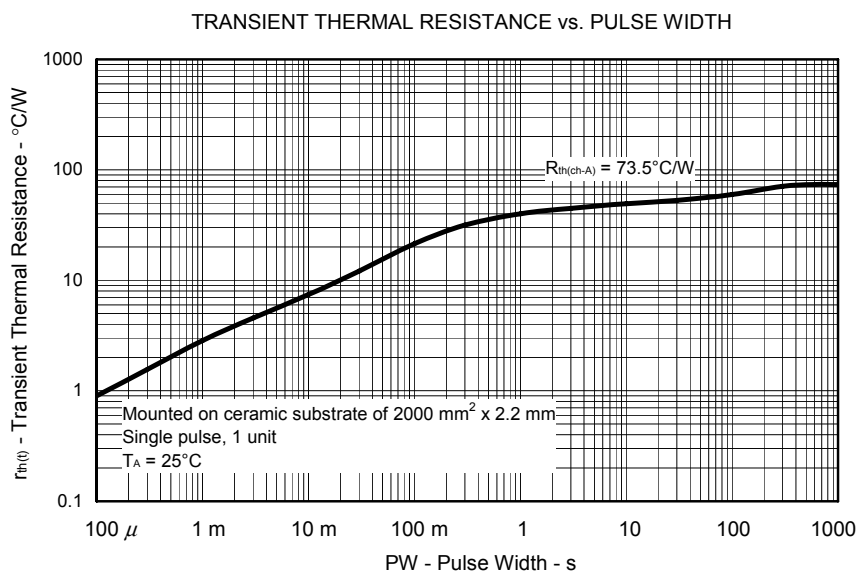
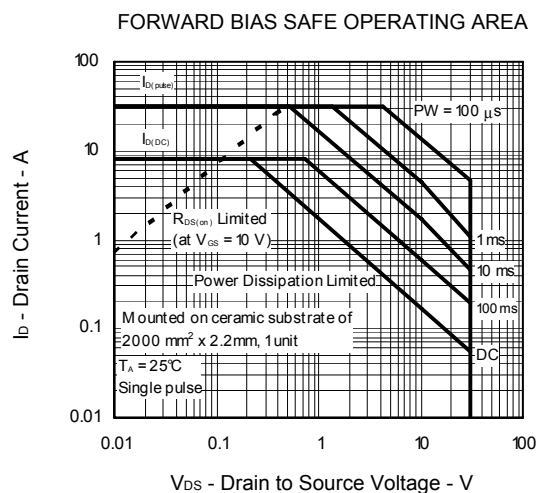
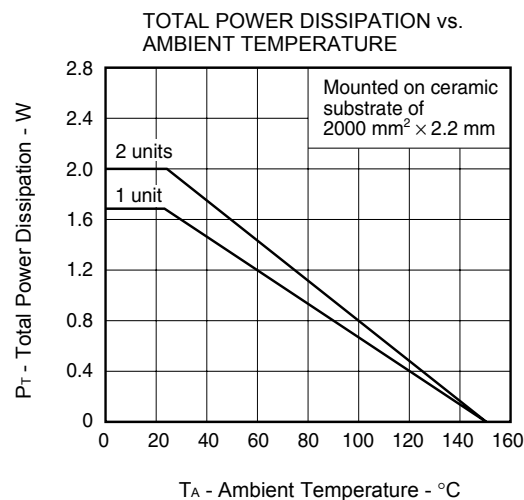
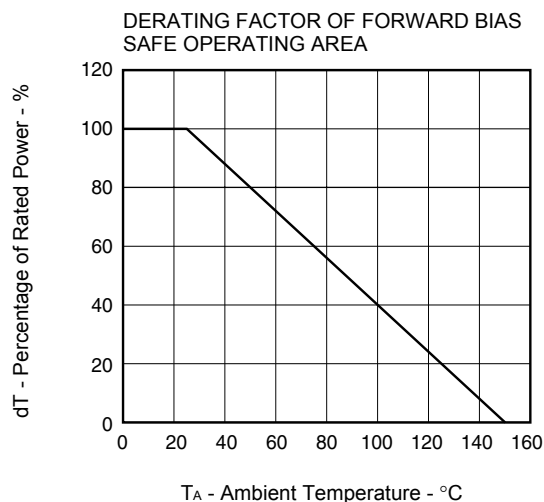
TEST CIRCUIT 2 SWITCHING TIME



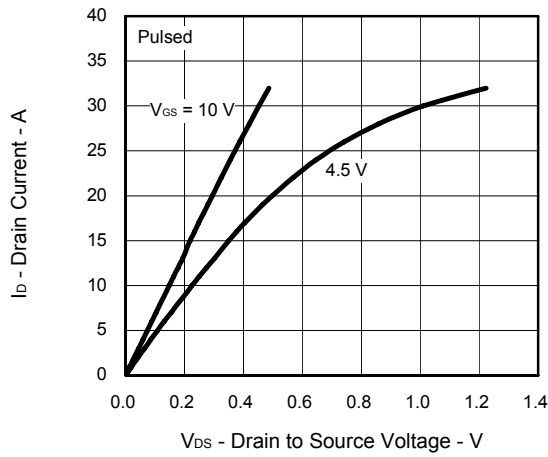
TEST CIRCUIT 3 GATE CHARGE



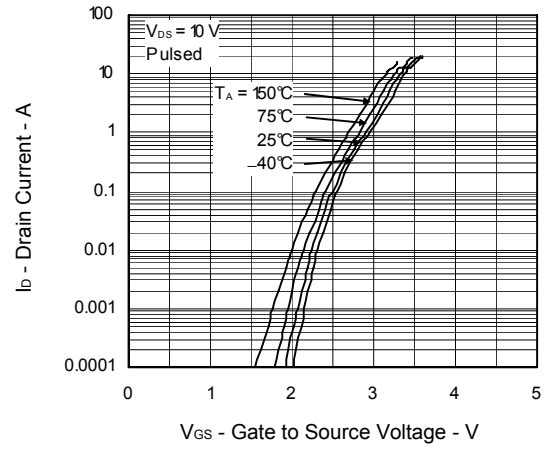
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



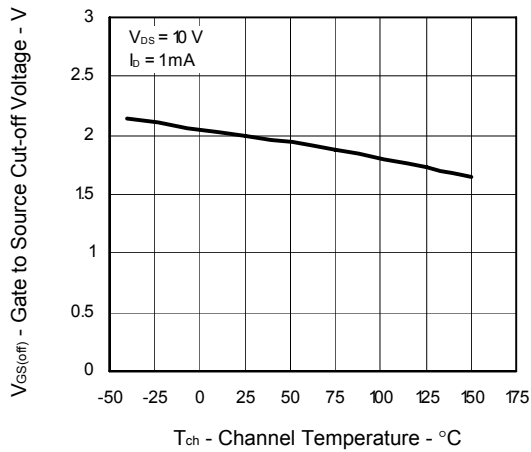
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



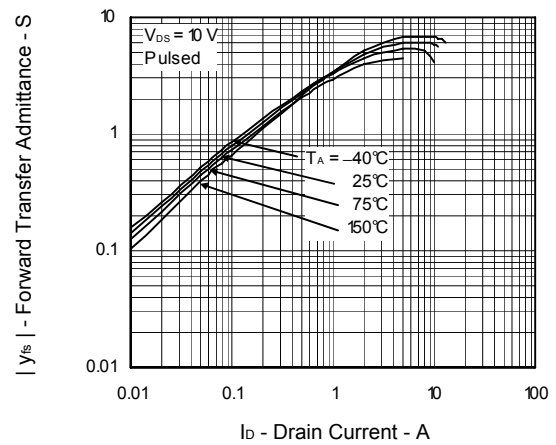
FORWARD TRANSFER CHARACTERISTICS



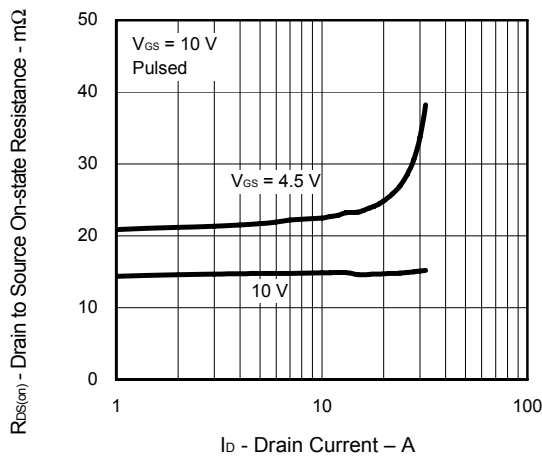
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



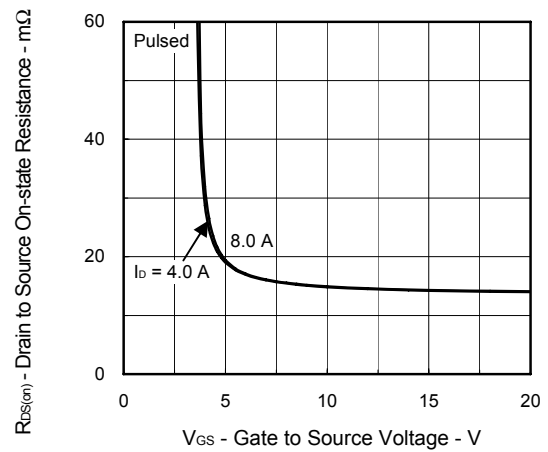
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



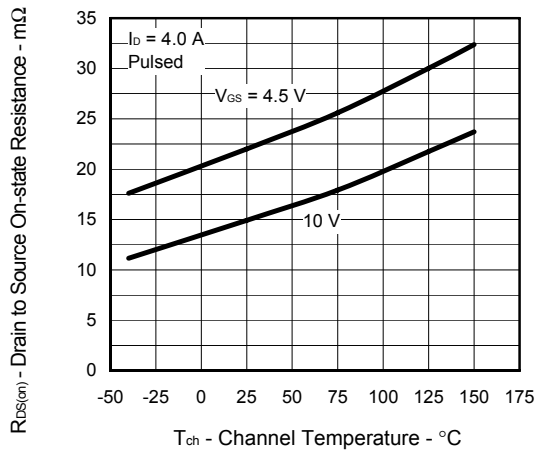
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



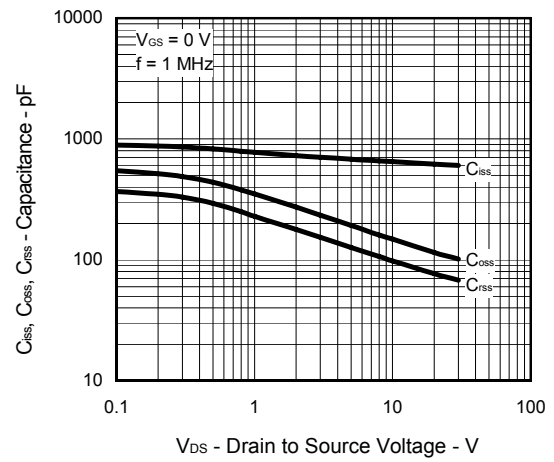
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



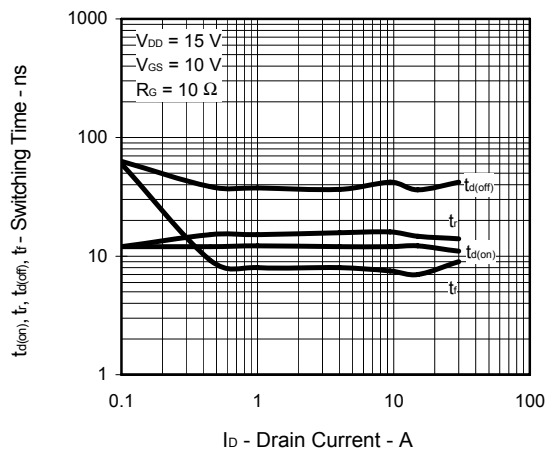
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



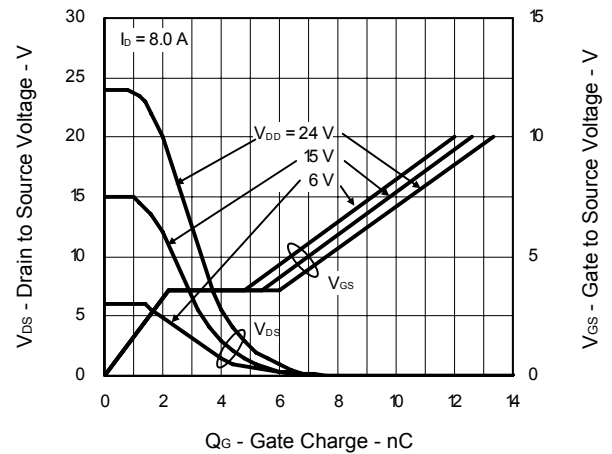
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



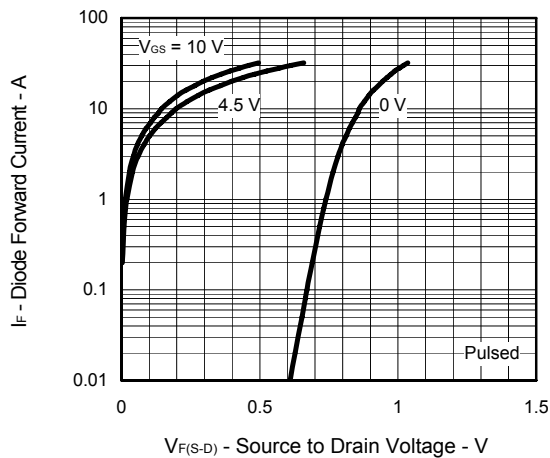
SWITCHING CHARACTERISTICS



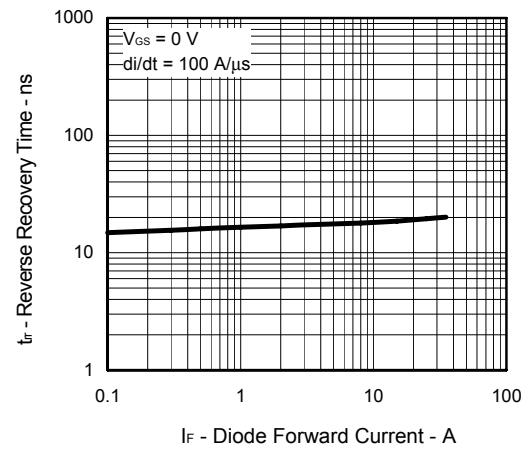
DYNAMIC INPUT/OUTPUT CHARACTERISTICS

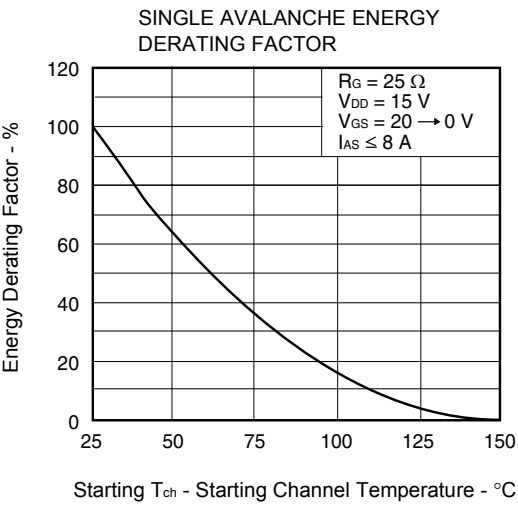
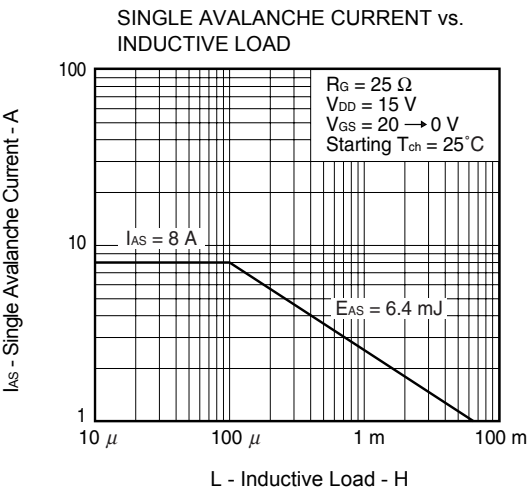


SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT





ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
μ PA2755AGR-E1-AT ^{Note}	Pure Sn (Tin)	Tape 2500 p/reel	Power SOP8
μ PA2755AGR-E2-AT ^{Note}			0.08 g TYP.

Note Pb-free (This product does not contain Pb in external electrode and other parts.)

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