

DS26LV32AT 3V Enhanced CMOS Quad Differential Line Receiver

Check for Samples: [DS26LV32AT](#)

FEATURES

- Low Power CMOS Design (30 mW typical)
- Interoperable with Existing 5V RS-422 Networks
- Industrial and Military Temperature Range
- Conforms to TIA/EIA-422-B (RS-422) and ITU-T V.11 Recommendation
- 3.3V Operation
- $\pm 7V$ Common Mode Range @ $V_{ID} = 3V$
- $\pm 10V$ Common Mode Range @ $V_{ID} = 0.2V$
- Receiver OPEN Input Failsafe Feature
- Guaranteed AC Parameter:
 - Maximum Receiver Skew: 4 ns
 - Maximum Transition Time: 10 ns
- Pin Compatible with DS26C32AT
- 32 MHz Toggle Frequency
- > 6.5k ESD Tolerance (HBM)

- Available in SOIC and CLGA Packaging
- Standard Microcircuit Drawing (SMD) 5962-98585

DESCRIPTION

The DS26LV32A is a high speed quad differential CMOS receiver that meets the requirements of both TIA/EIA-422-B and ITU-T V.11. The CMOS DS26LV32AT features typical low static I_{CC} of 9 mA which makes it ideal for battery powered and power conscious applications. The TRI-STATE enables, EN and EN*, allow the device to be active High or active Low. The enables are common to all four receivers.

The receiver output (RO) is guaranteed to be High when the inputs are left open. The receiver can detect signals as low as ± 200 mV over the common mode range of $\pm 10V$. The receiver outputs (RO) are compatible with TTL and LVCMOS levels.

Connection Diagram

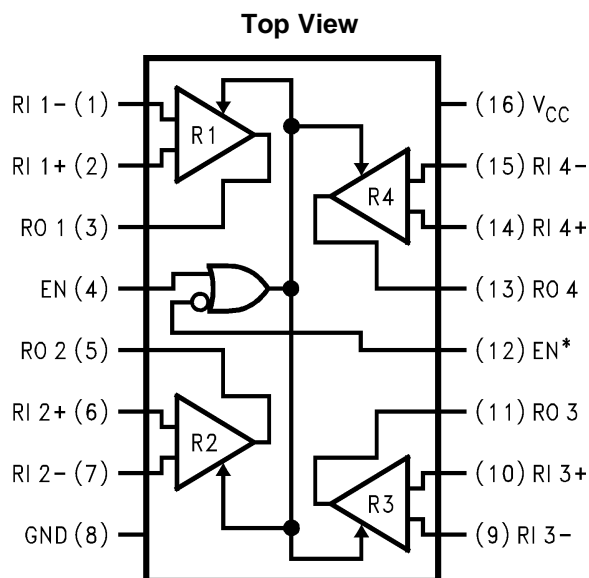


Figure 1.
SOIC Package
See Package Numbers D0016A or NAD0016A



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

Truth Table⁽¹⁾

Enables		Inputs	Output
EN	EN*	RI+–RI–	RO
L	H	X	Z
All other combinations of enable inputs		$V_{ID} \geq +0.2V$	H
		$V_{ID} \leq -0.2V$	L
		Open ⁽²⁾	H

- (1) L = Logic Low
 H = Logic High
 X = Irrelevant
 Z = TRI-STATE
- (2) Open, not terminated



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

Supply Voltage (V_{CC})	–0.5V to +7V
Enable Input Voltage (EN, EN*)	–0.5V to $V_{CC} + 0.5V$
Receiver Input Voltage (V_{ID} : RI+, RI–)	$\pm 14V$
Receiver Input Voltage (VCM: RI+, RI–)	$\pm 14V$
Receiver Output Voltage (RO)	–0.5V to $V_{CC} + 0.5V$
Receiver Output Current (RO)	± 25 mA Maximum
Maximum Package Power Dissipation @ +25°C	
D0016A Package	1190 mW
NAD0016A Package	1087 mW
Derate D0016A Package 9.8 mW/°C above +25°C	
Derate NAD0016A Package 7.3 mW/°C above +25°C	
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range Soldering (4 Sec.)	+260°C
ESD Ratings (HBM, 1.5 k Ω , 100 pF)	
Receiver Inputs and Enables	≥ 6.5 kV
Other Pins	≥ 2 kV

- (1) “Absolute Maximum ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The [Electrical Characteristics](#) specifies conditions of device operation.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature Range (T_A)				
DS26LV32AT	–40	+25	+85	°C
DS26LV32AW	–55	+25	+125	°C

Electrical Characteristics (1) (2)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.

Parameter	Test Conditions	Pin	Min	Typ	Max	Units	
V _{TH}	Differential Input Threshold V _{OUT} = V _{OH} or V _{OL}	RI+, RI-	V _{CM} = -7V to +7V, T _A = -40°C to +85°C	-200	±17.5	+200	mV
			V _{CM} = -0.5V to +5.5V, T _A = -55°C to +125°C ⁽³⁾	-200		+200	mV
V _{HY}	Hysteresis			35		mV	
V _{IH}	Minimum High Level Input Voltage	EN, EN*	2.0			V	
V _{IL}	Maximum Low Level Input Voltage				0.8	V	
R _{IN}	Input Resistance		V _{IN} = -7V, +7V, T _A = -40°C to +85°C (Other Input = GND)	5.0	8.5		kΩ
			V _{IN} = -0.5V, +5.5V, T _A = -55°C to +125°C (Other Input = GND) ⁽³⁾	5.0			kΩ
I _{IN}	Input Current (Other Input = 0V, Power On, or V _{CC} = 0V)	RI+, RI-	V _{IN} = +10V	0	1.1	1.8	mA
			V _{IN} = +3V				
			V _{IN} = 0.5V				
			V _{IN} = -3V	0	-0.43		mA
			V _{IN} = -10V				
			V _{IN} = -0.5V	0		-1.8	mA
			V _{IN} = 5.5V				
					1.8	mA	
I _{EN}	Input Current	EN, EN*			±1	μA	
V _{OH}	High Level Output Voltage		I _{OH} = -6 mA, V _{ID} = +1V	2.4	3		V
			I _{OH} = -6 mA, V _{ID} = OPEN				
V _{OH}	High Level Output Voltage		I _{OH} = -100 μA, V _{ID} = +1V		V _{CC} - 0.1		V
			I _{OH} = -100 μA, V _{ID} = OPEN				
V _{OL}	Low Level Output Voltage			0.13	0.5	V	
I _{OZ}	Output TRI-STATE Leakage Current		V _{OUT} = V _{CC} or GND			±50	μA
			EN = V _{IL} , EN* = V _{IH}				
I _{SC}	Output Short Circuit Current		-10	-35	-70	mA	
I _{CC}	Power Supply Current	V _{CC}	No Load, All RI+, RI- = OPEN, EN, EN* = V _{CC} or GND	T _A = -40°C to +85°C	9	15	mA
			T _A = -55°C to +125°C			20	mA

 (1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{ID}.

 (2) All typicals are given for: V_{CC} = +3.3V, T_A = +25°C.

(3) This parameter does not meet the TIA/EIA-422-B specification.

(4) Short one output at a time to ground. Do not exceed package.

Switching Characteristics - Industrial ^{(1) (2)}

Over Supply Voltage and -40°C to +85°C Operating Temperature range, unless otherwise specified.

Parameter		Test Conditions	Min	Typ	Max	Units
t _{PHL}	Propagation Delay High to Low	C _L = 15 pF, V _{CM} = 1.5V (Figure 2 and Figure 3)	6	17.5	35	ns
t _{PLH}	Propagation Delay Low to High		6	17.8	35	ns
t _r	Rise Time (20% to 80%)			4.1	10	ns
t _f	Fall Time (80% to 20%)			3.3	10	ns
t _{PHZ}	Disable Time	C _L = 50 pF, V _{CM} = 1.5V (Figure 4 and Figure 5)			40	ns
t _{PLZ}	Disable Time				40	ns
t _{PZH}	Enable Time				40	ns
t _{PZL}	Enable Time				40	ns
t _{SK1}	Skew, t _{PHL} - t _{PLH} ⁽³⁾	C _L = 15 pF, V _{CM} = 1.5V		0.3	4	ns
t _{SK2}	Skew, Pin to Pin ⁽⁴⁾			0.6	4	ns
t _{SK3}	Skew, Part to Part ⁽²⁾			7	17	ns
f _{MAX}	Maximum Operating Frequency ⁽⁵⁾	C _L = 15 pF, V _{CM} = 1.5V	32			MHz

(1) All typicals are given for: V_{CC} = +3.3V, T_A = +25°C.

(2) t_{SK3} is the difference in propagation delay times between any channels of any devices. This specification (maximum limit) applies to devices within V_{CC} ±0.1V of one another, and a Delta T_A = ±5°C (between devices) within the operating temperature range. This parameter is guaranteed by design and characterization.

(3) t_{SK1} is the |t_{PHL} - t_{PLH}| of a channel.

(4) t_{SK2} is the maximum skew between any two channels within a device, either edge.

(5) All channels switching, Output Duty Cycle criteria is 40%/60% measured at 50%. Input = 1V to 2V, 50% Duty Cycle, t_r/t_f ≤ 5 ns. This parameter is guaranteed by design and characterization.

Switching Characteristics - Military

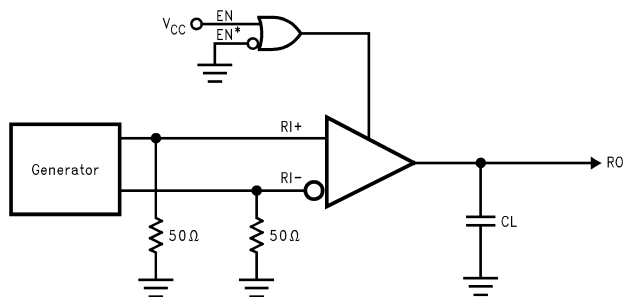
Over Supply Voltage and -55°C to +125°C Operating Temperature range, unless otherwise specified.

Parameter		Test Conditions	Min	Max	Units
t _{PHL}	Propagation Delay High to Low	C _L = 50 pF, V _{CM} = 1.5V (Figure 2 and Figure 3)	6	45	ns
t _{PLH}	Propagation Delay Low to High		6	45	ns
t _{PHZ}	Disable Time	C _L = 50 pF, V _{CM} = 1.5V (Figure 4 and Figure 5)		50	ns
t _{PLZ}	Disable Time			50	ns
t _{PZH}	Enable Time			50	ns
t _{PZL}	Enable Time			50	ns
t _{SK1}	Skew, t _{PHL} - t _{PLH} ⁽¹⁾	C _L = 50 pF, V _{CM} = 1.5V		6	ns
t _{SK2}	Skew, Pin to Pin ⁽²⁾			6	ns

(1) t_{SK1} is the |t_{PHL} - t_{PLH}| of a channel.

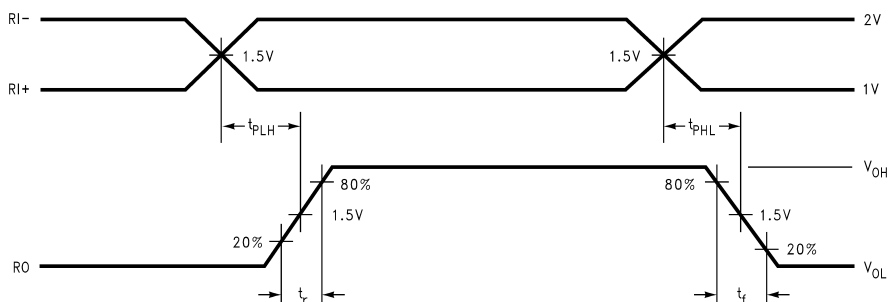
(2) t_{SK2} is the maximum skew between any two channels within a device, either edge.

PARAMETER MEASUREMENT INFORMATION



- A. Generator waveform for all tests unless otherwise specified: $f = 1 \text{ MHz}$, Duty Cycle = 50%, $Z_O = 50\Omega$, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.
- B. C_L includes probe and jig capacitance.

Figure 2. Receiver Propagation Delay and Transition Time Test Circuit



- A. Generator waveform for all tests unless otherwise specified: $f = 1 \text{ MHz}$, Duty Cycle = 50%, $Z_O = 50\Omega$, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.
- B. C_L includes probe and jig capacitance.
- C. For military grade product, $t_r \leq 6\text{ns}$ and $t_f \leq 6\text{ns}$.
- D. For military grade product the measure point is $1/2 V_{CC}$ for t_{PLH} , t_{PHL} , t_{PZL} , and t_{PZH} .

Figure 3. Receiver Propagation Delay and Transition Time Waveform

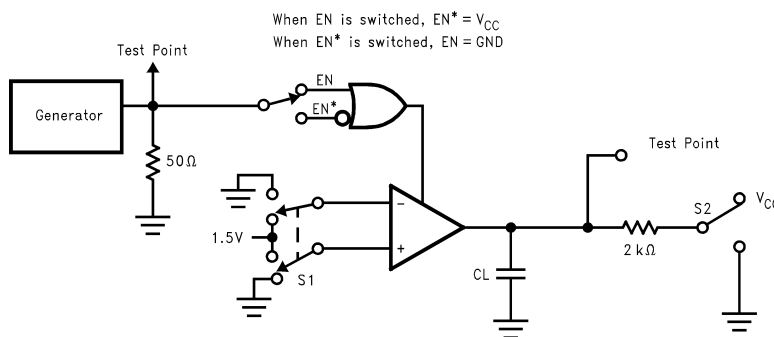
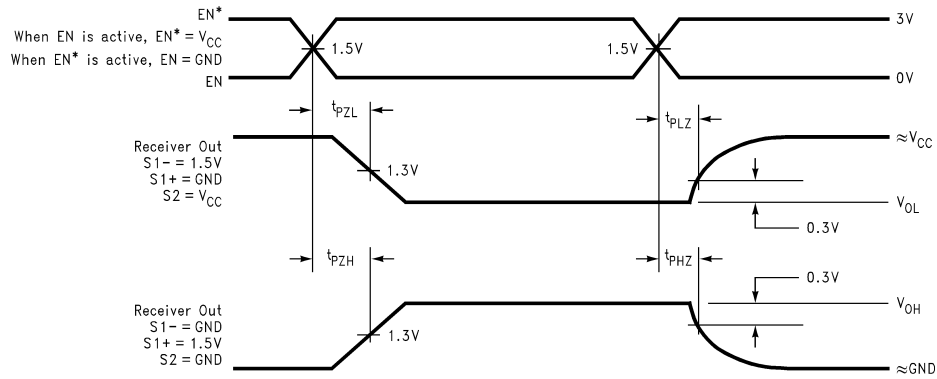


Figure 4. Receiver TRI-STATE Test Circuit



- Generator waveform for all tests unless otherwise specified: $f = 1 \text{ MHz}$, Duty Cycle = 50%, $Z_O = 50\Omega$, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.
- C_L includes probe and jig capacitance.
- For military grade product, $t_r \leq 6\text{ns}$ and $t_f \leq 6\text{ns}$.
- For military grade product the measure point is $1/2 V_{CC}$ for t_{PLH} , t_{PHL} , t_{PZL} , and t_{PZH} .

Figure 5. Receiver TRI-STATE Output Enable and Disable Waveforms

TYPICAL APPLICATION INFORMATION

General application guidelines and hints for differential drivers and receivers may be found in the following application notes:

- AN-214
- AN-457
- AN-805
- AN-847
- AN-903
- AN-912
- AN-916

Power Decoupling Recommendations:

Bypass caps must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1 μF in parallel with 0.01 μF at the power supply pin. A 10 μF or greater solid tantalum or electrolytic should be connected at the power entry point on the printed circuit board.

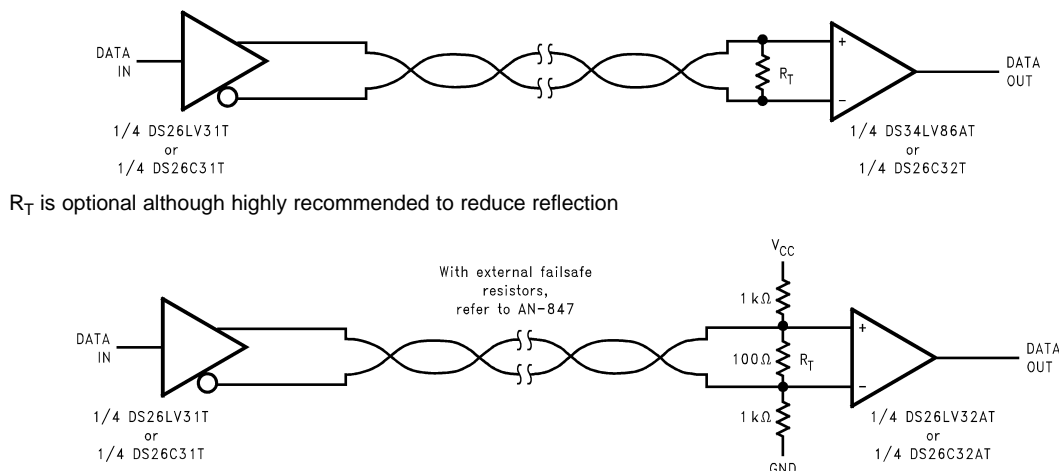


Figure 6. Typical Receiver Connections

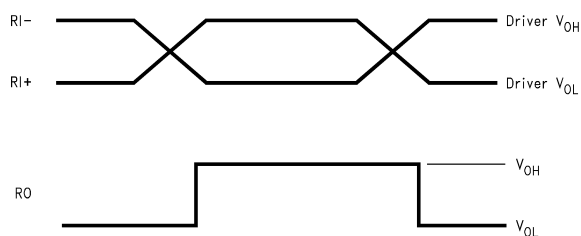


Figure 7. Typical Receiver Output Waveforms

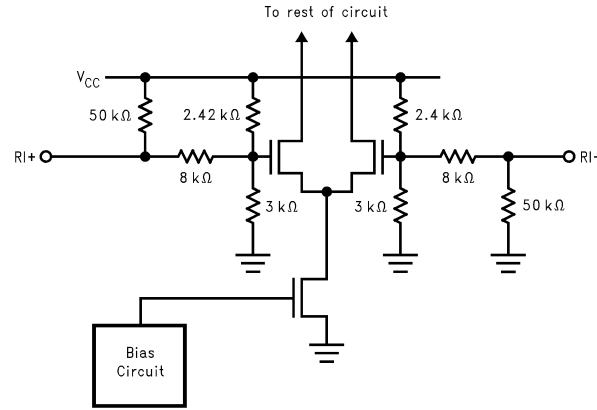


Figure 8. Typical Receiver Input Circuit

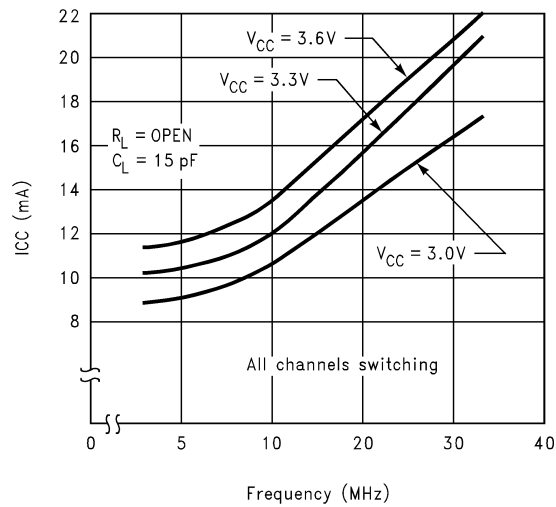


Figure 9. Typical I_{CC} vs Frequency

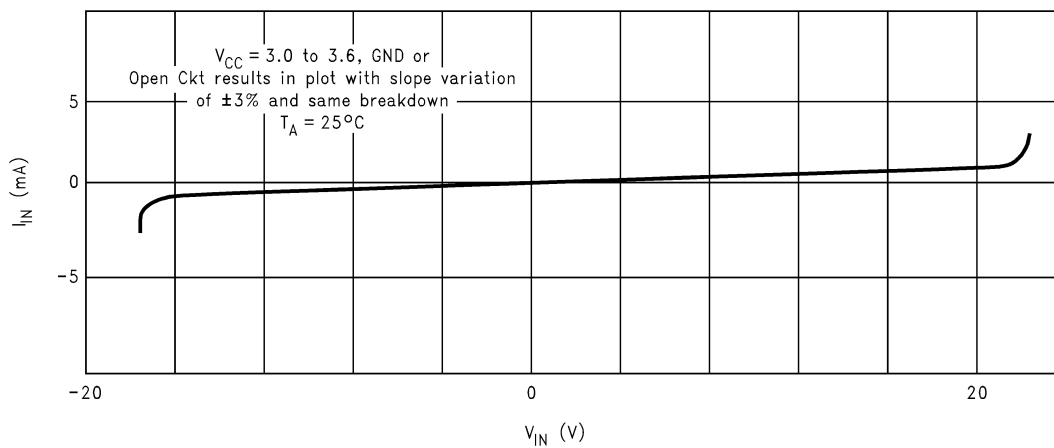


Figure 10. Receiver I_{IN} vs V_{IN} (Power On or Power Off)

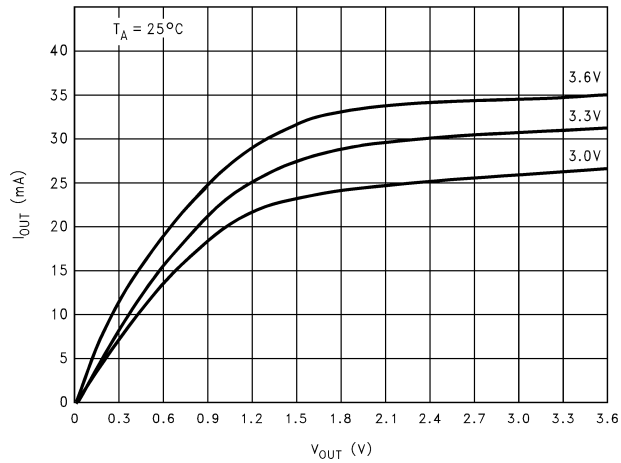


Figure 11. I_{OL} vs V_{OL}

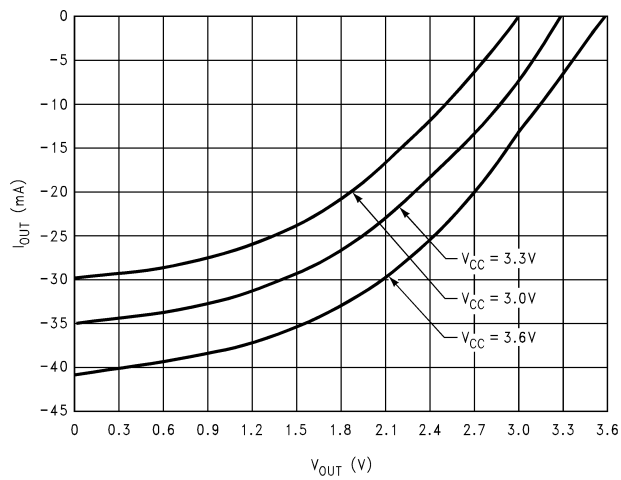


Figure 12. I_{OH} vs V_{OH}

REVISION HISTORY

Changes from Revision B (February 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS26LV32ATM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS26LV32A TM	Samples
DS26LV32ATMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS26LV32A TM	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



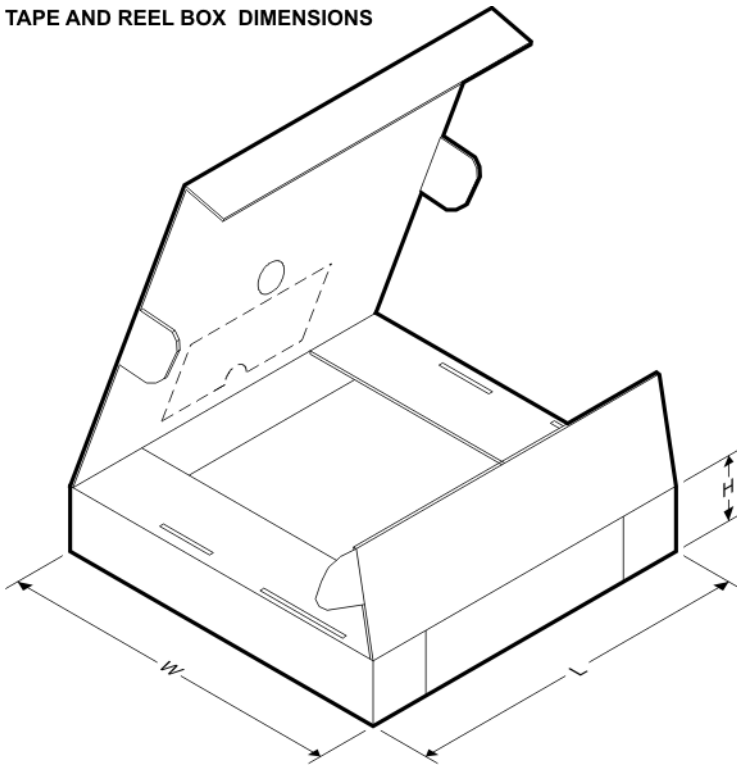
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS26LV32ATMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS26LV32ATMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.