

Data sheet acquired from Harris Semiconductor SCHS026C – Revised September 2003

CMOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

High-Voltage Types (20-Volt Rating)

CD4016B Series types are quad bilateral switches intended for the transmission or multiplexing of analog or digital signals. Each of the four independent bilateral switches has a single control signal input which simultaneously biases both the p and n device in a given switch on or off.

The CD4016 "B" Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

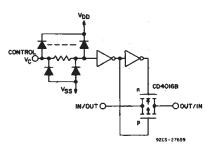
- 20-V digital or ± 10-V peak-to-peak switching
- 280-Ω typical on-state resistance for 15-V operation
- \blacksquare Switch on-state resistance matched to within 10 Ω typ. over 15-V signal-input range
- High on/off output-voltage ratio: 65 dB typ. @ f_{is} = 10 kHz, R_L = 10 k Ω
- High degree of linearity: <0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 V_{p-p} , V_{DD} - V_{SS} ≥ 10 V, R L = 10 k Ω
- Extremely low off-state switch leakage resulting in very low offset current and high effective off-state resistance:
 100 pA typ. @ VDD-VSS=18 V, TA=25°C
- Extremely high control input impedance (control circuit isolated from signal circuit: $10^{12} \Omega$ typ.
- Low crosstalk between switches: -50 dB typ. @ f_{is} = 0.9 MHz, R \underline{L} = 1 k Ω
- Matched control-input to signal-output capacitance:

Reduces output signal transients

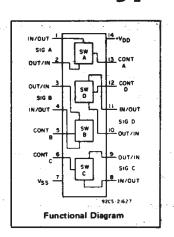
- Frequency response, switch on = 40 MHz (typ.)
- 100% tested for quiescent current at 20 V
- Maximum control input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V at 25°C
- 5-V, 10-V, and 15-V parametric ratings Applications:
- Analog signal switching/multiplexing
 Signal gating
 Modulator
 Squelch control
 Demodulator
 Chopper
 Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital & digital-toanalog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

CD4016B Types

SIG A IN 2 13 CONTROL A 3 12 CONTROL B 5 10 OUT SIG D CONTROL CONTROL



Schematic diagram - 1 of 4 identical sections.



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIN	UNITS	
	Min.	Max.	0.41.3
Supply Voltage Range (For T _A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, Absolute-Maximum Values:

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max+265°C

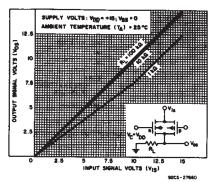


Fig. 1 – Typ. on-state characteristics for 1 of 4 switches with $V_{DD} = +15 V$, $V_{SS} = 0 V$.

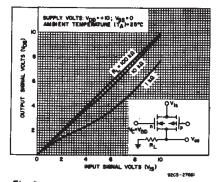


Fig. 2— Typ. on-state characteristics for 1 of 4 switches with $V_{DD} = +10 \text{ V}$, $V_{SS} = 0 \text{ V}$.

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ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TI	EST CONDITI	LIMITS AT INDICATED TEMPERATURES (°C)								
		V _{DD}			,-		+2	+25			
·	W.		(V)	(V)	-55	40	+85		Тур.	Max.	
Outros de Durin			0,5	5	0.25		7.5		0.01	0.25	1
Quiescent Device Current, IDD			0,10	10	0.5	0.5	15		0.01	0.5	μА
. 00	1		15	1	1	30	_	0.01	1		
Signal Inputs (Vis) and Output	(V _{OS})	0,20	20	5	5	150	150	0.02	5	<u> </u>
		05		Ι	l .	<u> </u>	-		<u> </u>	_	ı
On-State	VC = VDD	L				ندد					
Resistance, ron	R _L = 10kΩ	V _{is} =V _{DD} o	VSS	10	600	610	_		-	660	
Max.	Returned	V _{is} =4.75 to	5.75 \	10	1870	1900	2380	2600	_	2000	
.		V _{is} =V _{DD} or		15	360	370	520	600	_	400	Ω
	. 2 .	V _{is} =7.25 to	7.75 \	15	775	790	1080	1230	_	850	
∆On-State Resistance				5	_	_	_	_	15	_	
Between Any	.RL=10 kΩ,	$V_C = V_{DD}$		10	_	-	_	_	10	-	Ω
2 Switches, ∆ron			15	_	_	-	_	5		1	
Total Harmonic Distortion, THD	V _C =V _{DD} = = 5V (Sine v R _L =10 kΩ,	vave centere	d on 0	V)	_	_	_	_	0.4	-	%
-3dB Cutoff Frequency (Switch on)	$V_{is(p\cdot p)} = 5$	5V, V _{SS} = V (Sine wav n 0 V) R _L =	e		-	-	_	_	40	-	MHz
-50dB Feed- through Frequency (Switch off)	V _C =V _{SS} = - (Sine wave of R _L = 1 lkΩ	-5V, V _{is(p-p} centered on	5)=5V 0V)		-	-	-	_	1.25	_	MHz
Input/Output Leakage Current (Switch off) Iis Max.	$V_{C} = 0 V$ $V_{is} = 18 V$, $V_{is} = 0 V$, $V_{os} = 18 V$:	18	±0.1	±0.1	±1	±1	10-4	±0.1	μΑ
-50 dB Crosstalk Frequency	$\begin{array}{l} V_{C}(A) = V_{D} \\ V_{C}(B) = V_{S} \\ V_{is}(A) = 5 \\ 50 \Omega \text{ source} \\ R_{L} = 1 \text{ k}\Omega \end{array}$	S = -5 V, / _{P-p} ,		9	- .	_	1 2	_	0.9		MHz
Propagation	RL = 200 kl	Non = GND		5		_	_	-	40	100	
Delay (Signal	VC = VDD, CL = 50 pF	*88 - GIAD	•	10	_	-	_	_	20	40	ns
Input to Signal Output) t _{pd}	V _{is} = Square 0 to V _{DD} t _r , t _f = 20 ns	e Wave		15	-	-	-	-	15	30	
Capacitance: Input, C _{is}	V _{DD} = +5 V				_	_	_		4	_	
Output, C _{OS}	V _C = V _{SS} =				_	_	-	_	4	=	pF
Feedthrough, C _{ios}					_	_	-	_	0.2		

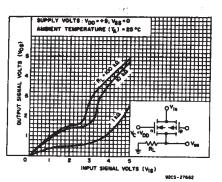


Fig. 3—Typ. on-state characteristics for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = 0 V.

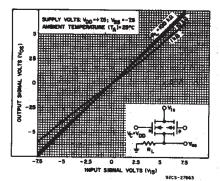


Fig. 4—Typ. on-state characteristics for 1 of 4 switches with V_{DD} =+7.5 V, V_{SS}=-7.5 V.

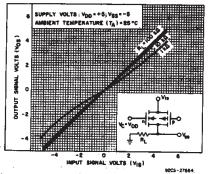


Fig. 5— Typ. on-state characteristics for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = -5 V.

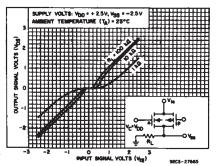


Fig. 6— Typ. on-state characteristics for 1 of 4 switches with V_{DD} = +2.5 V, V_{SS} = -2.5 V.

ELECTRICAL C	HARACTERISTICS (cont'd)									
CHARACTERISTIC	TEST CONDITIONS		LIMITS AT INDICATED TEMPERATURES (°C)							
		V _{DD}					+2	T		
		(v)	-55	-40	+85	+125	Тур.	Max.		
Control (V _C)										
Control Input Low Voltage, VILC (Max.)	$ I_{is} < 10 \mu A$ $V_{is} = V_{SS}, V_{OS} = V_{DD}$ and $V_{is} = V_{DD}, V_{OS} = V_{SS}$	5,10, 15	0.9	0.9	0.4	0.4	<u>-</u>	0.7	v,	
Control Input High Voltage, VIHC	See Fig. 10	5 10 15			7 (Min.) Min.) Min.)			٧	
Input Current, IN (Max.)	V _{is} ≤ V _{DD} V _{DD} - V _{SS} = 18 V V _{CC} ≤ V _{DD} - V _{SS}	18	±0.1	±0.1	±1	±1	±10-5	±0.1	μΑ	
Crosstalk (Con- trol Input to Signal Output)	$V_C = 10 \text{ V (Sq. Wave)}$ t_r , $t_f = 20 \text{ ns}$ $R_L = 10 \text{ k}\Omega$	10	_	_	-	_	50		mV	
Turn-On	t _r , t _f = 20 ns	5	_	_	_	_	35	70		
Propagation Delay	CL = 50 pF R _I = 1 kΩ	10	_	_	_	-	20	40	ns	
Delay	2	15	_	-	_	_	15	30		
Maximum Control Input Repetition Rate	$\begin{aligned} &V_{is} = V_{DD}, V_{SS} = GND, \\ &R_{L} = 1 \text{ k}\Omega \text{ to gnd,} \\ &C_{L} = 50 \text{ pF,} \\ &V_{C} = 10 \text{ V(Square} \\ &\text{wave centered on 5 V)} \\ &t_{r}, t_{f} = 20 \text{ ns,} \\ &V_{OS} = \frac{1}{2} V_{OS} @ 1 \text{ kHz} \end{aligned}$	10		_	_	_	10	-	MHz	
Input Capacitance, C _{IN}			_	_	_	_	5	7.5	μF	

			Switch Ir	Switch Output				
Via		Vos (V)						
(V)	-55°C	-40°C	25°C*	25°C▲	+85°C	+125°C	Min.	Max.
0	0.25	0.2	0.2	0.16	0.12	0.14	- 46	0.4
0	0.62	0.5	0.5	0.4	0.3	0.35	-	0.5
10	-0.62	0.5	-0.5	-0.4	-0.3	-0.35	9.5	
0 15	1.8 -1.8	1.4 -1,4	1.5 -1.5	1.2 -1.2	1 -1	1.1 -1.1	- 13.5	1.5 -
	0 5 0 10	(V) -55°C 0 0.25 5 -0.25 0 0.62 10 -0.62 0 1.8	(V) -55°C -40°C 0 0.25 0.2 5 -0.25 -0.2 0 0.62 0.5 10 -0.62 -0.5 0 1.8 1.4	Vis (V) Iis (m) 0 0.25°C -40°C 25°C* 0 0.25 0.2 0.2 5 -0.25 -0.2 -0.2 0 0.62 0.5 0.5 10 -0.62 -0.5 -0.5 0 1.8 1.4 1.5	(V) -55°C -40°C 25°C* 25°C* 0 0.25 0.2 0.2 0.16 5 -0.25 -0.2 -0.2 -0.16 0 0.62 0.5 0.5 0.5 0.4 10 -0.62 -0.5 -0.5 -0.4 0 1.8 1.4 1.5 1.2	V _{is} (V) 1 _{is} (mA) 0 -55°C -40°C 25°C* 25°C* +85°C 0 0.25 0.2 0.2 0.16 0.12 5 -0.25 -0.2 -0.2 -0.16 -0.12 0 0.62 0.5 0.5 0.4 0.3 10 -0.62 -0.5 -0.5 -0.4 -0.3 0 1.8 1.4 1.5 1.2 1	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$

^{*} Plastic package

Ceramic package

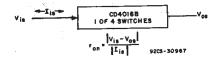


Fig. 10— Determination of $r_{\rm OR}$ as a test condition for control input high voltage (V_{IHC}) specification.

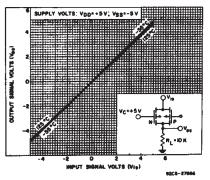


Fig. 7.— Typ. on-state characteristics as a function of temp. for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = -5 V.

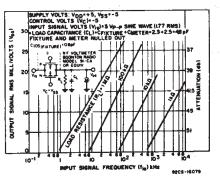


Fig. 8 — Typ. feedthru vs. frequency — switch off.

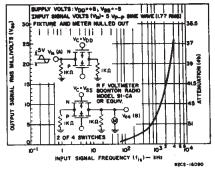


Fig. 9— Typical crosstalk between switch circuits in the same package.

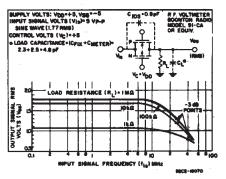


Fig. 11 — Typical frequency response — switch on.

TYPICAL ON-STATE RESISTANCE CHARACTERISTICS, TA = 25°C

CHARAC- TERISTIC*	SUP COND	PLY ITIONS	4		CONDI	AD TIONS		
			R _L =	R _L = 1kΩ		10kΩ	RL=	100kΩ
	V _{DD} (V)	V _{SS}	VALŪE (S2)	V _{is} (V)	VALUE:	V _i ,	VALUE	V _{is} (V)
	.45		200	+15	200	+15	180	+15
ron	+15	0	200	0	200	0	200	0
ron (max.)	+15	0	300	+11	300	+9.3	320	+9.2
_	+10	0	290	+10	250	+10	240	+10
ron	710	0	290	0	250	0	300	0
r _{on} (max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
	+ 5	5 0	860	+ 5	470	+ 5	450	+ 5
ron		·	600	0	. 580	0	800	0
r _{on} (max.)	+ 5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
	+7.5	-7.5	200	+7.5	200	+7.5	180	+7.5
ron			200	7.5	200	7.5	180	-7.5
ron (max.)	+7.5	-7.5	290	±0.25	280	±25	400	±0.25
r.	+ 5	- 5	260	+ 5	250	+ 5	240	+ 5
ron			310	- 5	250	- 5	240	– 5
ron (max.)	+ 5	- 5	600	±0.25	580	±0.25	760	±0.25
r	+2.5	~2.5	590	+2.5	450	+2.5	490	+2.5
ron	72.5	~2.0	720	-2.5	520	-2.5	520	-2.5
r _{on} (max.)	+2.5	-2.5	232k	±0.25	300k	±0.25	870k	±0.25

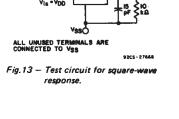
^{*} Variation from aperfect switch, $r_{on} = 0 \Omega$.



SCALE: X = 0.2 ma/DIV Y = 2.0 V/DIV VDD = VC = +5 V, VSS = 5 V, RL = $10 K\Omega$ CL = $16 p^{6}$ (IS = 1 KMz VIS = 5 V pp DISTORTION = 0.4 R

9205-27613

Fig. 15 – Typical sine wave response of V_{DD} = +5 V, V_{SS} = -5 V.



 $Q^{V_{DD}}$

ALL UNUSED TERMINALS ARE CONNECTED TO VSS

Fig. 12 - Off-state switch input or output leakage current test circuit.



SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV VDD = VC = +2.5V, VSS = -2.5V, R_L = 10ΚΩ C_L = 15 pF I_S = 1 KHz V_IS = 5V p.p DISTORTION = 3 %

92CS - 27614

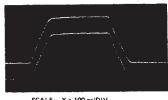
Fig. 16 – Typical sine wave response of V_{DD} = +2.5 V, V_{SS} = -2.5 V.



SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV VDD = VC = +7.5V, VSS = -7.5V, RL = 10KΩ CL = 15 pF fls = 1 KHz VIS = 5V pp DISTORTION = 0.2 %

92CS-27612

Fig. 14 - Typical sine wave response of V_{DD} = $+7.5 \text{ V}, \text{ V}_{SS} = -7.5 \text{ V}.$



SCALE: X = 100 ns/DIV Y = 5.0 V/DIV

92CS-276I5

Fig. 17 - Typical square wave response at $V_{DD} = V_C = +15 V$, $V_{SS} = Gnd$.



SCALE: X = 100 ns/DIV Y = 5.0 V/DIV

Fig. 18 — Typical square wave response at $V_{DD} = V_C = +10 \text{ V}$, $V_{SS} = Gnd$.

92CS-276I6



SCALE: X = 100 ns/DIV Y = 2 V/DIV

92CS-27617

Fig.19 - Typical square wave response at V_{DD} $= V_C = +5 V$, $V_{SS} = Gnd$.

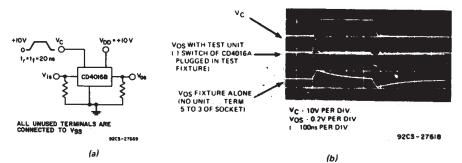


Fig. 20 - Crosstalk-control input to signal output.

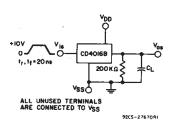


Fig.21 — Propagation delay time signal input (V_{IS}) to signal output (V_{OS}).

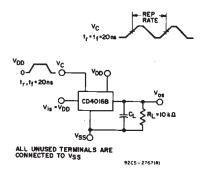


Fig. 22 - Max. control-input repetition rate.

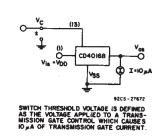


Fig.23 - Switch threshold voltage.

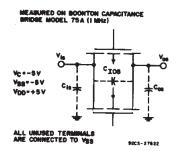
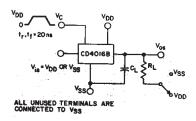


Fig.24 - Capacitance C_{IOS} and C_{OS}.



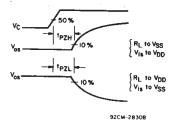
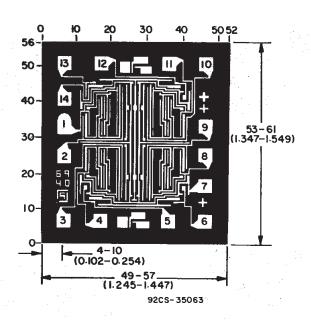


Fig.25 - Turn-On propagation delay-control input.

Dimensions and pad layout for CD4016BH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3}) inch).





10-Jun-2014

PACKAGING INFORMATION

Orderable Device	Status	Package Type	_	Pins	_	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
5962-9064001CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9064001CA CD4016BF3A	Samples
CD4016BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4016BE	Samples
CD4016BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4016BE	Samples
CD4016BF	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4016BF	Samples
CD4016BF3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9064001CA CD4016BF3A	Samples
CD4016BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016BM	Samples
CD4016BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016BM	Samples
CD4016BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016BM	Samples
CD4016BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016BM	Samples
CD4016BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016BM	Samples
CD4016BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016B	Samples
CD4016BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM016B	Samples
CD4016BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM016B	Samples
CD4016BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM016B	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

PACKAGE OPTION ADDENDUM



10-Jun-2014

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD4016B, CD4016B-MIL:

Catalog: CD4016B

Military: CD4016B-MIL

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product





10-Jun-2014

• Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

All ulmensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4016BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4016BMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4016BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4016BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4016BM96	SOIC	D	14	2500	367.0	367.0	38.0
CD4016BMT	SOIC	D	14	250	367.0	367.0	38.0
CD4016BNSR	SO	NS	14	2000	367.0	367.0	38.0
CD4016BPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
 - Sody length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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