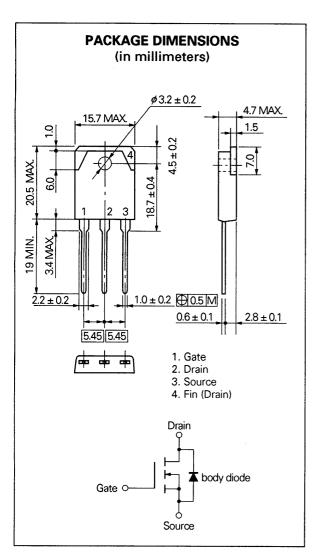
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N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR 2SK1271

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE



DESCRIPTION

The 2SK1271 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- High Voltage Rating VDss = 1 400 V
- Low On-state Resistance
 RDS(on) = 4.0 Ω MAX. (Vgs = 10 V, ID = 3 A)
- Low Ciss Ciss = 1 800 pF TYP.

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Tempera	ture	-55 to +150	°C
Channel Tempera	iture	150 MAX.	°C
Maximum Power D	issipation		
Total Power Dissi	240	W	
Maximum Voltages	and Currents (Ta = 25 °C)		
Voss	Drain to Source Voltage	1 400	٧
Vgss	Gate to Source Voltage	±20	٧
ID(DC)	Drain Current (DC)	± 5	Α
D(pulse)*	Drain Current (pulse)	±10	Α

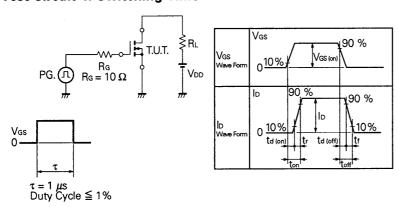
^{*} PW \leq 10 μ s, Duty Cycle \leq 1 %



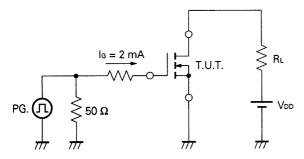
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	Ros(on)		3.5	4.0	Ω	Vgs = 10 V, lp = 3 A
Gate to Source Cutoff Voltage	Vgs(off)	1.5		3.5	V	Vos = 10 V, lo = 1 mA
Forward Transfer Admittance	y fs	1.5			S	Vos = 20 V, Io = 3 A
Drain Leakage Current	Ipss			100	μΑ	Vps = 1 120 V, Vgs = 0
Gate to Source Leakage Current	Igss			±100	μΑ	Vgs = ±20 V, Vps = 0
Input Capacitance	Ciss		1 800		pF	V _{DS} = 10 V V _{GS} = 0 f = 1 MHz
Output Capacitance	Coss		500		pF	
Reverse Transfer Capacitance	Crss		360		pF	
Turn-On Delay Time	td(on)		25		ns	$V_{GS} = 10 \text{ V}$ $V_{DD} = 150 \text{ V}$ $I_{D} = 3 \text{ A}, R_{G} = 10 \Omega$ $R_{L} = 50 \Omega$
Rise Time	tr		30		ns	
Turn-Off Delay Time	td(off)		220		ns	
Fall Time	tr		40		ns	
Total Gate Charge	QG		125		nC	V _{GS} = 10 V I _D = 5 A V _{DD} = 450 V
Gate to Source Charge	Qgs		15		nC	
Gate to Drain Charge	QGD		70		nC	
Diode Forward Voltage	V _F (S-D)		0.9		V	If = 5 A, Vgs = 0
Reverse Recovery Time	trr		1 400		ns	I _F = 5 A di/dt = 50 A/μs
Reverse Recovery Charge	Qrr		30		μC	

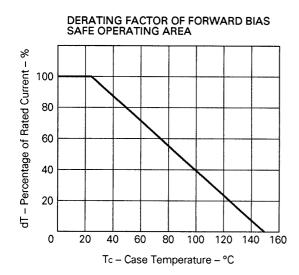
Test Circuit 1: Switching Time

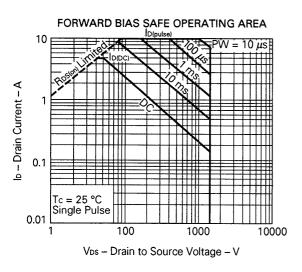


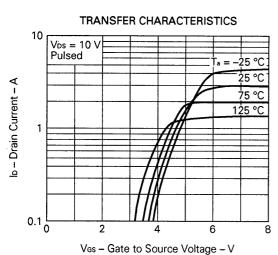
Test Circuit 2: Gate Charge

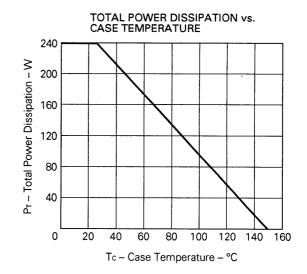


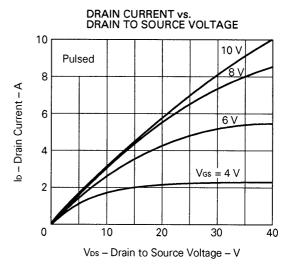
TYPICAL CHARACTERISTICS (Ta = 25 °C)



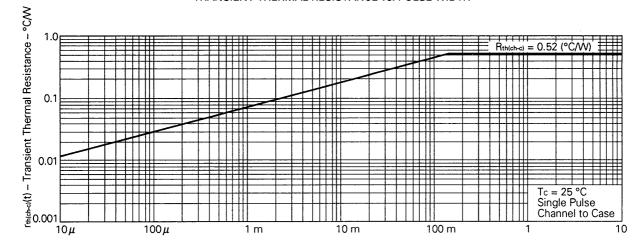




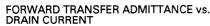


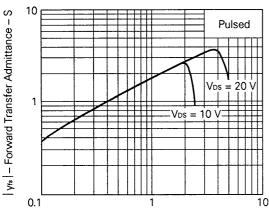


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

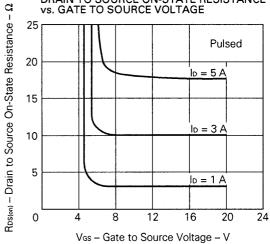


PW - Pulse Width - s



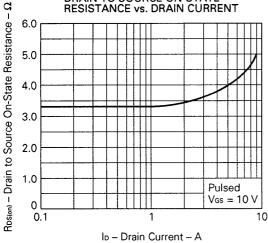


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

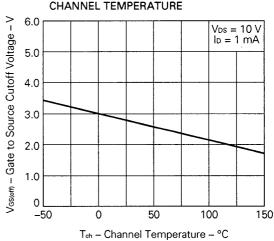


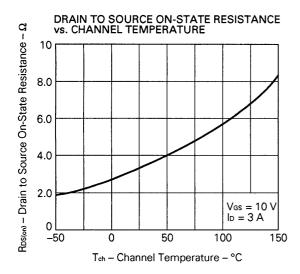
lo - Drain Current - A

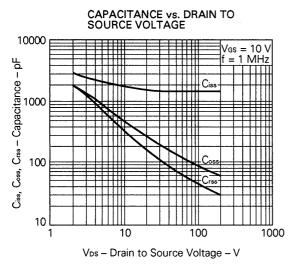
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

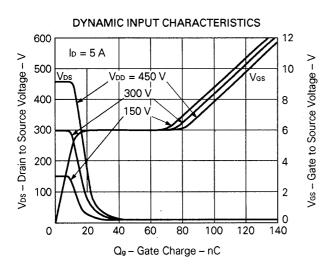


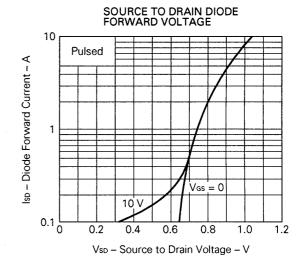
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

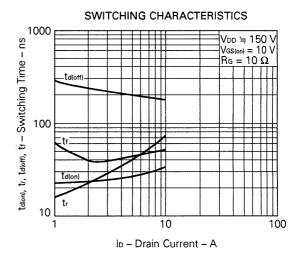


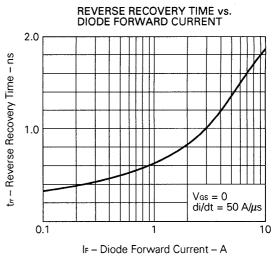












Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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Special: Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.

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