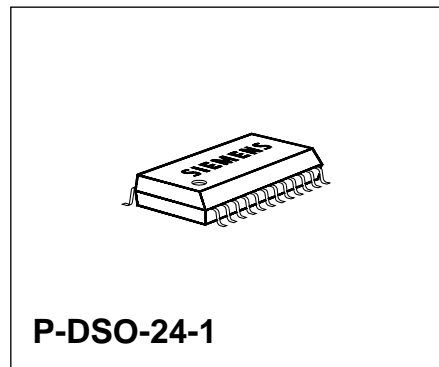


### 1 Overview

#### 1.1 Features

- 155 MHz FM and 40 MHz AM input frequency
- 30 mV<sub>eff</sub> AM and 50 mV<sub>eff</sub> FM sensitivity
- Additional open drain ports controlled by I<sup>2</sup>C Bus
- 2-pin quartz oscillator
- Fast phase detector with short anti-backlash pulses and polarity reversal
- Charge pump current programmable in four steps up to 4.5 mA
- Frequency resolution of 1, 5 and 10 kHz AM and 12.5, 25 and 50 kHz FM
- P-DSO-24 package



Type	Ordering Code	Package
SDA 4331X	Q67100-H5139	P-DSO-24-1

#### 1.2 Application

The SDA 4331X provides separated input and output ports for AM and FM and is well suited for extremely fast loop settling times in the FM mode.

1.3 Pin Configuration  
(top view)

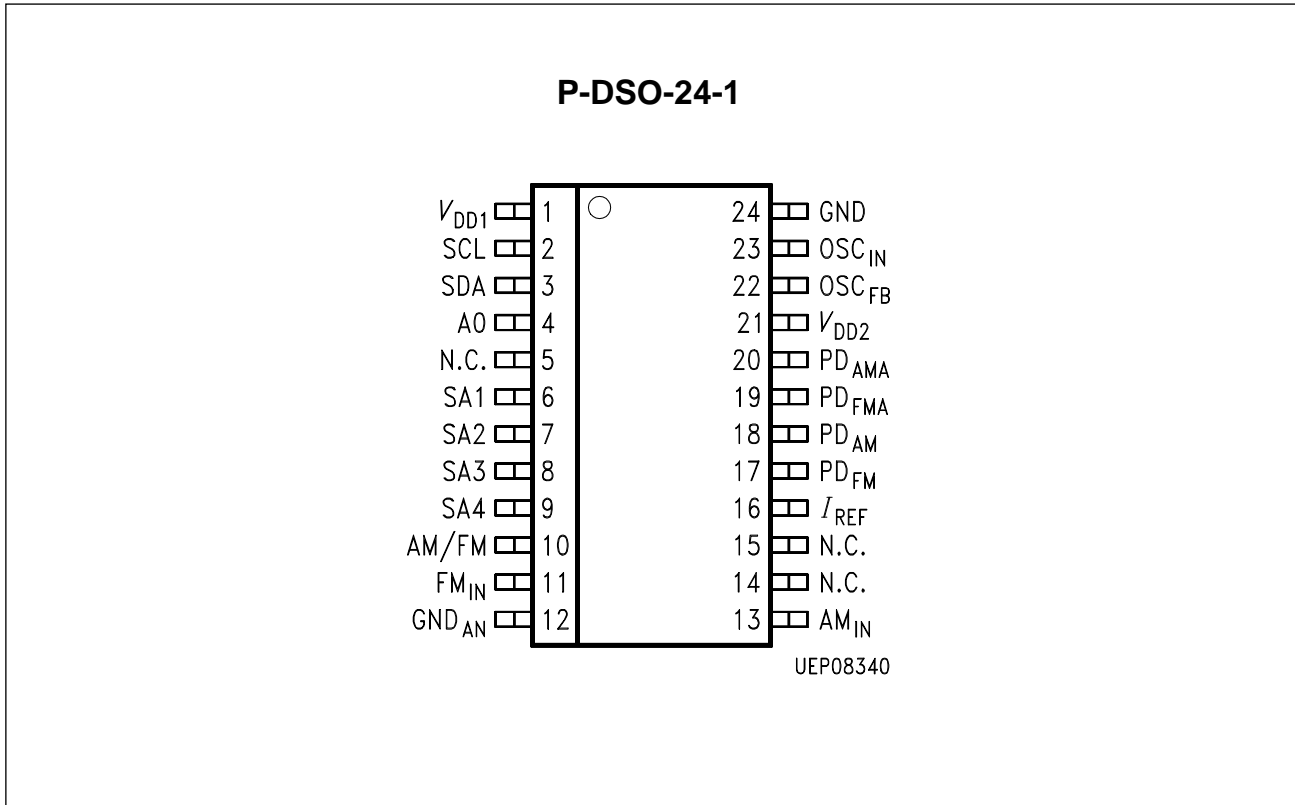


Figure 1

#### 1.4 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
1	$V_{DD1}$		Supply voltage digital (5 V)
2	SCL	I	Clock I <sup>2</sup> C Bus
3	SDA	I/O	Data I <sup>2</sup> C Bus
4	A0	I	Address selection, sets the LSB of the IC-address
5	N.C.		
6 ... 9	SA1 ... SA4	O	10 V open drain output, controlled via I <sup>2</sup> C Bus
10	AM/FM	O	10 V open drain output, indicating the operation mode (H = AM)
11	FM <sub>IN</sub>	I	Input for the FM signal from VCO
12	GND <sub>AN</sub>		Ground analog
13	AM <sub>IN</sub>	I	Input for the AM signal from VCO
14	N.C.		
15	N.C.		
16	$I_{REF}$	I	Reference current, setting the base current level for the charge pumps
17	PD <sub>FM</sub>	O	FM charge pump output
18	PD <sub>AM</sub>	O	AM charge pump output
19	PD <sub>FMA</sub>	O	Source follower output FM
20	PD <sub>AMA</sub>	O	Source follower output AM
21	$V_{DD2}$		Supply voltage digital for charge pump and source followers (up to 10 V)
22	OSC <sub>FB</sub>	I/O	Oscillator feedback, quartz terminal
23	OSC <sub>IN</sub>	I	Oscillator input, quartz terminal, optionally input for external reference
24	GND		Ground digital

1.5 Functional Block Diagram

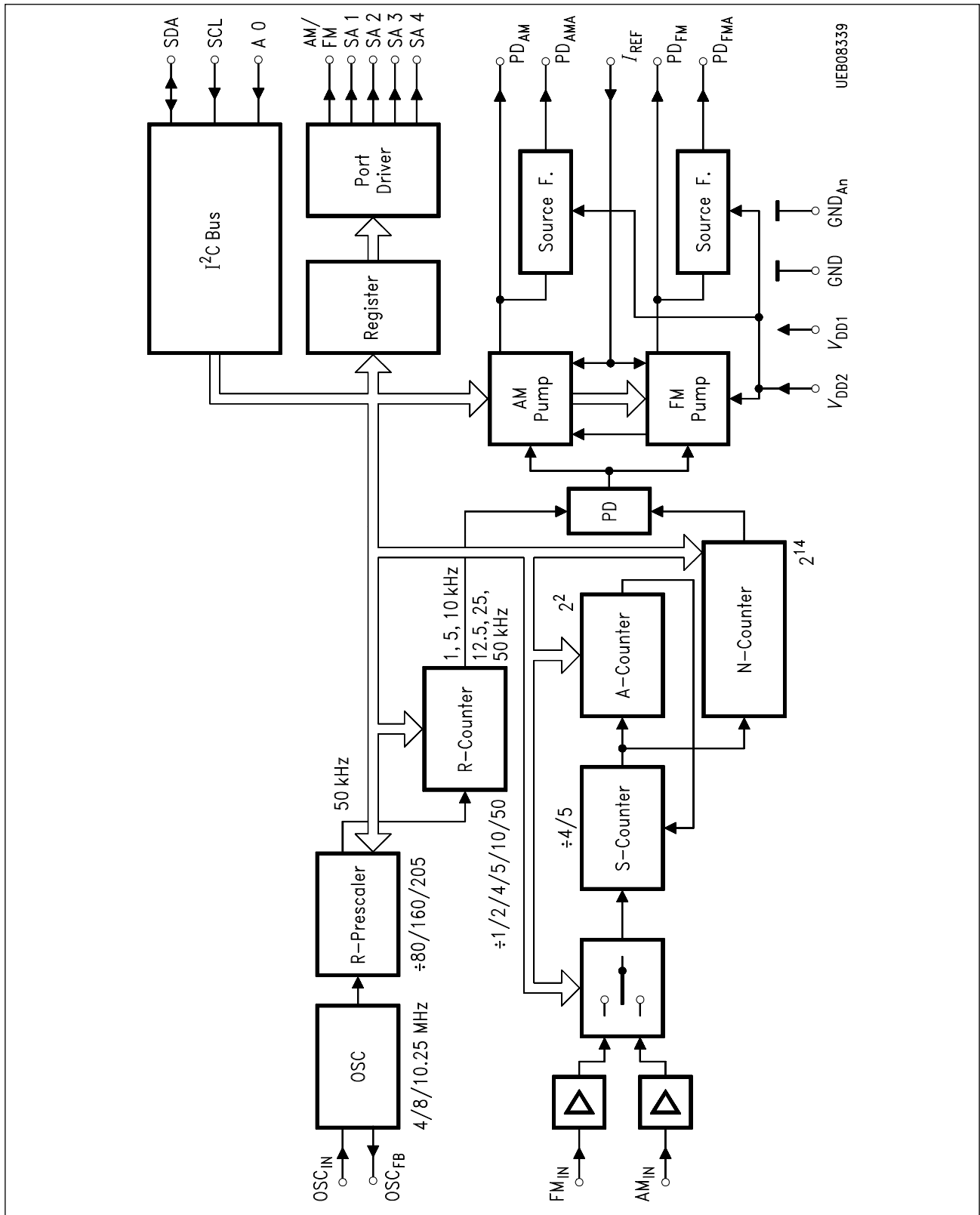


Figure 2  
Block Diagram

## 2 Functional Description

The SDA 4331X is a radio PLL controlled via I<sup>2</sup>C Bus for frequency synthesis in the AM and FM range.

## 3 Circuit Description

The reference frequency for the PLL is derived from the quartz oscillator OSC<sup>1)</sup>. The R-prescaler can be adapted to quartz frequencies of 4, 8 or 10.25 MHz, respectively, yielding an internal 50 kHz reference. Programming the R-counter sets the phase detector reference frequency to 1, 5 or 10 kHz in the AM mode or to 12.5, 25 or 50 kHz in the FM mode. The VCO frequency is set by programming the A/N-counter which operates as dual-modulus counter for FM and AM using a divide by 4/5 swallow counter.

The phase detector drives two different charge pumps for AM and FM mode. Additional source followers are connected to the charge pump. There are four programmable current levels for each charge pump. The supply voltage for the charge pump and the source followers is supplied via the V<sub>DD2</sub> pin and can reach 10 V maximum. AM/FM is an open drain output as well as the additional outputs SA1 ... SA4 which are controlled by I<sup>2</sup>C Bus.

The I<sup>2</sup>C Bus interface provides slave receiver functions. There are two addresses selected by the A0 pin. The I<sup>2</sup>C-protocol (see **diagram 1**) contains one string for programming all counters and functions. The transfer may be stopped optionally after each word if the remaining functions are not to be altered. After power ON all control signals are undefined, so that the complete write sequence must be executed.

<sup>1)</sup> The power dissipation of the quartz is given by:

$$P_V = 2 \times R_1 (\Pi \times f_Q \times (C_O + C_L) \times V_{DD})^2$$

R<sub>1</sub> ... Series resistance of the quartz

f<sub>Q</sub> ... Quartz frequency

C<sub>O</sub> ... Parallel capacitance of the quartz

C<sub>L</sub> ... Load capacitance, including input capacitance of the IC

## 4 Electrical Characteristics

### 4.1 Absolute Maximum Ratings

$T_A = -25\text{ °C to }85\text{ °C}$

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	$V_{DD1}$	- 0.3	6	V	
Supply voltage	$V_{DD2}$	- 0.3	10.5	V	
Input voltage	$V_{IN}$	- 0.3	$V_{DD1} + 0.3$	V	
Power dissipation per output	$P_Q$		10	mW	
Power dissipation	$P_{tot}$		t.b.d.	mW	
Storage temperature	$T_S$	- 40	125	°C	
Output voltage SA1 ... SA4, AM/FM	$V_{QH}$		10.5	V	
ESD voltage (HBM: 1.5 kΩ, 100 pF)	$V_{ESD}$	- 1	1	kV	

*Note: Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.*

### 4.2 Operational Range

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	$V_{DD1}$	4.5	5	5.5	V
Supply voltage	$V_{DD2}$	9		10.3	V
Supply current	$I_{DD1}$		4	10	mA
Supply current <sup>1)</sup>	$I_{DD2}$			0.5	mA
Ambient temperature	$T_A$	- 25		+ 85	°C
Output voltage SA1 ... SA4, AM/FM	$V_{QH}$			$V_{DD2}$	V

<sup>1)</sup> Measurement conditions: No load on pins 17 ... 20.

*Note: In the operating range the functions given in the circuit description are fulfilled.*

4.3 AC/DC Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Input AM<sub>IN</sub>**

Input voltage (sine wave)	$V_{IN}$	30			mVeff	$V_{DD1} = 4.5 V$ $0.5 MHz < f_{IN} < 40 MHz$
Input capacitance	$C$			4	pF	
Input current	$I_{IN}$	- 50		50	μA	$0 \leq V_{IN} \leq V_{DD1}$

**Input FM<sub>IN</sub>**

Input voltage (sine wave)	$V_{IN}$	50 120			mVeff mVeff	$V_{DD1} = 4.5 V$ $20 MHz < f_{IN} < 120 MHz$ $10 MHz < f_{IN} < 155 MHz$
Input capacitance	$C$			4	pF	
Input current	$I_{IN}$	- 100		100	μA	$0 \leq V_{IN} \leq V_{DD1}$

**Input OSC<sub>IN</sub>**

Input voltage (sine wave)	$V_{IN}$	100 150 200			mVeff mVeff mVeff	$V_{DD1} = 4.5 V$ $f_{IN} = 4 MHz$ $f_{IN} = 8 MHz$ $f_{IN} = 10.25 MHz$
Input capacitance	$C$			10	pF	
Input current	$I_{IN}$	- 30		30	μA	$0 \leq V_Q \leq V_{DD1}$

**Input/Output SDA**

H-input voltage	$V_{IH}$	$0.7 \times V_{DD1}$		$V_{DD1}$	V	
L-input voltage	$V_{IL}$	0		$0.3 \times V_{DD1}$	V	
L-output voltage	$V_{QL}$			0.4	V	$I_{QL} = 3 mA, V_{DD1} = 5 V,$ $C_L = 400 pF$
Input leakage current	$I_{Leakage}$	- 10		10	μA	$0 \leq V_{IN} \leq V_{DD1}$
Input capacitance	$C$			10	pF	

4.3 AC/DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Inputs SCL, A0

H-input voltage	$V_{IH}$	$0.7 \times V_{DD1}$		$V_{DD1}$	V	
L-input voltage	$V_{IL}$	0		$0.3 \times V_{DD1}$	V	
Input leakage current	$I_{Leakage}$	- 10		10	$\mu A$	$0 \leq V_{IN} \leq V_{DD1}$
Input capacitance	$C$			10	pF	

Outputs SA1, SA2, SA3, SA4, AM/FM (open drain outputs)

L-output voltage	$V_{QL}$			0.4	V	$I_{QL} = 1 \text{ mA}$ $V_{DD1} = 5 \text{ V}$ $I_{QL} = 0.1 \text{ mA}$
	$V_{QL}$			0.1	V	

Input  $I_{REF}$

Input current	$I_{IN}$	t.b.d.	100	t.b.d.	$\mu A$	
Voltage at $I_{REF}$	$V_{IREF}$		1.2		V	$I_{IN} = 100 \mu A$

Output  $PD_{FM}$

PD current A	$I_Q$		$\pm 4.5$		mA	$V_{PD} = 4 \text{ V}$
PD current B	$I_Q$		$\pm 3$		mA	
PD current C	$I_Q$		$\pm 1.5$		mA	
PD current D	$I_Q$		$\pm 150$		$\mu A$	

Output  $PD_{AM}$

PD current A	$I_Q$		$\pm 450$		$\mu A$	$V_{PD} = 4 \text{ V}$
PD current B	$I_Q$		$\pm 300$		$\mu A$	
PD current C	$I_Q$		$\pm 150$		$\mu A$	
PD current D	$I_Q$		$\pm 30$		$\mu A$	



4.3 AC/DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Output PD<sub>FMA</sub>

H-output voltage	$V_{QH}$	7.5	7.7		V	$I_{QH} = 2 \text{ mA}$ $V_{PD\text{ FM}} = V_{DD2} = 9 \text{ V}$
H-output current	$I_{QH}$		2	5	mA	$V_{PD\text{ FM}} = V_{DD2} = 9 \text{ V}$
L-output current	$I_{QL}$	10			$\mu\text{A}$	$V_{PD\text{ FM}} = \text{GND}$ $V_Q = 4 \text{ V}$

Output PD<sub>AMA</sub>

H-output voltage	$I_{QH}$		1	2.5	mA	$V_{PD\text{ AM}} = 5 \text{ V}$
L-output current	$I_{QL}$	0.1			mA	$V_{PD\text{ AM}} = \text{GND}$ $V_Q = 5 \text{ V}$

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at  $T_A = 25^\circ\text{C}$  and the given supply voltage.

Table 1  
Programming of Mode and Frequency Resolution

AM/FM	R1	R0	Mode	Frequency Resolution [MHz]
0	0	1	FM	12.5
0	1	0	FM	25
0	1	1	FM	50
1	0	1	AM	1
1	1	0	AM	5
1	1	1	AM	10

**Table 2**  
**Programming R-prescaler**

RP1	RP0	Divide Ratio	Quartz Frequency [MHz]
0	0	1:1	Test mode only
0	1	1:80	4
1	0	1:160	8
1	1	1:205	10.25

**Table 3**  
**Programming Phase Detector**

PD1	PD0	Current Level
0	0	D
0	1	C
1	0	B
1	1	A

PPD	Polarity
0	Normal
1	Invers

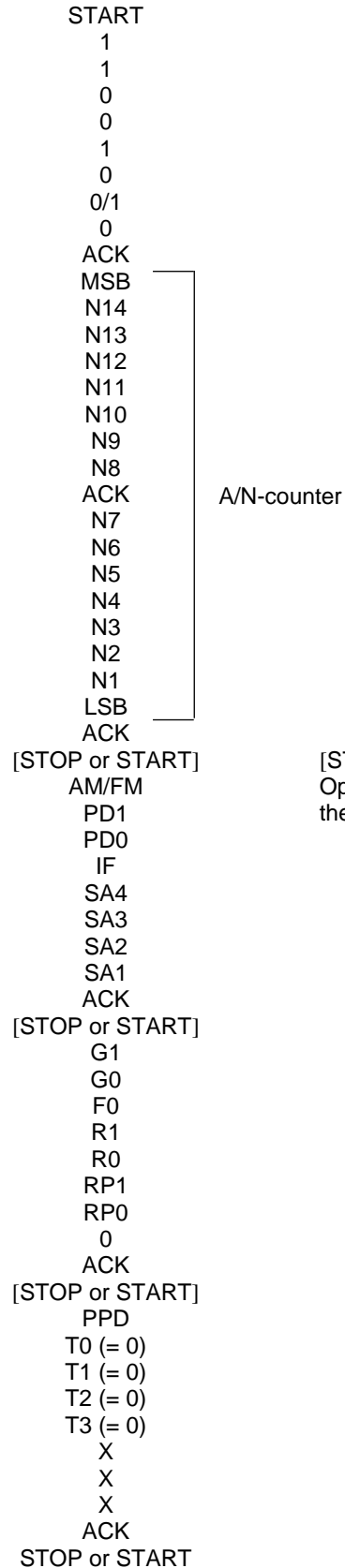
**Table 4**  
**Programming Test Mode**

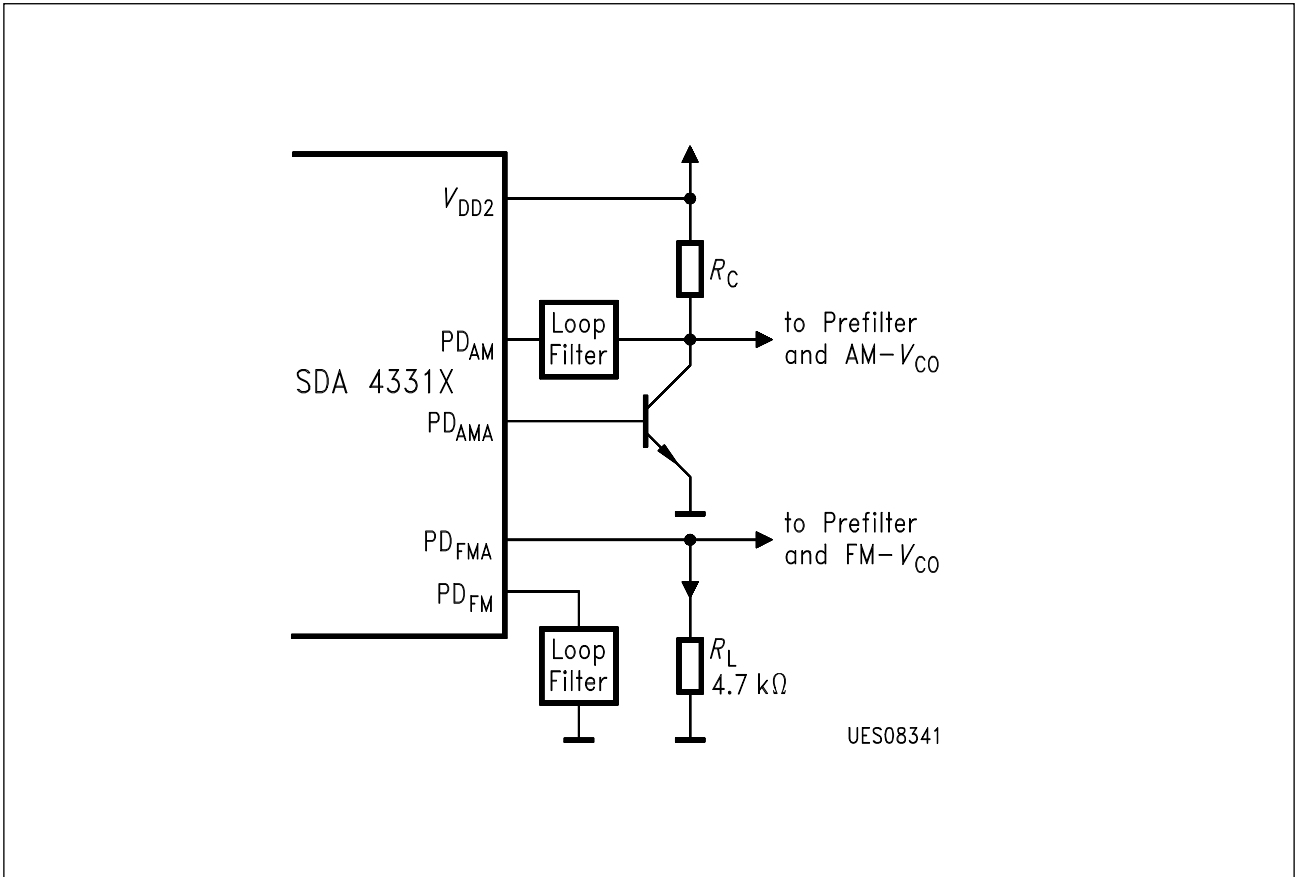
T1	T2	SA1	SA2	SA3	SA4
0	0	Controlled by I <sup>2</sup> C Bus			
1	0	PD_MUX	Clk_50 kHz	N_A_CLN	

T3	Operation
0	Normal
1	Test reset

## Diagram 1: I<sup>2</sup>C Protocol

Slave-receive (Write)

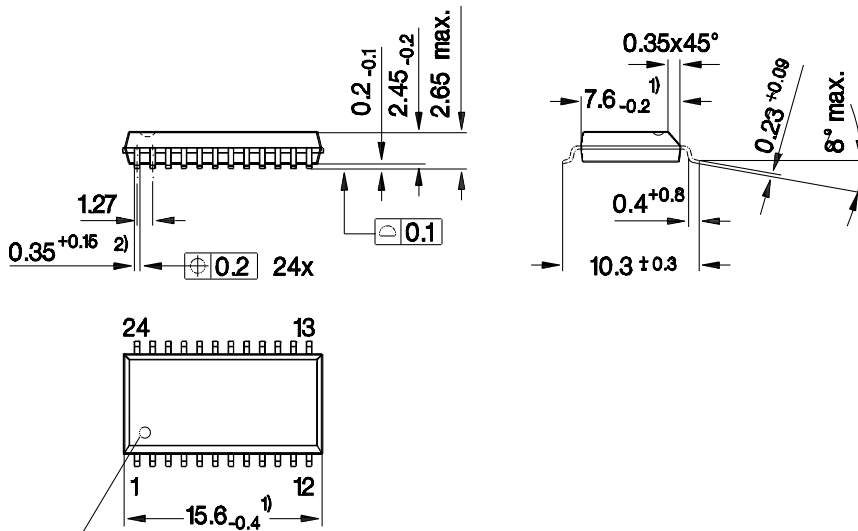




**Figure 3**  
**Application Circuit for AM and FM Charge Pump Output**

5 Package Outlines

**P-DSO-24-1**  
(Plastic Dual Small Outline Package)



Index Marking

- 1) Does not include plastic or metal protrusion of 0.15 max. per side
- 2) Does not include dambar protrusion

GPS05144

**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm