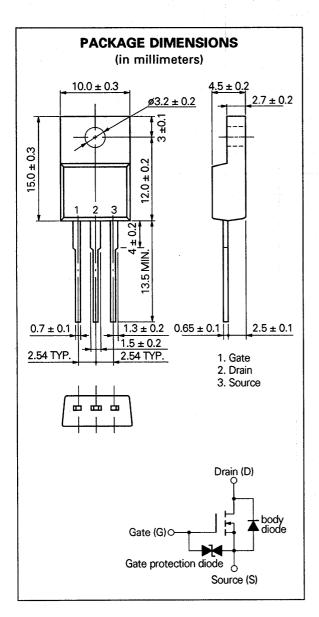


N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR 2SK1290

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE



DESCRIPTION

The 2SK1290 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

• Low On-state Resistance

RDS(on) \leq 45 m Ω MAX. (VGS = 10 V, ID = 13 A) RDS(on) \leq 60 m Ω MAX. (VGS = 4 V, ID = 13 A)

- Low Ciss Ciss = 2 200 pF TYP.
- Built-in G-S Gate Protection Diodes

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS

* PW \leq 10 μ s, Duty Cycle \leq 1 %

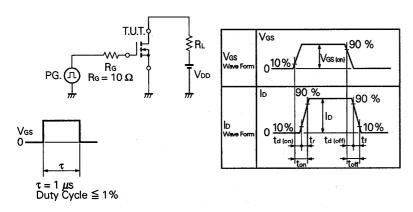
Maximum Te	mperatures		
Storage Te	mperature	-55 to +150	°C
Channel Te	emperature	150	°C MAX.
Maximum Po	wer Dissipation		
Total Powe	er Dissipation (Ta = 25 °C)	2.0	W
Total Powe	er Dissipation (Tc = 25 °C)	35	W
Maximum Vo	oltages and Currents (Ta = 25 °C)		
Voss	Drain to Source Voltage	60	V
Vgss(AC)	Gate to Source Voltage	±20	V
ID(DC)	Drain Current (DC)	±25	Α
D(pulse)*	Drain Current (pulse)	±100	Α



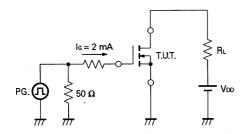
ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Drain to Source On-state Resistance	RDS(on)		35	45	mΩ	Vgs = 10 V, lp = 13 A	
Drain to Source On-state Resistance	RDS(on)		45	60	mΩ	Vgs = 4.0 V, lp = 13 A	
Gate to Source Cutoff Voltage	VGS(off)	1.0		2.5	V	V _{DS} = 10 V, I _D = 1 mA	
Forward Transfer Admittance	y _{fs}	12	25		s	V _{DS} = 10 V, I _D = 13 A	
Drain Leakage Current	loss			10	μΑ	Vps = 60 V, Vgs = 0	
Gate to Source Leakage Current	IGSS			±10	μΑ	Vgs = ±20 V, Vps = 0	
Input Capacitance	Ciss		2 200		pF	V _{DS} = 10 V V _{GS} = 0 f = 1 MHz	
Output Capacitance	Coss		750		pF		
Reverse Transfer Capacitance	Cres		180		pF		
Turn-On Delay Time	td(on)		30		ns	V _{GS(on)} = 10 V V _{DD} = 30 V I _D = 15 A, R _G = 10 Ω	
Rise Time	tr td(off)		240		ns ns		
Turn-Off Delay Time							
Fall Time	tr		140		ns	$R_L = 2.0 \Omega$	
Total Gate Charge	QG		50		nC	V _{GS} = 10 V I _D = 30 A	
Gate to Source Charge	Qgs		10		· nC		
Gate to Drain Charge	QgD		10		nC	VDD = 48 V	
Diode Forward Voltage	Vsp		1.1		V	IsD = 25 A, Vgs = 0	
Reverse Recovery Time	ţ _{rr}		130	:	ns	I _F = 30 A, V _{GS} = 0 di/dt = 50 A/μs	
Reverse Recovery Charge	Qrr		220		nC		

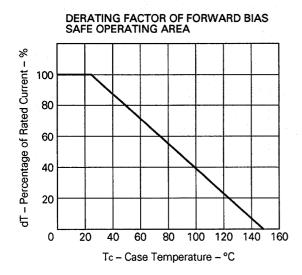
Test Circuit 1: Switching Time

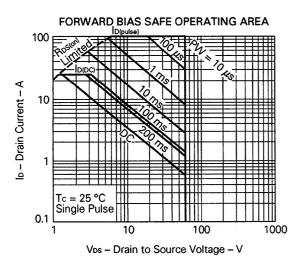


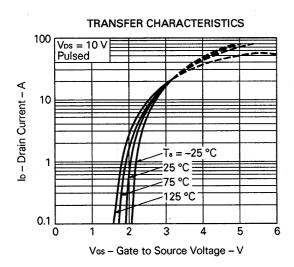
Test Circuit 2: Gate Charge

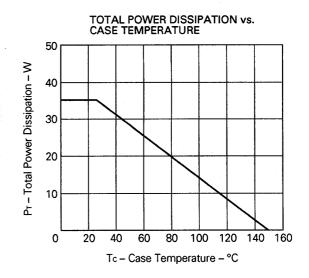


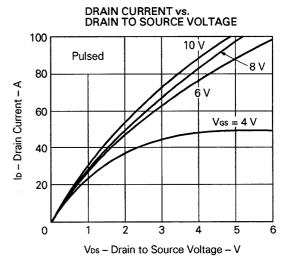
TYPICAL CHARACTERISTICS (Ta = 25 °C)

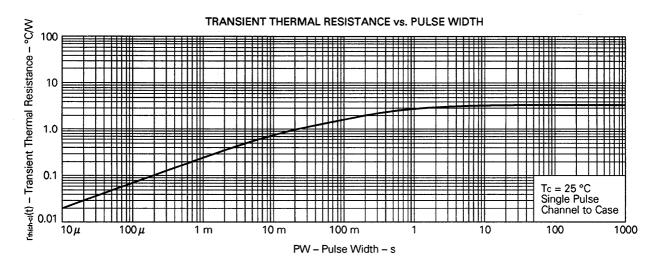


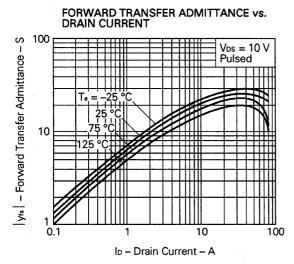


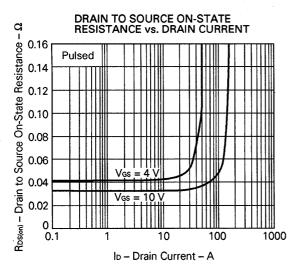


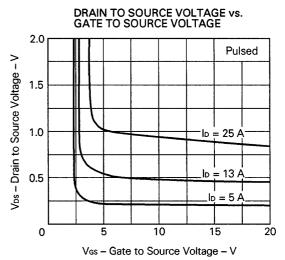


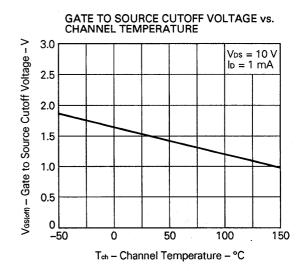


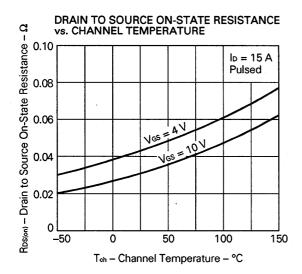


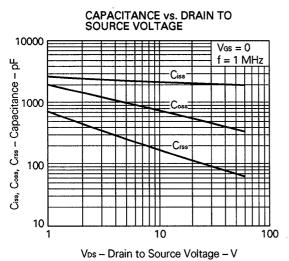


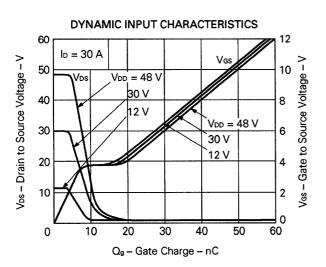


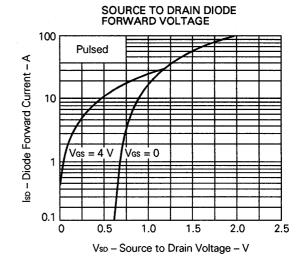


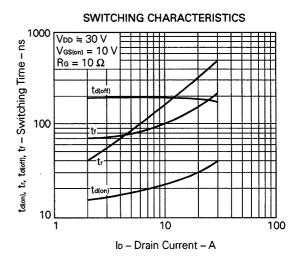


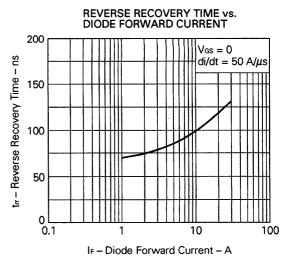












Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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