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# FDC6333C

## 30V N & P-Channel PowerTrench<sup>®</sup> MOSFETs

### General Description

These N & P-Channel MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

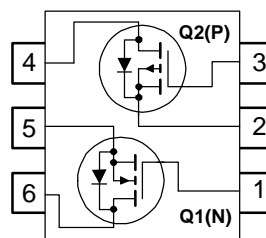
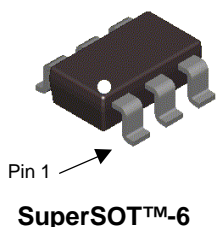
These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive SO-8 and TSSOP-8 packages are impractical.

### Applications

- DC/DC converter
- Load switch
- LCD display inverter

### Features

- **Q1** 2.5 A, 30V.  $R_{DS(ON)} = 95 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$   
 $R_{DS(ON)} = 150 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
- **Q2** -2.0 A, 30V.  $R_{DS(ON)} = 150 \text{ m}\Omega @ V_{GS} = -10 \text{ V}$   
 $R_{DS(ON)} = 220 \text{ m}\Omega @ V_{GS} = -4.5 \text{ V}$
- Low gate charge
- High performance trench technology for extremely low  $R_{DS(ON)}$ .
- SuperSOT -6 package: small footprint (72% smaller than SO-8); low profile (1mm thick).



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V <sub>DSS</sub>	Drain-Source Voltage	30	-30	V
V <sub>GSS</sub>	Gate-Source Voltage	±16	±25	V
I <sub>D</sub>	Drain Current – Continuous (Note 1a)	2.5	-2.0	A
	– Pulsed	8	-8	
P <sub>D</sub>	Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c)	0.96		W
		0.9		
		0.7		
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +150		°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	130	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	60	°C/W

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.333	FDC6333C	7"	8mm	3000 units

### Electrical Characteristics

T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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#### Off Characteristics

BV <sub>DSS</sub>	Drain–Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA V <sub>GS</sub> = 0 V, I <sub>D</sub> = –250 μA	Q1 Q2	30 –30		V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Ref. to 25°C I <sub>D</sub> = –250 μA, Ref. to 25°C	Q1 Q2		27 –22	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V V <sub>DS</sub> = –24 V, V <sub>GS</sub> = 0 V	Q1 Q2		1 –1	μA
I <sub>GSSF</sub>	Gate–Body Leakage, Forward	V <sub>GS</sub> = 16 V, V <sub>DS</sub> = 0 V V <sub>GS</sub> = 25 V, V <sub>DS</sub> = 0 V	Q1 Q2		100 100	nA
I <sub>GSSR</sub>	Gate–Body Leakage, Reverse	V <sub>GS</sub> = –16 V, V <sub>DS</sub> = 0 V V <sub>GS</sub> = –25 V, V <sub>DS</sub> = 0 V	Q1 Q2		–100 –100	nA

#### On Characteristics (Note 2)

V <sub>GS(th)</sub>	Gate Threshold Voltage	Q1	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1	1.8	3	V
		Q2	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = –250 μA	–1	–1.8	–3	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	Q1	I <sub>D</sub> = 250 μA, Ref. To 25°C		4		mV/°C
		Q2	I <sub>D</sub> = –250 μA, Ref. to 25°C		–4		
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	Q1	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.5 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2.0 A V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.5 A, T <sub>J</sub> = 125°C		73 90 106	95 150 148	mΩ
		Q2	V <sub>GS</sub> = –10 V, I <sub>D</sub> = –2.0 A V <sub>GS</sub> = –4.5 V, I <sub>D</sub> = –1.7 A V <sub>GS</sub> = 10 V, I <sub>D</sub> = –2.0 A, T <sub>J</sub> = 125°C		95 142 149	130 220 216	
I <sub>D(on)</sub>	On–State Drain Current	Q1	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 5 V	8			A
		Q2	V <sub>GS</sub> = –10 V, V <sub>DS</sub> = –5 V	–8			
g <sub>FS</sub>	Forward Transconductance	Q1	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 2.5 A		7		S
		Q2	V <sub>DS</sub> = –5 V, I <sub>D</sub> = –2.0 A		3		

#### Dynamic Characteristics

C <sub>iss</sub>	Input Capacitance	Q1	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		282		pF
		Q2	V <sub>DS</sub> = –15 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		185		
C <sub>oss</sub>	Output Capacitance	Q1	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		49		pF
		Q2	V <sub>DS</sub> = –15 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		56		
C <sub>rss</sub>	Reverse Transfer Capacitance	Q1	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		20		pF
		Q2	V <sub>DS</sub> = –15 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		26		

#### Switching Characteristics (Note 2)

t <sub>d(on)</sub>	Turn–On Delay Time	Q1	For Q1: V <sub>DS</sub> = 15 V, I <sub>DS</sub> = 1 A V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω		4.5	9	ns
		Q2			4.5	9	
t <sub>r</sub>	Turn–On Rise Time	Q1	For Q2: V <sub>DS</sub> = –15 V, I <sub>DS</sub> = –1 A V <sub>GS</sub> = –10 V, R <sub>GEN</sub> = 6 Ω		6	12	ns
		Q2			13	23	
t <sub>d(off)</sub>	Turn–Off Delay Time	Q1			19	34	ns
		Q2			11	20	
t <sub>f</sub>	Turn–Off Fall Time	Q1			1.5	3	ns
		Q2			2	4	
Q <sub>g</sub>	Total Gate Charge	Q1	For Q1: V <sub>DS</sub> = 15 V, I <sub>DS</sub> = 2.5 A V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω		4.7	6.6	nC
		Q2			4.1	5.7	
Q <sub>gs</sub>	Gate–Source Charge	Q1	For Q2: V <sub>DS</sub> = –15 V, I <sub>DS</sub> = –2.0 A V <sub>GS</sub> = –10 V,		0.9		nC
		Q2			0.8		
Q <sub>gd</sub>	Gate–Drain Charge	Q1			0.6		nC
		Q2			0.4		

### Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

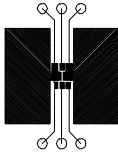
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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#### Drain–Source Diode Characteristics and Maximum Ratings

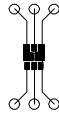
$I_S$	Maximum Continuous Drain–Source Diode Forward Current	Q1			0.8	A	
		Q2			-0.8		
$V_{SD}$	Drain–Source Diode Forward Voltage	Q1	$V_{GS} = 0\text{ V}, I_S = 0.8\text{ A}$ (Note 2)		0.8	1.2	V
		Q2	$V_{GS} = 0\text{ V}, I_S = 0.8\text{ A}$ (Note 2)		0.8	-1.2	

**Notes:**

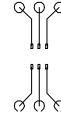
1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



- a)  $130^\circ\text{C/W}$  when mounted on a  $0.125\text{ in}^2$  pad of 2 oz. copper.



- b)  $140^\circ\text{C/W}$  when mounted on a  $.004\text{ in}^2$  pad of 2 oz copper



- c)  $180^\circ\text{C/W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width <  $300\mu\text{s}$ , Duty Cycle < 2.0%

Typical Characteristics: N-Channel

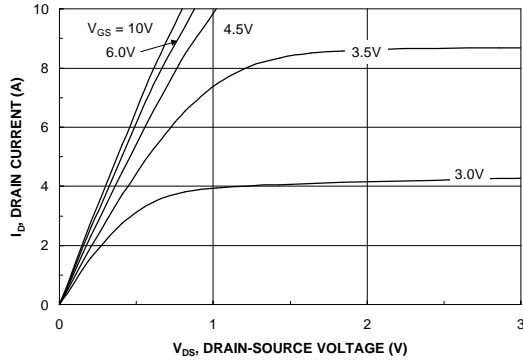


Figure 1. On-Region Characteristics.

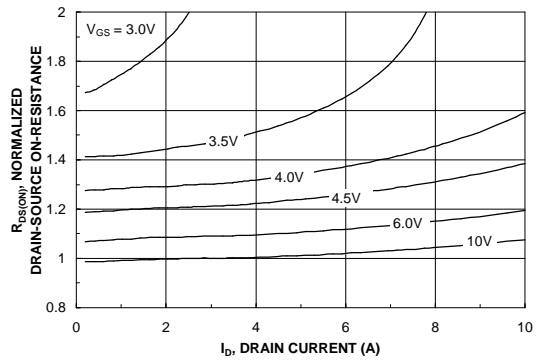


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

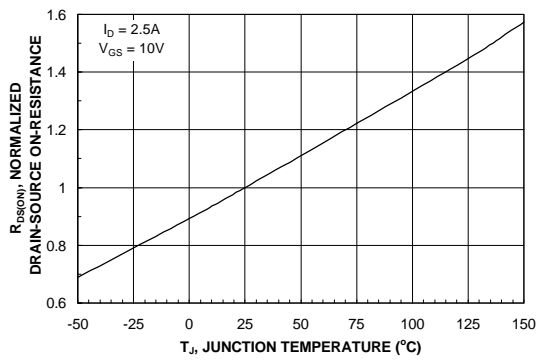


Figure 3. On-Resistance Variation with Temperature.

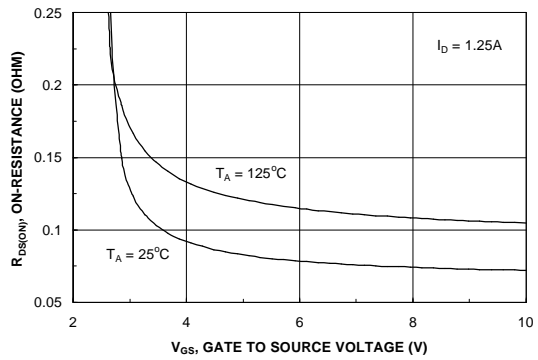


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

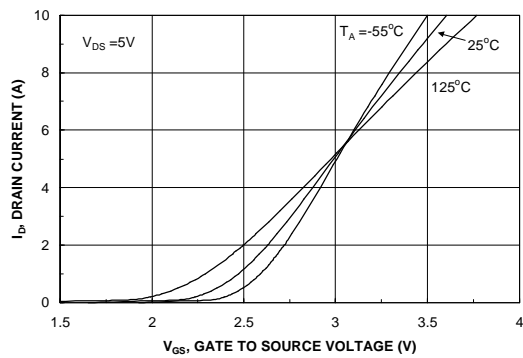


Figure 5. Transfer Characteristics.

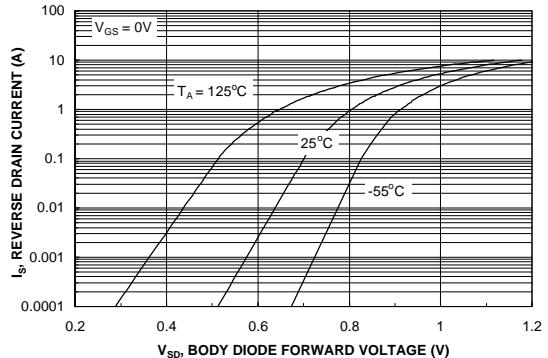


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: N-Channel (continued)

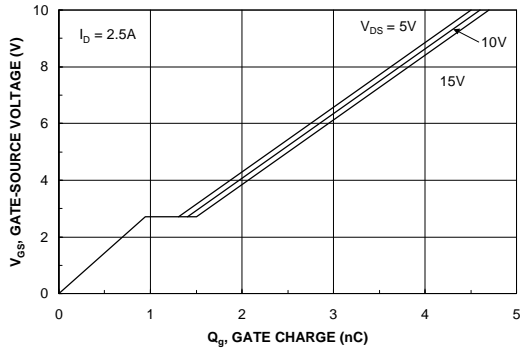


Figure 7. Gate Charge Characteristics.

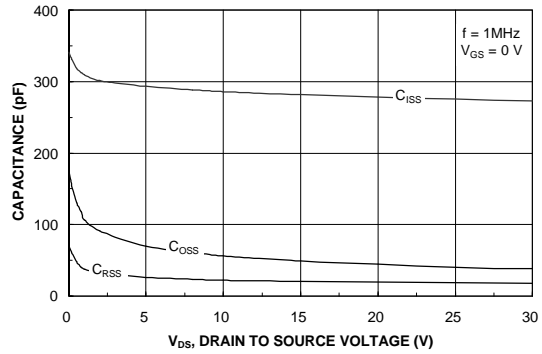


Figure 8. Capacitance Characteristics.

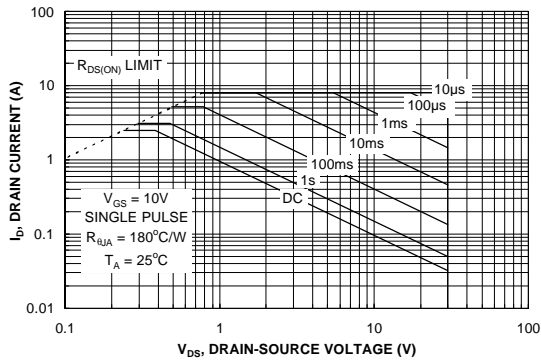


Figure 9. Maximum Safe Operating Area.

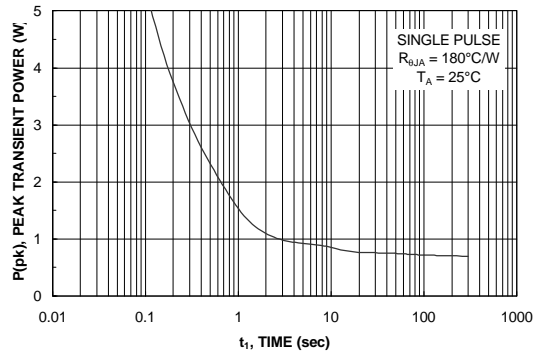


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: P-Channel

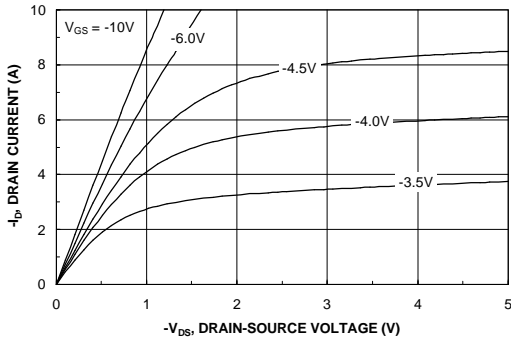


Figure 11. On-Region Characteristics.

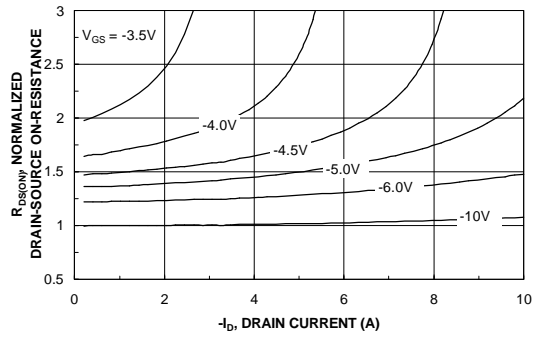


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

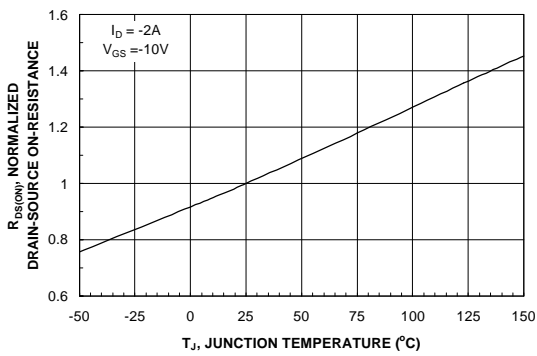


Figure 13. On-Resistance Variation with Temperature.

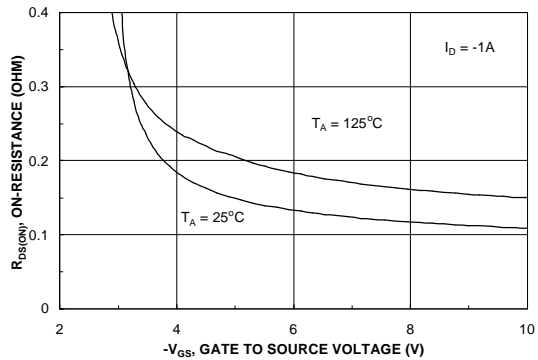


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

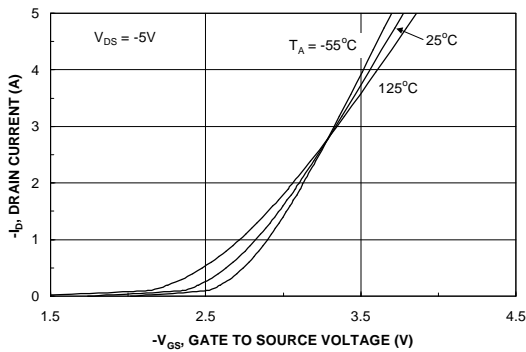


Figure 15. Transfer Characteristics.

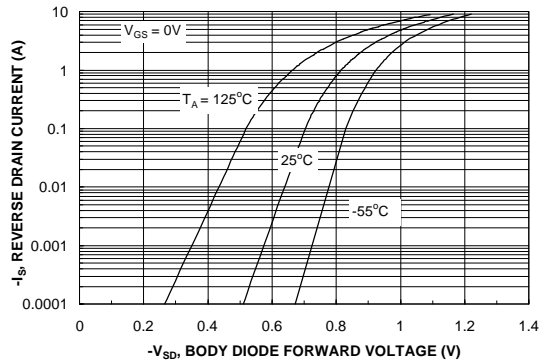
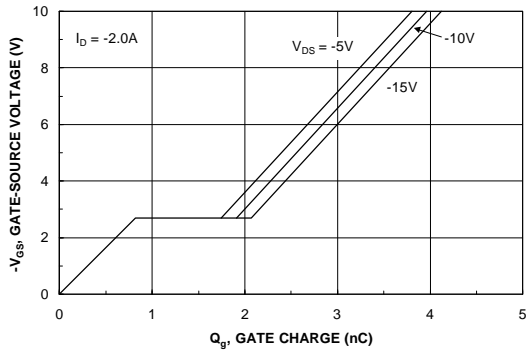
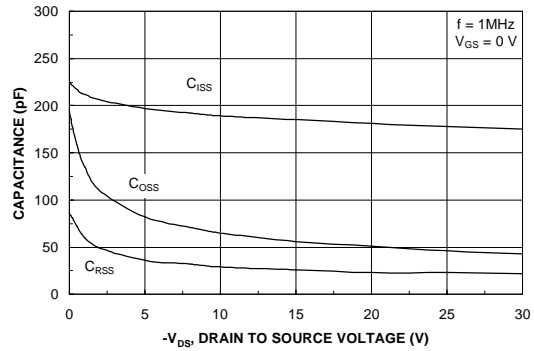


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

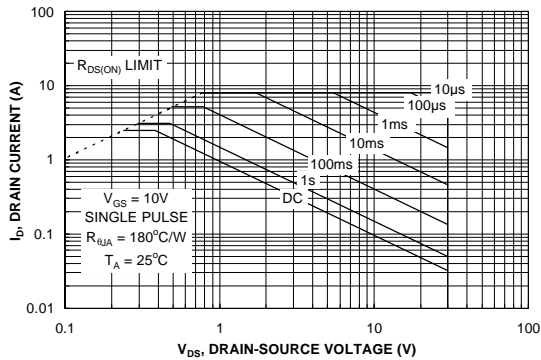
**Typical Characteristics: P-Channel** (continued)



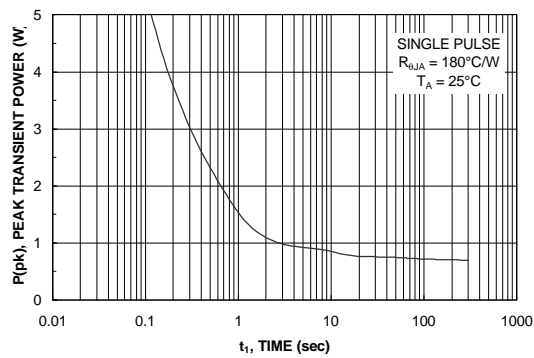
**Figure 17. Gate Charge Characteristics.**



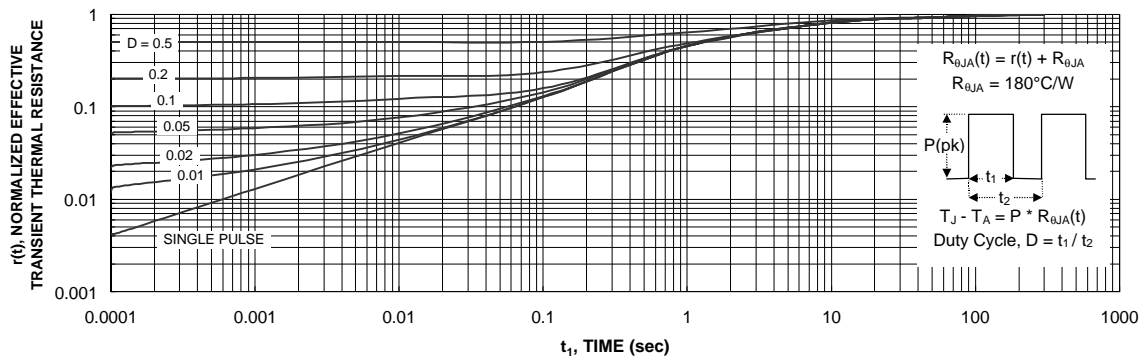
**Figure 18. Capacitance Characteristics.**



**Figure 19. Maximum Safe Operating Area.**



**Figure 20. Single Pulse Maximum Power Dissipation.**



**Figure 21. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c.  
Transient thermal response will change depending on the circuit board design.



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