M-Power 2A

MP2ASeries

Application Note (Ver.1.1)

Ver.1.1 2007.01.12

Contents

1. Outline

In recent years switching power supplies have been required to be not only compact and light weight but also to have low power consumption and a high power factor. A current resonant converter is applied, because it is superior to other topology from the viewpoint of low noise and efficiency. However at light loads efficiency is low and several watts of loss occur even at no load. This means that a sub-power supply is required at standby time which adds to the size of the unit.

Fuji Electric has utilized the advantages of the current resonant converter and developed a new multi-oscillated current resonant converter with controllability that allows easy power supply design (control method : combine PWM control and self-oscillated control).

The M-Power2A series of special power devices have been developed for the Converter. These multiple-chip power devices incorporate two-MOSFET and a special control IC in one package.

When the M-Power2A is used with the multi-oscillated current resonant converter, energy is conserved at standby mode without a sub-power supply. Also when the M-Power2A is combined with a PFC circuit, a switching power supply for high power factors can easily be designed.

2. Features

2-1 High efficiency, low noise

- Two-MOSFET (Q1, Q2) soft switching operation
- Low-noise secondary-side diode (No surge voltage at reverse recovery)
- Multi-oscillation means limited increase in frequency for light loads (Frequency increase of 20% of rated load for rated 10% load) and limited reactive power of transformer magnetizing current.

2-2 Fail-safe design: It is easy to construct a fail-safe power supply system.

- Protection functions with latch shutdown: Over current (OC), over voltage (OV), and over heating (OH).

3. Lineup

Type Name	MOS-FET (Q1)		MOS-FET (Q2)		Control IC	
	V_{DS}	R_{DS}(ON)	V_{DS}	R_{DS}(ON)	V_{CC}(ON)	Tj(OH)
MP2A5038	500V	0.38Ω	500V	0.38Ω	16.5V	125 ～ 150 ℃
MP2A5050	500V	0.5Ω	500V	0.5Ω		
MP2A5060	500V	0.6Ω	500V	0.6Ω		
MP2A5077	500V	0.77Ω	500V	0.77Ω		
MP2A2013	250V	0.125Ω	250V	0.125Ω		

4. Description of the multi-oscillated current resonant circuit

4-1 Description of basic circuit configuration and operation

1) Basic circuit configuration

Figure 1 shows the basic configuration of a multi-oscillated current resonant circuit that uses the M-Power2A. With this method current resonance is performed using the series resonant circuit of a leakage inductance of the transformer and capacitor Cr. The Q1 MOSFET performs PWM oscillation driven by the control IC and the Q2 MOSFET performs self-oscillation driven by the drive winding of the transformer Tr.

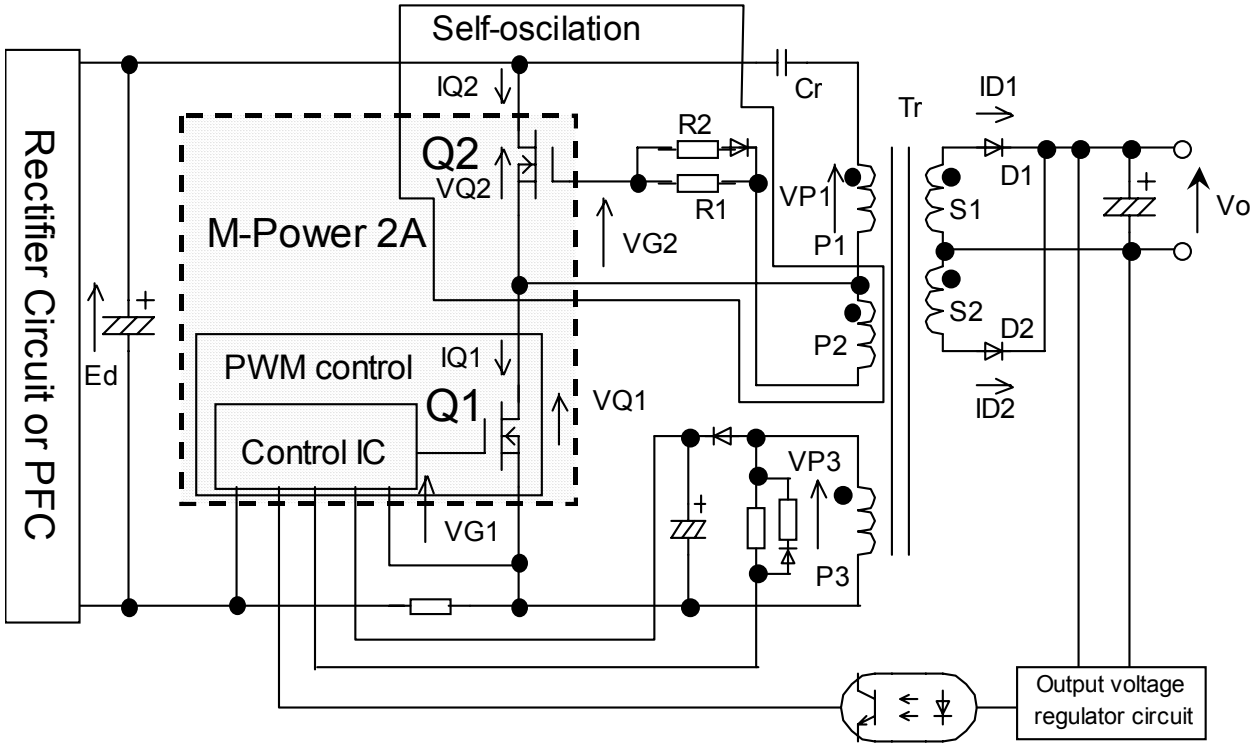


Fig.1 Basic Circuit Configuration

2) Operation

This section describes the operation of the multi-oscillated current resonant circuit.

Figure 2 shows the timing chart and Figure 3 shows the current path during periods I to VI.

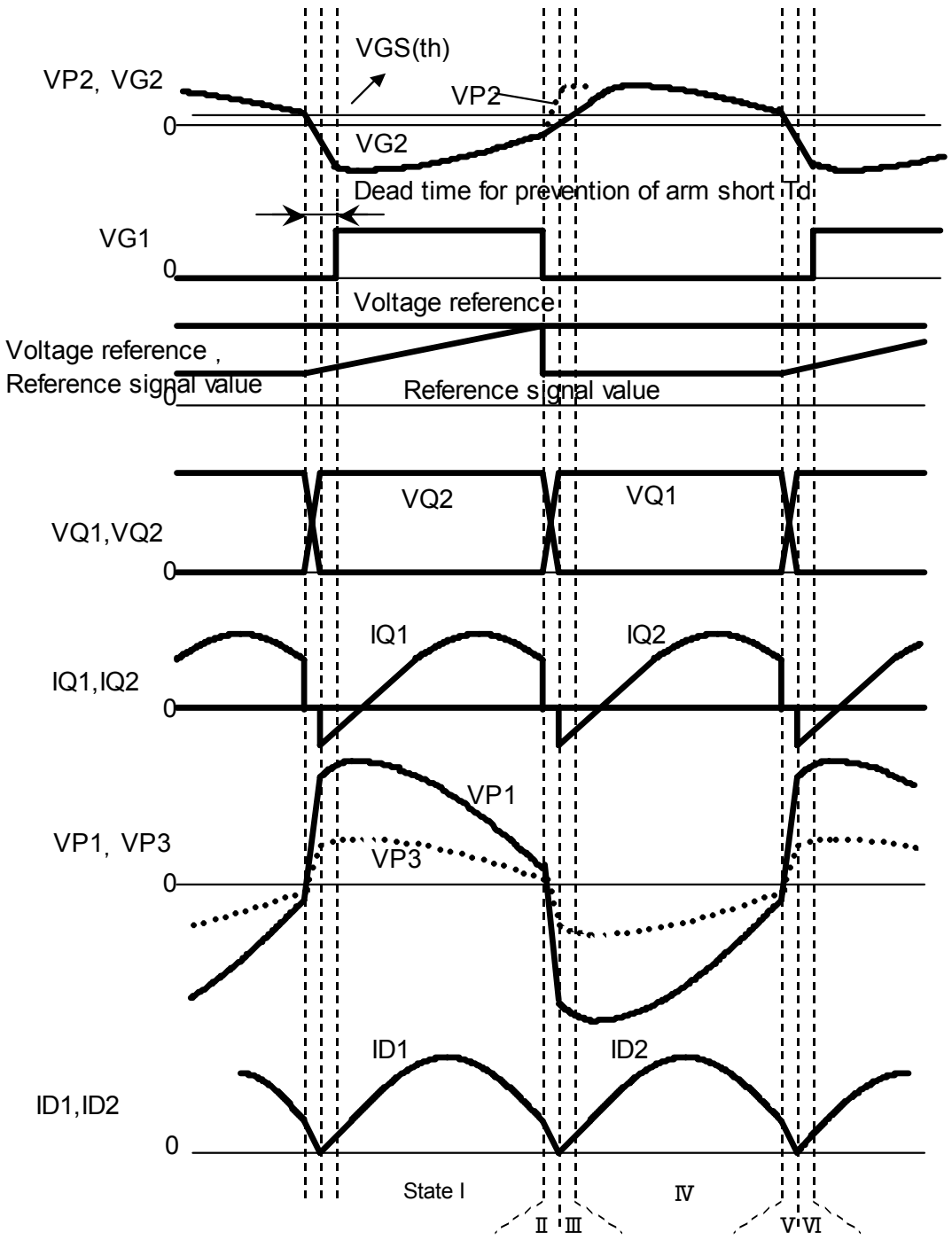


Fig.2 Timing Diagram

Figure 3 shows the current path during periods I to VI.

In Figures 3.1 to 3.6, capacitors CQ1 and CQ2 show the output capacity of Q1 and Q2, diodes Dq1 and Dq2 indicate the Q1 and Q2 body diodes, Lm indicates the T1 exciting inductance, and Rl indicates the load.

Ll indicates the inductance for the resonant current sent to the secondary side load and is included in the Figure 3 circuit drawings to assist the description of the operation in this section.

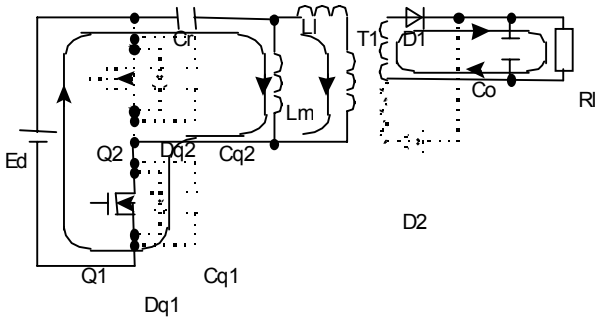


Fig.3.1 Current path at state I

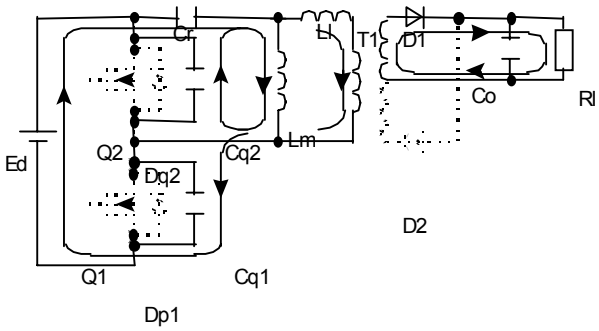


Fig.3.2 Current path at state II

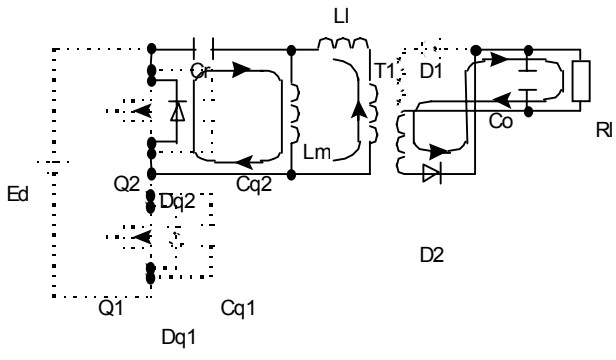


Fig.3.3 Current path at state III

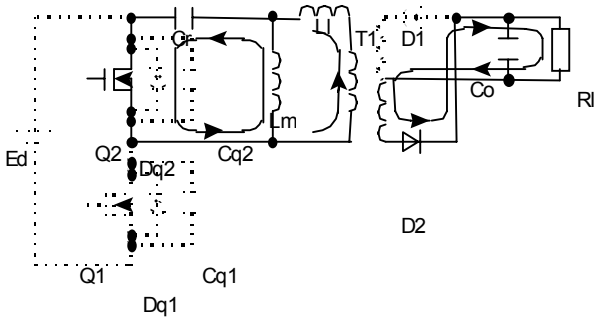


Fig.3.4 Current path at state IV

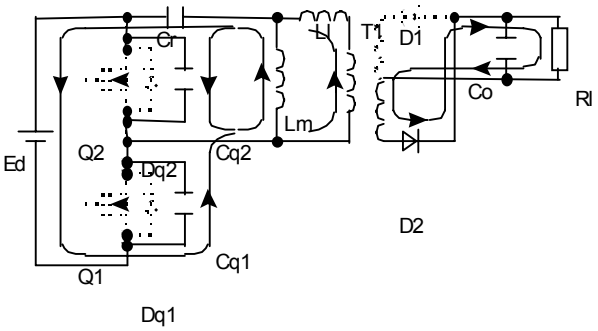


Fig.3.5 Current path at state V

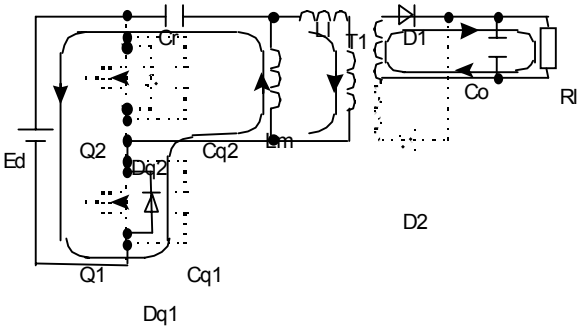


Fig.3.1 Current path at state VI

Fig. 3 Current path during period I to VI

Period I (Fig. 3.1)

Q1 is ON, Q2 is OFF, and the current flows through the circuit shown in solid lines in the diagram. If the currents that flows to Cr, LI, and Lm are indicated as I_{Cr}, I_{LI}, and I_{Lm}, equation (1) is true.

$I_{Cr} = I_{LI} + I_{Lm}$ …….. (1)

Equation (2) is true based on the product of ampere turns (At).

$N_{P1} \times I_{L1} = N_{S1} \times I_{D1}$ …. (2)

Np1: Number of P1 windings; Ns1: Number of S1 windings; I_{D1}: D1 current

Power continues to be supplied to the load and accumulates at LI and Lm.

Period II (Fig. 3.2)

When Q1 turns OFF, Cq1 is charged using the energy accumulated at LI and Lm and Cq2 is discharged. Equations (1) and (2) above and equations (3) and (4), below, are true during this period.

$I_{Cr} = I_{Cq1} + I_{Cq2}$ ….. (3)

$I_{Cq1} = I_{Cq2}$ ….. (4)

I_{Cq1}: Cq1 current; I_{Cq2}: Cq2 current

The rate of the Q1 voltage increase is restrained therefore, by the charging speed of Cq1 and the rate of the Q2 voltage decrease is restrained by the discharging speed of Cq2.

Period III (Fig. 3.3)

Dq2 conducts current when the Cq1 voltage reaches the DC bus voltage Ed and Cq2 reaches zero voltage, and the current flows through the path indicated in the figure 3.3. Therefore the Q2 voltage is clamped by Ed.

During this period, equations (1) and (2) above and equation (5), below, are true.

$I_{Cr} = I_{Dq2}$ ….. (5)

I_{Dq2}: Dq2 current

When current is flowing to Dq2, zero voltage switching (ZVS) operation is achieved by providing current to Q2.

Period IV (Fig. 3.4)

The transformer primary-side current is inverted and the current flows through the path indicated in Figure 3.4. Equations (1) and (2) hold even during this period.

Also, energy is accumulated at LI and Lm.

Period V (Fig. 3.5)

Q2 turns OFF, Cq1 is discharged, and Cq2 is charged by the energy accumulated at LI and Lm. Equations (1), (2), (3), and (4) are true during this period. Therefore, the rate of voltage decrease for Q1 is restrained by the discharging speed of Cq1 and the rate of voltage increase for Q2 is restrained by the charging speed of Cq2.

Period VI (Fig. 3.6)

Dq1 conducts current when Cq1 reaches zero voltage and Cq2 voltage reaches Ed. Therefore, Q1 voltage is clamped by Ed. During this period, equations (1), (2), and (6), below, are true.

$I_{Cr} = I_{Dq1}$ ….. (6)

I_{Dq1}: Dq1 current

When current is flowing to Dq1, zero voltage switching (ZVS) operation is achieved by turning ON Q1.

In other words, I_{Lm} current circulates around the primary side and the secondary side load is supplied at the secondary conversion value of the I_{LI} current.

5. Description of M-Power2A

5 - 1. Block diagram

Figure 4 shows the block diagram of the M-Power2A.

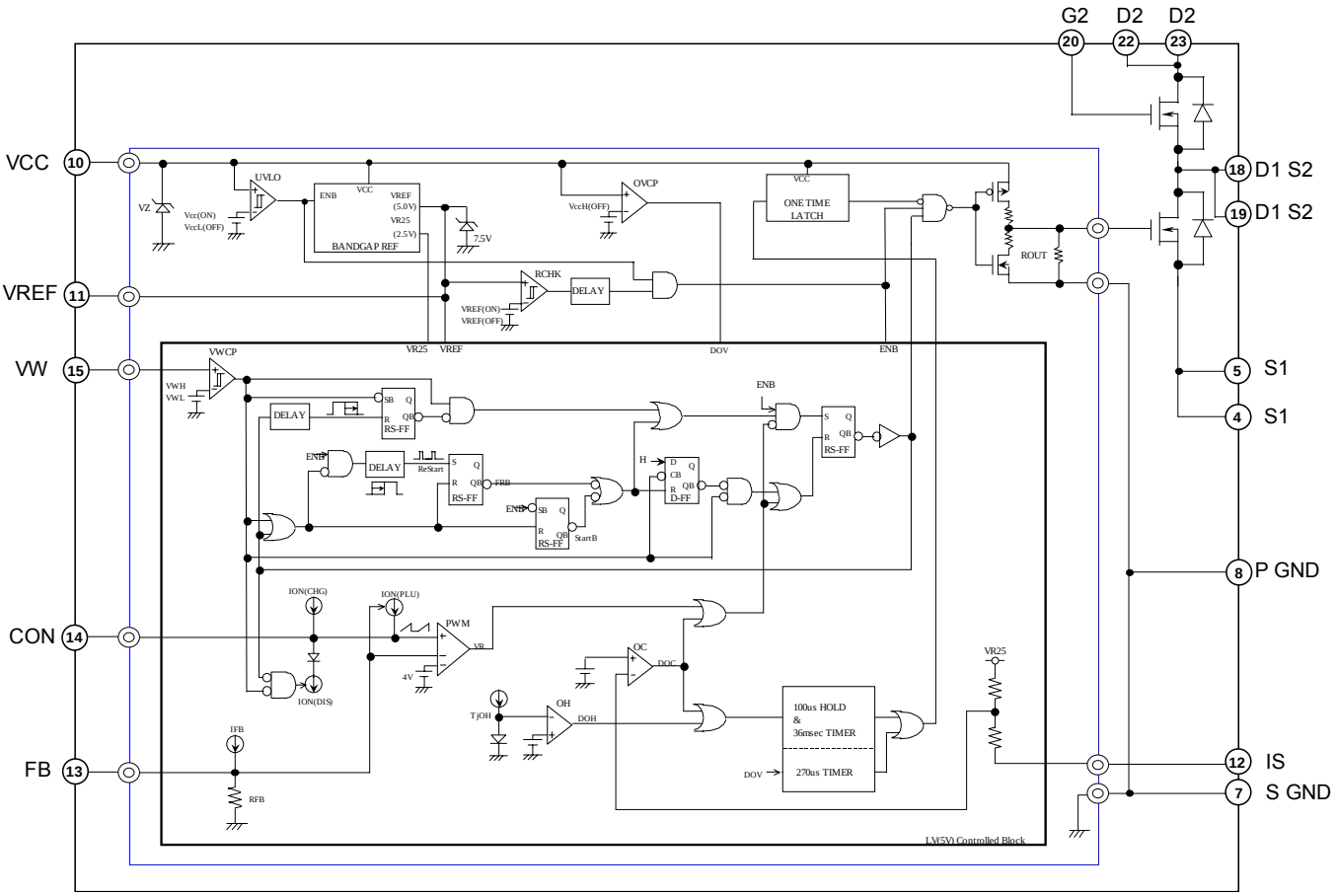
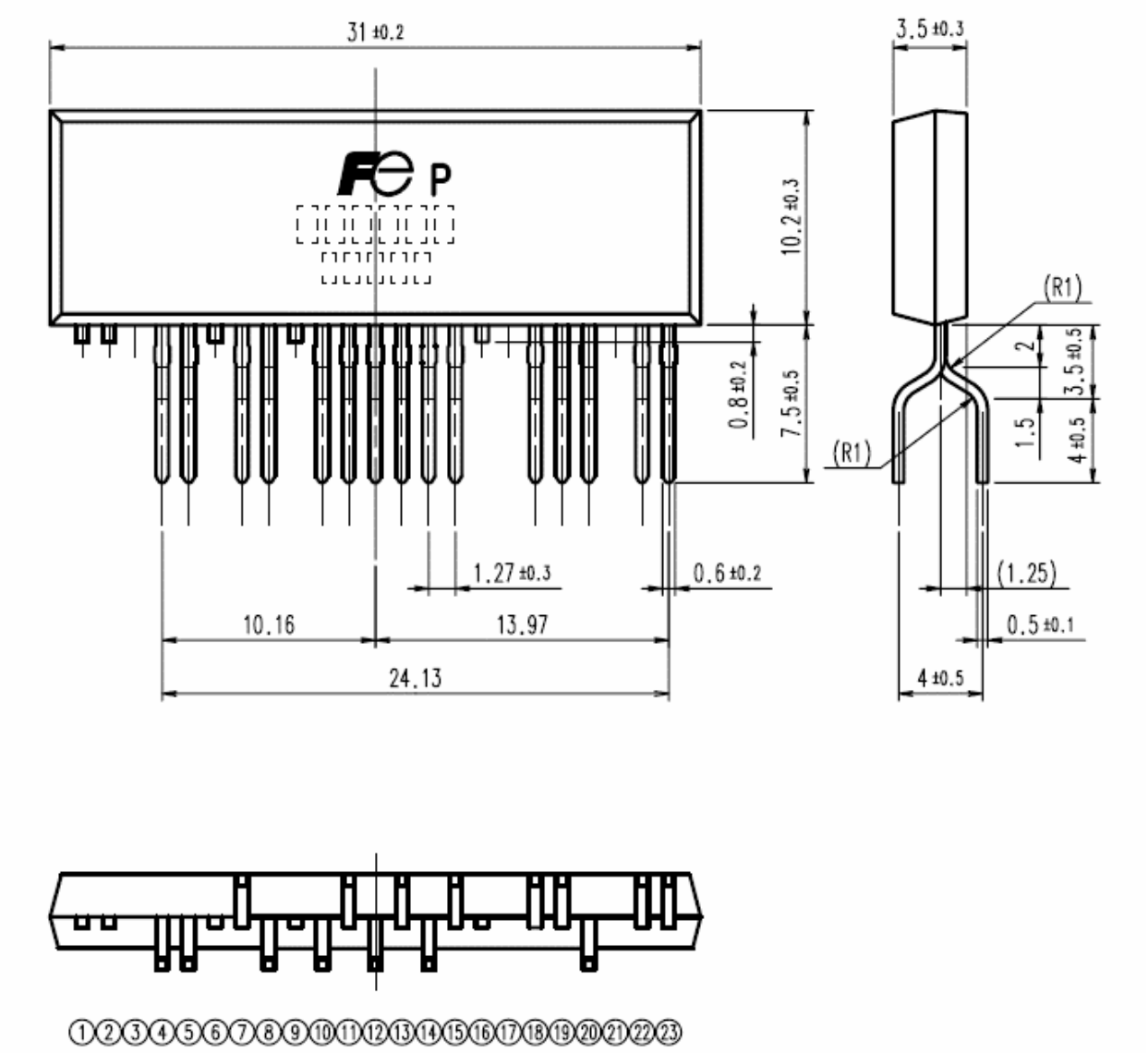


Fig. 4 M-Power 2A Block Diagram

5-2. External drawing

Figure 5 shows an external drawing of the M-Power2A.



Units: mm

Fig. 5 External Drawings: F219 Forming

5-3. Description of pin functions

Table 1 Pin Functions

Termainal	Symbol	Function
4, 5	S1	MOSFET (Q1) Source
7	S-GND	Signal-Ground (V_{REF}, FB, CON, VW)
8	P-GND	Power-Ground (V_{CC}, IS)
10	V_{CC}	Power Supply
11	V_{REF}	Reference Voltage Output
12	IS	Over Current Detection
13	FB	Feedback Signal Input for Constant Voltage Control
14	CON	Reference Oscillation of Q1 ON-time
15	VW	Q1 Turn on and off Timing Detection
18, 19	D1, S2	Q1 Drain and Q2 Source
20	G2	Q2 Gate
22, 23	D2	Q2 Drain

Note:

* Pins 3, 17, and 21 are cut.
* Pins 1, 2, 6, and 16 have no pin frames.
* Pin 9 is disconnected.

  This pin is connected to the Q1 gate but never connect it for waveform observation or any other purpose. Connection of the pin 9 could lead to major problems and could destroy the M-Power2A.

5-4. Circuit block descriptions

(1) Power supply control voltage

1) V_{CC}(ON) or less

To ensure that the IC is in a completely operable status before the internal IC outputs are enabled, two low-voltage lockout comparators, UVLO and RCHK, are built in to monitor the power supply voltage V_{CC} and the reference voltage VREF levels.

2) Vcc(ON): Operation startup voltage and startup current

The UVLO ON threshold $V_{CC(ON)}$ ranges between 15.5 and 17.5V. The switching operation starts when Vcc reaches $V_{CC(ON)}$. The current (Icc) flowing to the IC just prior to the start of IC operation is exceptionally small. Refer to the Vcc-Icc current diagram in the delivery specifications for details.

Item	Vcc voltage		
VccH(OFF)	↑ 28.0[V] ↓ 24.0[V]		
Normal Operation (Caution : IC Heating)	↑ 24.0[V]		
Normal Operation	↑ 22.0[V] ↓ 13.0[V]	↑ 17.5[V] ↓ 15.5[V]	Vcc(ON)
		↑ 9.9 [V] ↓ 7.9 [V]	VccL(OFF)
Vcc(LA)	↑ 4.1[V] ↓ 0.9[V]		

Fig. 6 Control Voltage and Operating Switching Points

3) $V_{CCL(OFF)}$: Operation stop (insufficient) voltage

The UVLO OFF threshold $V_{CCL(OFF)}$ ranges between 8.0 and 10.0V. This is the value of V_{CC} at which the switching operation is stopped when V_{CC} decreased from its value during operating status.

4) $V_{CC}H = V_{CC}(ON) - V_{CC}L(OFF)$: Hysteresis width

The threshold voltage to turn the UVLO ON and OFF has hysteresis. The hysteresis width is 7.5V (typical).

5) $V_{CCH(OFF)}$: Over voltage threshold voltage

$V_{CCH(OFF)}$ is the over voltage (OV) comparator threshold voltage and it is the value of V_{cc} at which a latched shutdown occurs when V_{cc} increases above this $V_{CCH(OFF)}$ value.

6) $V_{CC(LA)}$: Latch-stop Cancellation Voltage

$V_{cc(LA)}$ is the value of V_{CC} at which the latch is released when V_{CC} decreases after a latched shutdown has occurred for an over voltage or over current.

7) Zener Diode

A zener diode with a withstand voltage of approximately 30V is built-in between V_{cc} (pin 10) and S GND (pin 7) to protect the IC.

8) Recommended Operating Range

The recommended V_{CC} range for normal operation is 19.0 to 20.0V

9) Current consumption

The current consumption depends on the model, V_{CC} (pin 10) voltage, operating frequency, and operating status (normal operation or latched operation). Refer to the Vcc-Icc and Fc-Icc diagrams in the delivery specifications for your model for details.

（2）Q1 Pulse width control circuit

Figure 7 shows a schematic block diagram of the Q1 drive circuit and Figure 8 shows the Q1 pulse width controlled timing chart.

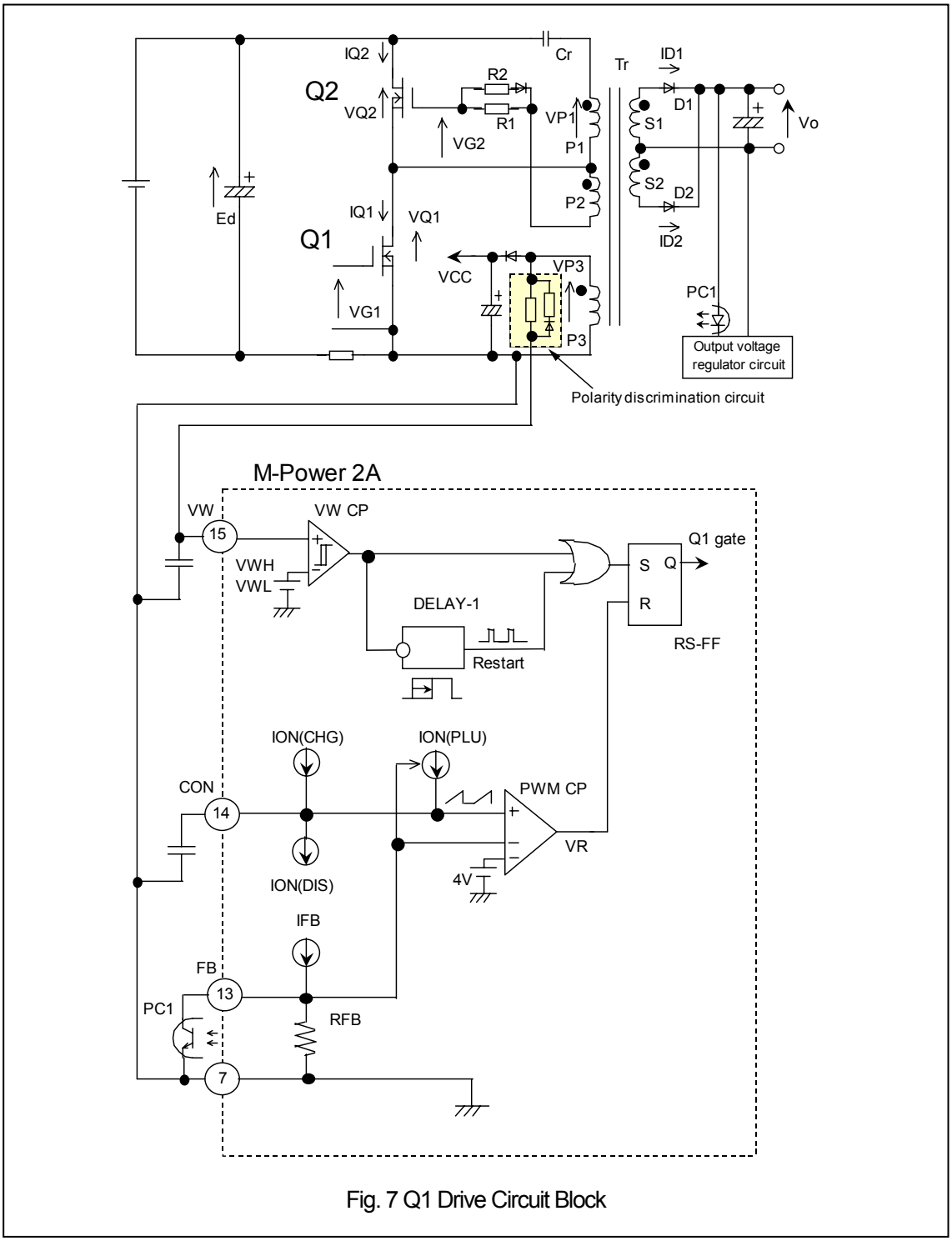


Fig. 7 Q1 Drive Circuit Block

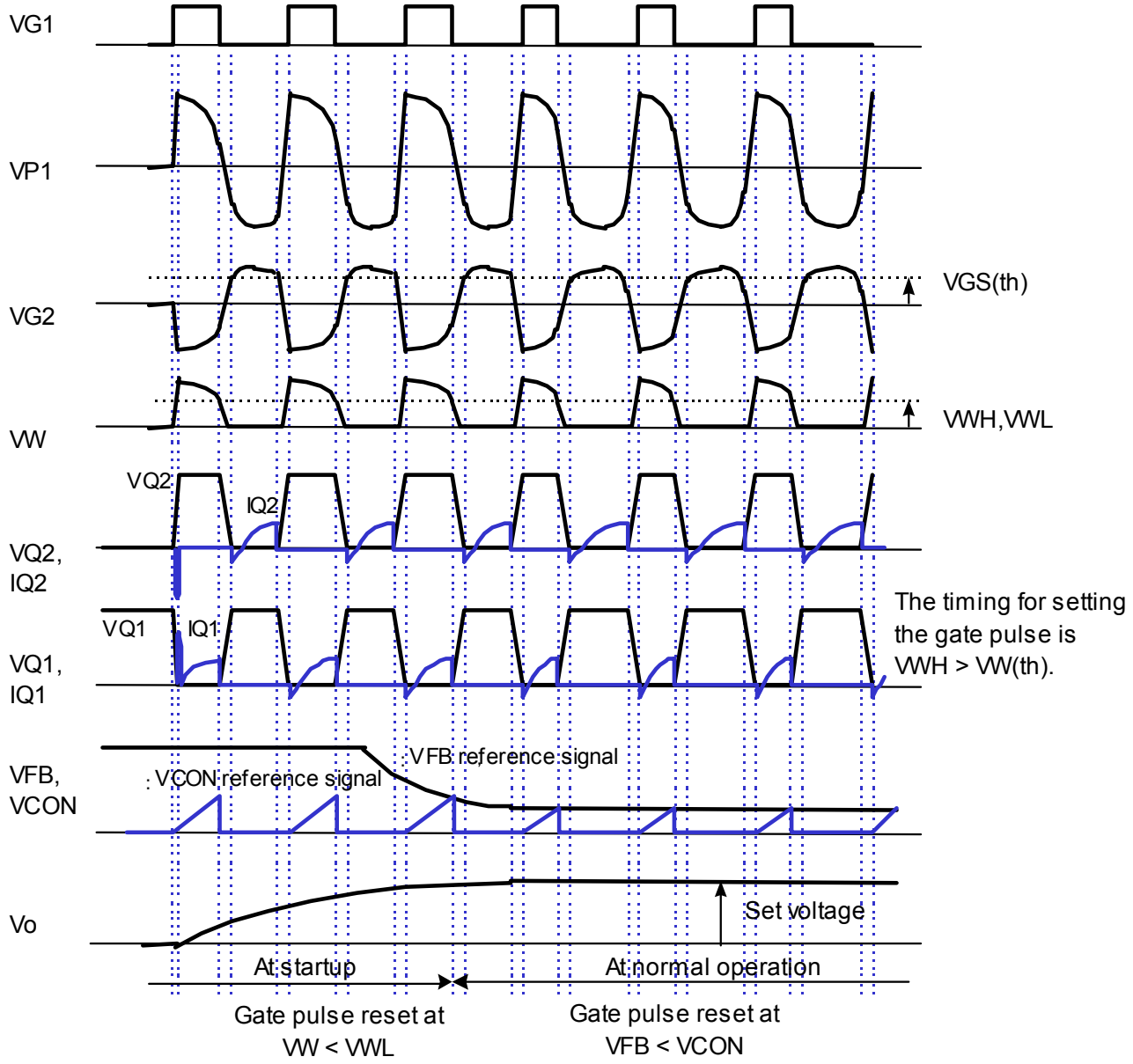


Fig. 8 Q1 Pulse Width Control Timing Chart

The Q1 pulse width control circuit holds steady the output voltage. The input signals for this circuit are the output signal VW from the winding voltage polarity discrimination circuit and the voltage reference value V_{FB} which holds the output voltage steady.

In the circuit shown in Figure 7 the auxiliary winding voltage for control power supply (V_{CC}) is negative and the VW voltage reaches zero level while Q2 is on. When Q2 turns off, the auxiliary winding voltage becomes positive and VW exceeds the threshold value VWH. The Q1 ON time is determined by this timing. In addition a capacitor time setting is needed in the VW circuit so that the gate signal is output after Q1 voltage reaches zero.

The voltage reference V_{FB} is generated by the output voltage adjustment circuit generating a signal for deviation from the set output voltage value, isolating the deviation signal using photo

isolator PC1 and converting it to the collector voltage value for the transistor on the light-receiving side. During normal operation, the size of the reference signal V_{CON} value, which increases in proportion from the time when the voltage reference value V_{FB} and the auxiliary winding voltage turn positive, is compared using the comparator PWMCP. The RS flip-flop FT1 is set and Q1 turns off when the reference signal value exceeds the voltage reference value.

When Q1 turns off, the Q2 gate voltage VG2 goes from negative to positive and Q2 turns ON when VG2 exceeds the Q2 gate threshold value VGS(th). The reference signal V_{CON} will return to the default setting after Q1 has turned off and when it drops below VWL.

At startup, the transformer winding voltage VP1 (refer to Fig. 1) may switch from positive to negative before the reference signal exceeds the voltage reference value after Q1 has turned ON. To prevent arm short circuits in such circumstances, the M-Power2A has a function to force Q1 off when VW has dropped below the threshold value voltage VWL, before the transformer winding voltage VP1 switches from positive to negative.

(3) MOSFET drive, dead time

The Q1 in the MOSFET is driven directly by the control IC. The circuit in the output section from the control IC consists of a CMOS push-pull circuit and the MOSFET gates provide a full swing to the Vcc voltage. The wire inductance between the MOSFET and the control IC is extremely small, eliminating malfunction. There is a dead time between when the VW voltage signal exceeds VWH to when Q1 turns on to prevent arm short circuits when Q1 turns on.

For safety the output stage from the control IC has a built-in resistor of 10kΩ between G and S enabling the Q1 drain voltage to be applied even when there is no V_{CC}. For example, during the latch protection operation, there is no chance of destruction even if the AC input remains supplied.

(4) Protection functions and latched shutdown

・Over current protection

The following form of over current protection is built in to protect the M-Power2A and power supply even if there is a problem with the load.

Over current (OC) protection and pulse-by-pulse operation voltage: V_{OC}

A latched shutdown operation is also provided for over current and short circuit current to ensure stopping for any problems. When stopped, the control IC drive output maintains a sinking status. A 36ms dead timer is provided for an over current latched shutdown. This is to prevent protection from operating for over current such as the charge current for an electrolytic capacitor on the load side when starting.

・Over voltage protection

A latched shutdown is implemented if the M-Power2A V_{CC} pin voltage exceeds the operation stop over voltage $V_{CCH(OFF)}$.

・Over heating protection

Over heating protection (T_{jOH}) is built into the control IC. If the temperature of the control IC

increases to the over heating protection (T_{jOH}) operating point due to a problem in the load or other cause, a latched shutdown (36ms timer latch) is implemented.

The latched shutdown is released by reducing the power supply voltage V_{CC} to the latch release voltage $V_{CC(LA)}$ or less.

The following table lists the specifications of the latched shutdown implemented as a protection function.

No.	Protection Function	Latched shutdown specifications
1	Over current protection(OC)	When an over current is detected on Vcc for 36ms or longer a latched shutdown is implemented(timer latch).
2	Over voltage protection(OV)	A latched shutdown is implemented when V_{CCH}(OFF) is detected once.
3	Over heat protection(OH)	When a temperature higher than TjOH is detected for 36ms or longer a latched shutdown is implemented(timer latch).

5-5. Internal structure

As shown in Figure 9, Q1 Q2 and the control IC are die-bonded in three frames and are connected between the frames using aluminum wire. In other words a discrete device structure is used without a ceramic board such as the ones used in hybrid IC structures or other wiring boards. There are thus fewer structural parts assembly processing is faster and a simple highly reliable structure is achieved.

The M-Power2A uses full-molded structures without any poles on the rear side. The structure also provides adequate insulation between Q1, Q2, and the control IC.

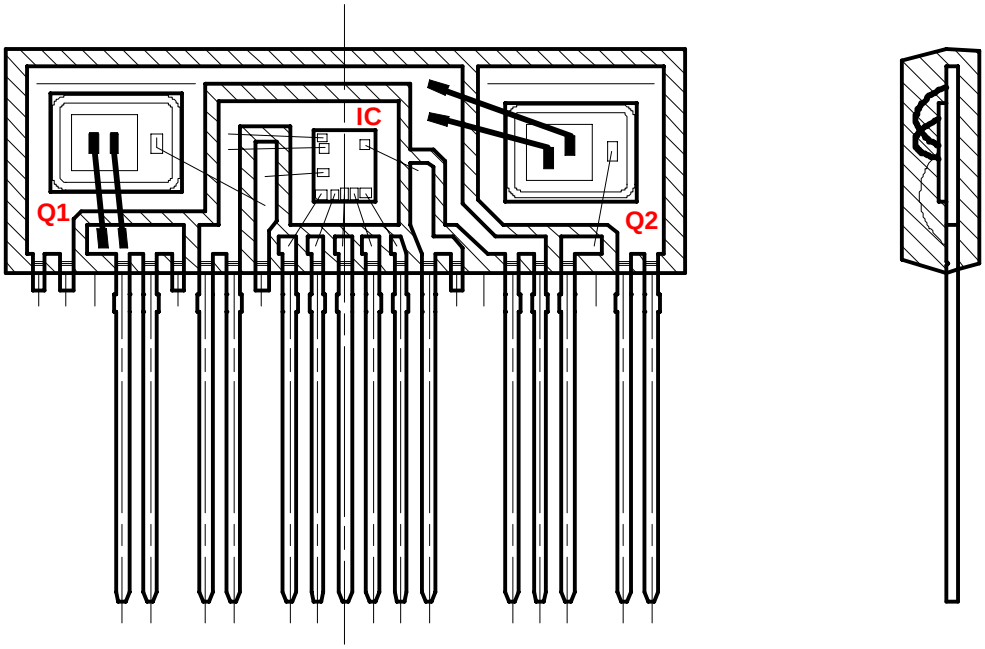


Fig.9 Internal Structure

6. Design advices

6-1 Setting resonant conditions: Figure 10 shows the transformer configuration.

(1) Maximum power Po(max) : Calculating Po(max)

① PCr(max): The maximum power supplied from the resonant capacitor Cr.

The following equation can be used to calculate PCr(max) assuming that the resonant capacitor's voltage amplitude equals the DC bus voltage (Ed) when the power supplied from the resonant capacitor is at its maximum value.

$$P(Cr) = Cr \times Ed^2 \times fr \quad \cdots\cdots(6\text{-}1)$$

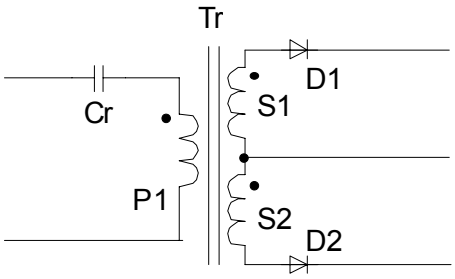


Fig. 10 Transformer configuration

fr: Resonant frequency

Calculate the resonant frequency (fr) with the following equation.

$$fr = \frac{1}{2\pi\sqrt{Cr \times Ls}} \quad \cdots\cdots(6\text{-}2)$$

Ls: Inductance in primary with one of the secondary windings (either S1 or S2) short-circuited. The power supplied from the resonant capacitor is the component of the power supplied in the secondary and the transformer's magnetizing energy (reactive power.)

② Magnetizing energy: PLm(max)

Calculate the transformer's peak magnetizing current (ILmp) with the following equation.

$$ILmp = \frac{1}{2} \times \frac{n \cdot Vo}{Lm} \times \frac{1}{2 \cdot fr} = \frac{n \cdot Vo}{4 \cdot Lm \cdot fr}$$

Equation 6-3 yields the maximum magnetizing energy PLm(max). In this equation Lo is the primary winding inductance when secondary windings are open Vo is the output voltage and n is the turn ratio (Np1/Np2.)

$$PLm(max) = Lo \times (ILmp)^2 \times fr = \frac{(n \cdot Vo)^2}{16\pi Lo \cdot fr} \quad \cdots\cdots(6\text{-}3)$$

③ Maximum power supplied to secondary: Po(max)

The results from equations 6-1 and 6-3 can be used to find Po(max) using equation 6-4.

$$Po(max) = PCr(max) - PLm(max) = Cr \cdot Ed^2 \cdot fr - \frac{(n \cdot Vo)^2}{16\pi Lo \cdot fr} \quad \cdots\cdots(6\text{-}4)$$

(2) Method for Setting the Resonant Conditions

① Maximum power Po(max) : Setting Po(max)

When actually designing the system the effect of the conversion efficiency (η) on the power supply maximum load (Pload(max)) must be taken into account when calculating the maximum power (Po(max).)

$$Po(max) = Pload(max) / \eta \quad \cdots\cdots(6 - 5)$$

The conversion efficiency (η) is about 0.9.

② Setting Lo : the inductance Lo when transformer's secondary windings are open.

In order for Q1 and Q2 to provide zero voltage switching the transformer's magnetizing energy must be greater than the energy involved in charging/discharging the output capacitance of Q1 and Q2. Consequently the inductance when the transformer's secondary is open (Lo) is set between 1.0 and 2.0mH.

③ Setting fr : the resonant frequency: fr and minimum switching frequency :fs(min).

Since the secondary diodes (Ds1 and Ds2) have current flowing continuously (without pause), design the resonant frequency (fr) so that the minimum switching frequency (fs(min)) is about 10% higher than the resonant frequency (fr). We recommend designing the resonant frequency at about 70kHz to 80kHz.

④ DC bus voltage : Ed

When setting the maximum power use the minimum value for the DC bus voltage (Ed(min).)

⑤ Setting the resonant capacitance (Cr) and inductance when the transformer's secondary winding is shorted (Ls.)

Enter the values set in steps 1 through 4 (Po(max), Lo, fr, n, Vo, and Ed(min)) into equation 6-4 to calculate Cr. Next, enter Cr into equation 6-2 to calculate Ls.

⑥ Setting Example

Setting conditions:

With Pload(max) = 80W, Vo = 15V, Ed(min) = 400V, Lo = 2mH, fr = 80kHz, and n = 80/6 = 13.33 (Np = 80 turns, Ns1 = Ns2 = 6 turns), Po can be calculated as follows:

Po = 80 ÷ 0.9 = 88.89W

The resonant capacitance (Cr) can be calculated from equation 6-4:

$$Cr = \frac{Po(\max) + (n \times Vo)^2 / 16 \times Lo \times fr \times \pi}{Ed(\min)^2 \times fr} = \frac{88.89 + (13.33 \times 15)^2 / 16 \times 2 \times 10^{-3} \times 80 \times 10^3 \times \pi}{400^2 \times 80 \times 10^3}$$

= 7.3n F

Ls can be calculated from equation 6-2:

$$Ls = 1 / Cr \times (fr \times 2\pi)^2 = 1 / 7.3 \times 10^{-9} \times (80 \times 10^3 \times 2\pi) = 542\mu \text{ H}$$

6-2 Startup circuit V_{CC} winding circuit and latched shutdown release

Figure 11 shows the startup circuit and V_{CC} winding circuit. The current input from the AC line flows to the M-Power2A through startup resistor R1 and charges electrolytic capacitor C2. The IC starts operating when this voltage reaches the on threshold voltage ($V_{CC(ON)}$) and then power is supplied to the IC from the transformer's auxiliary winding.

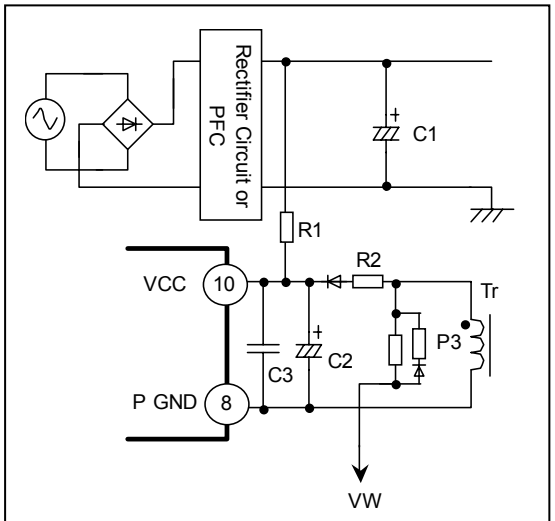


Fig.11 Startup and Vcc winding circuit example

A low control IC current consumption has been achieved by converting the control IC to CMOS. A current can be supplied below $V_{CC(ON)}$ to charge the electrolytic capacitor with an extremely small current consumption. We recommend setting the V_{CC} winding voltage so that the V_{CC} terminal voltage is between 19.0 and 20.0V at normal operation. (Refer to the current diagrams in the specifications for more details on current consumption.)

Figure 12 shows an example voltage waveform at the V_{CC} terminal at startup. Operation starts and the current consumption increases when V_{CC} reaches $V_{CC(ON)}$. After operation starts the V_{CC} terminal voltage begins to drop and continues to drop until power starts being supplied from the V_{CC} windings. If V_{CC} drops below $V_{CCL(OFF)}$ at this point, the UVLO will stop the control circuit and the startup will fail, so startup resistor R1 and capacitor C2 must be set so that V_{CC} does not drop below $V_{CCL(OFF)}$.

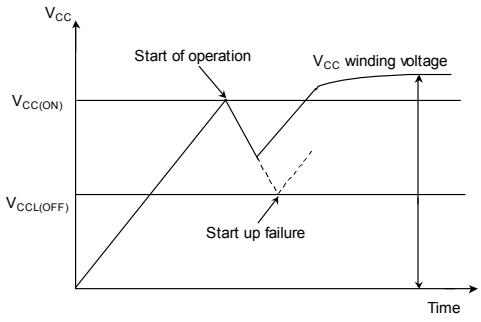


Fig. 12 Example waveform at Vcc terminal at startup

Furthermore the resistance of R2 in the V_{CC} winding circuit (see figure 11) must be 2.2Ω or higher. So capacitor C2 holds no charge at startup the VW voltage (described below) will be difficult to generate and normal operation will be impossible (due to the arm short circuit protection). In addition make a poor coupling between the V_{CC} winding and the secondary windings (S1 and S2) and a tight coupling between the V_{CC} winding and the primary winding (P1). Since the M-Power2A IC is a CMOS type connect a capacitor C3 with a capacitance of at least 0.1μF to the V_{CC} terminal.

A latched shutdown will be maintained as long as V_{CC} is above $V_{CC(LA)}$. To maintain the latched shutdown select a startup resistor that will produce a current higher than the latch hold current (40 to 60μA) so that V_{CC} will be above $V_{CC(LA)}$. Refer to the V_{CC}-I_{CC} (latched shutdown) diagram in the specifications for details. To release the latch V_{CC} must be decreased below $V_{CC(LA)}$.

6-3 Q2 Gate pin: Q2 drive circuit and Q2 drive winding (P2 Winding)

- Q2 drive circuit

Figure 13 shows an example of Q2 drive circuit. The following procedures show how to set the circuit constants for the circuit in Figure 13.

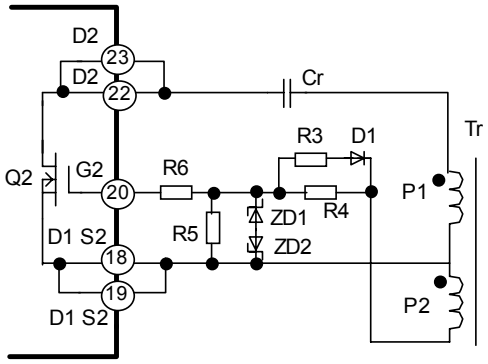


Fig. 13 Q2 Drive Circuit

<R3>

The resistances of R3 and R6 determine Q2 turn-off speed. We recommend a resistance of R3 about 22Ω and that of R6 about 47Ω. These are the same value as the IC output stage resistance when Q1 turns off.

<R4>

The resistances of R4 and R6 determine Q2 turn-on speed. Use the following two conditions. R4 must satisfy both conditions.

Condition 1:

Set R4 and R6 so that Q2 turns on after Q1 turns off and while current is still flowing through Q2's body diode.

Condition 2:

Set R4 and R6 so that an arm short circuit does not occur at startup when Q2 turns on. Verify that the V_{CC} winding's electrolytic capacitor (C2 in Figure 11) is completely charged at startup.

We recommend setting the R4 value between 150Ω and 470Ω.

<R5>

The R5 resistor is inserted so that the Q2 gate voltage will not rise at the dv/dt of Q2's drain voltage rate. We recommend setting the R5 value about 22kΩ.

Figure 14 shows another Q2 drive circuit preventing a reverse voltage across the gate to source of Q2 when the switch is off. This drive circuit is recommended when an input voltage (Ed) range is wide. When the P2 voltage is negative the diode D12 is on and the transistor TR1 turns on. Thus the Q2 gate to source voltage is zero.

We recommend R16 is 2.2Ω, R13 is 4.7kΩ(1/2W), D13 is high speed switching type which capacitance between terminals is less than 10pF and TR1 is a PNP transistor (V_{CE}= -50V, I_C= -0.5A, $f_T$min=100MHz).

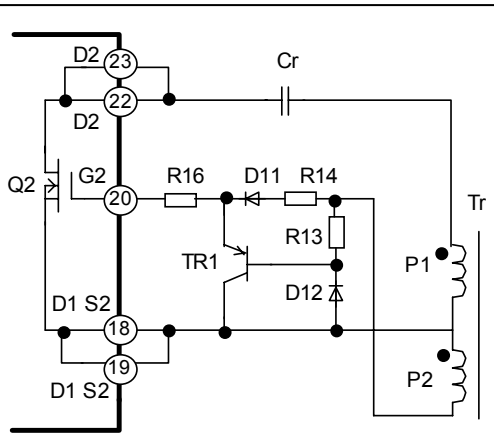


Fig. 14 Q2 Drive Circuit

・Q2 Drive winding (P2 winding)

Set the P2 winding's maximum voltage (VP2(max)) below the Q2 gate's absolute maximum rating (V_{GS}); we recommend setting VP2(max) between 80% and 90% of V_{GS}. The P2 winding generates its maximum voltage when the DC bus voltage (C1 voltage) is at its maximum value (Edc) and Q1's on duty is small. When Q1 is on a voltage close to Ed is being applied to the main winding (P1 winding). Use the following equation to calculate the number of winding turns in the Q2 drive winding.

$$\text{Edc(max)}/2 \times \frac{NP2}{NP1} \fallingdotseq VGS \times 0.8 \sim 0.9 < \text{Q2 gate's absolute maximum rating } (V_{GS})$$

Edc(max) is the maximum value of the DC bus voltage.

NP1 is the number of winding turns in the main winding (P1 winding).

NP2 is the number of winding turns in the Q2 drive winding (P2 winding).

Select zener diodes ZD1 and ZD2, shown in Figure 13, with the zener voltage that is below the Q2 gate's absolute maximum rating and below VP2(max).

6-4 VW pin

Figure 15 shows an example of VW terminal drive circuit.

A comparator (VWCP) is connected internally to the VW terminal. VWCP compares the threshold value with the VW terminal voltage and turns Q1 on or off (forced off).

Q1 on threshold: VWH is 1.56V (typical).

Q1 off threshold: VWL is 0.56V (typical).

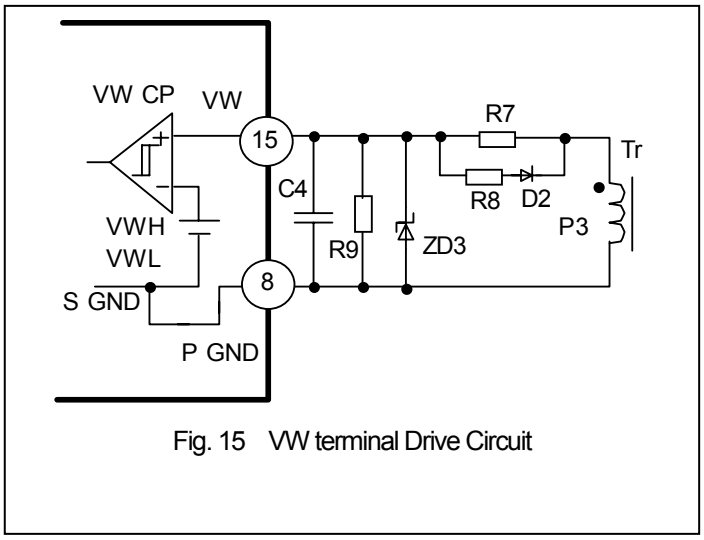


Fig. 15 VW terminal Drive Circuit

The power supply for VWCP is the V_{REF} voltage so the absolute maximum rating of the VW terminal is minimum voltage of V_{REF} voltage (4.75V). Thus as shown in Figure 15 insert a zener diode ZD3 that break down voltage is less than 4.5V. To delay Q1 turns on a capacitor C4 is added in this terminal. We recommend C4 is 820pF.

Make the resistance of R7 as small as possible so that the VW terminal voltage exceeds VWH even when the V_{CC} winding voltage is low. To force off Q1 when the VW terminal voltage is less than VWL make the resistance of R8 as small as possible.

We recommend setting R7 R8 R9 and ZD3 to the following values.

R7: 10 kΩ

R8: 1kΩ to 5.6 kΩ

R9: 100 kΩ

ZD3: 3.9V

These are recommended values. Verify that there are no problems by testing the circuits.

6-5 CON pin

Connect capacitor $C_{(CON)}$ between the CON terminal and S GND terminal to set the maximum Q1 ON width:t_{ON}. Figure 16 shows the relationship between t_{ON} and $C_{(CON)}$.The t_{ON} setting is determined so that the power supply can supply the maximum required load using minimum DC bus capacitor voltage. It is possible to verify experimentally that the output voltage does not decrease under the conditions outlined above.

The capacitance of $C_{(CON)}$ must be above 1000pF.

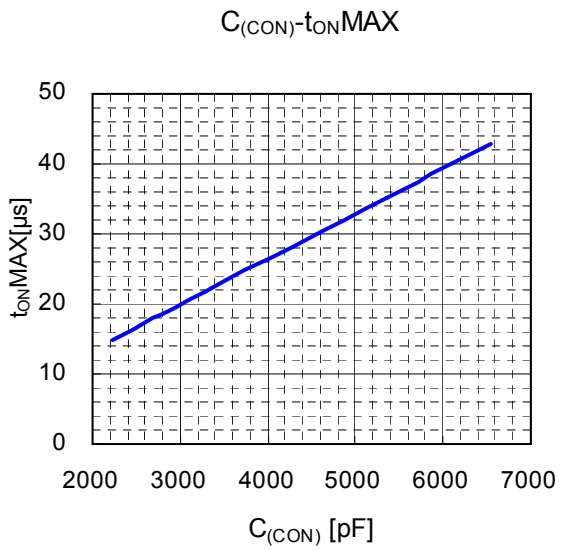


Fig. 16 Relationship between t_{ON} and $C_{(CON)}$.

6-6 VREF pin

The M-Power2A IC is a CMOS IC, so connect a capacitor C5 to VREF terminal as shown in Figure 17. We recommend a C5 capacitance above 1µF.

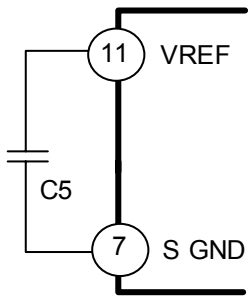


Fig. 17 VREF Terminal

6-7 IS pin

IS terminal is the over current detection terminal which is negative voltage to P GND. Connect S1 terminal and P GND. Insert the resistor Rs between C1 minus terminal and P GND terminal and low pass filter circuit composed of C6 and R10 as shown in Figure 18.

The resistance of Rs is determined as following equation.

$$Rs = (R_{10} I_{is} + V_{OC}) / ID1$$

In this equation Voc is the over current detection voltage

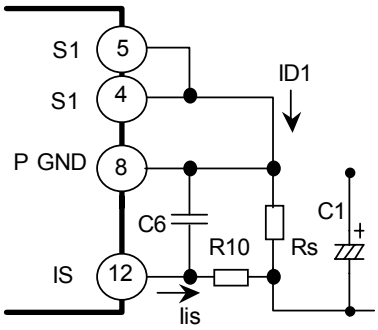


Fig. 18 IS Terminal

and Iis is the current flowing from IS terminal to R10. Iis is about 20uA. The over current detection is negative voltage but Voc is equal to plus 0.168V when using the above equation.

ID1 is a current flowing through Q1and ID1 is decreased when input voltage is minimum. Thus determine the resistance of Rs when input voltage is minimum rated. The corner frequency of the filter circuit composed of C6 and R10 is shown in the following equation.

$$fs = 1 / 2\pi R_{10} C_6$$

Setting C6 and R10 is determined as fs should be between 100kHz and 1MHz. We recommend C6 is 1000pF and R10 is 1kΩ.

6-8 FB pin: Feedback control

Figure 19 shows an example of the circuit in the vicinity of the FB terminal. The FB terminal is the input terminal for the feedback signal of the secondary's constant voltage control circuit. To prevent improper operation due to noise, insert a filter composed of a capacitor C7 and resistor R11 as shown in Figure 19. It is also needed to proper operation in a printed circuit board layout consideration that current paths from PC1 to FB and S GND terminals must be as near as possible and the paths must not be laid out under a transformer.

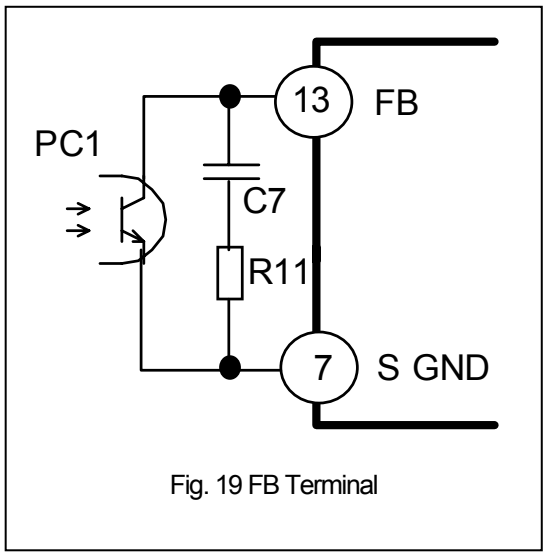


Fig. 19 FB Terminal

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