RFD16N05LSM

Product Preview

MOSFET - Power, N-Channel, Logic Level

50 V, 16 A, 47 mΩ

These are N−Channel logic level power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use with logic level (5 V) driving sources in applications such as programmable controllers, switching regulators, switching converters, motor relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3 V to 5 V range, thereby facilitating true on−off power control directly from logic circuit supply voltages.

Formerly developmental type TA09871.

Features

- 16 A, 50 V
- $r_{DS(ON)} = 0.047\ \Omega$
- UIS SOA Rating Curve (Single Pulse)
- Design Optimized for 5 V Gate Drives
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

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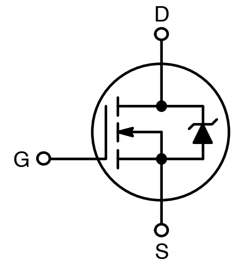
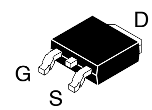
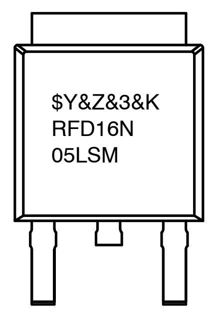




DPAK
TO−252
CASE 369AS

MARKING DIAGRAM



&Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
RFD16N05LSM	= Specific Device Code

ORDERING INFORMATION

Part Number	Package	Brand
RFD16N05LSM9A	TO−252AA	RFD16N05LSM

May, 2019 − Rev. 2
Publication Order Number:
RFD16N05LSM/D

MAXIMUM RATINGS

Rating	Symbol	RFD16N05LSM9A	Units
Drain to Source Voltage (Note 1)	V_{DS}	50	V
Drain to Gate Voltage (R_{GS} 20 kΩ) (Note 1)	V_{DGR}	50	V
Continuous Drain Current	I_D	16	A
Pulsed Drain Current (Note 3)	I_{DM}	45	A
Gate to Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation	P_D	60	W
Derate Above 25°C		0.48	W/°C
Operating and Storage Temperature	T_J, T_{STG}	−55 to 150	°C
Maximum Temperature for Soldering			
Leads at 0.063 in (1.6 mm) from Case for 10 s	T_L	300	°C
Package Body for 10 s, See Techbrief 334	T_{pkg}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. T_J = 25°C to 125°C.

ELECTRICAL SPECIFICATIONS (T_C = 25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250 mA, V_{GS} = 0 V, Figure 10		50	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA, Figure 9		1	–	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V		–	–	1	μA
			T_C = 150°C	–	–	50	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V		–	–	100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 16 A, V_{GS} = 5 V		–	–	0.047	Ω
		I_D = 16 A, V_{GS} = 4 V		–	–	0.056	Ω
Turn−On Time	$t_{(ON)}$	V_{DD} = 25 V, I_D = 8 A, V_{GS} = 5 V, R_{GS} = 12.5 Ω Figures 15, 16		–	–	60	ns
Turn−On Delay Time	$t_{d(ON)}$			–	14	–	ns
Rise Time	t_r			–	30	–	ns
Turn−Off Delay Time	$t_{d(OFF)}$			–	42	–	ns
Fall Time	t_f			–	14	–	ns
Turn−Off Time	$t_{(OFF)}$			–	–	–	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0 V to 10 V	V_{DD} = 40 V, I_D = 16 A, R_L = 2.5 Ω Figures 17, 18	–	–	80	nC
Gate Charge at 5 V	$Q_{g(5)}$	V_{GS} = 0 V to 5 V		–	–	45	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0 V to 1 V		–	–	3	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$			–	–	2.083	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			–	–	100	°C/W

SOURCE TO DRAIN DIODE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 16 A	-	-	1.5	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = 16 A, dI_{SD}/dt = 100 A/μs	-	-	125	ns

2. Pulse Test: Pulse Width ≤300 ms, Duty Cycle ≤2%.
3. Repetitive Rating: Pulse Width limited by max junction temperature.

TYPICAL PERFORMANCE CURVES (Unless Otherwise Specified)

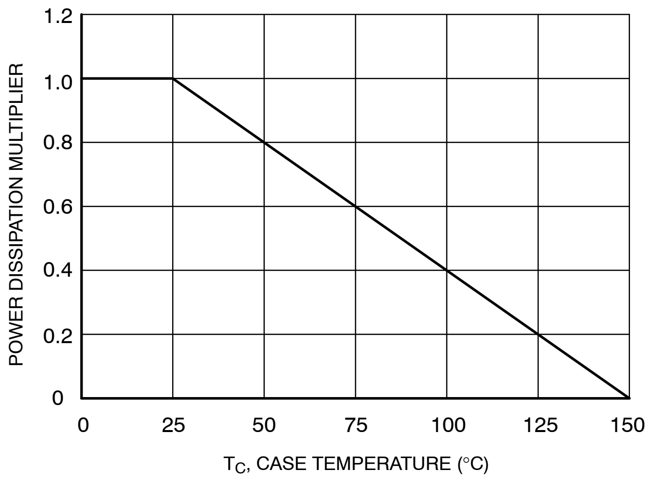


Figure 1. Normalized Power Dissipation vs Case Temperature

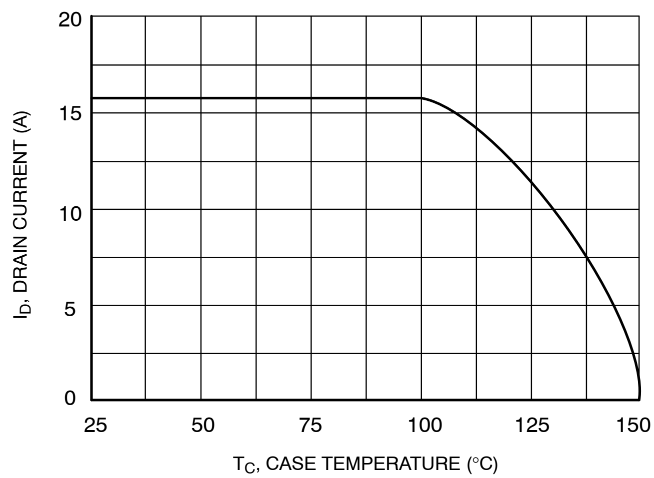


Figure 2. Maximum Continuous Drain Current vs Case Temperature

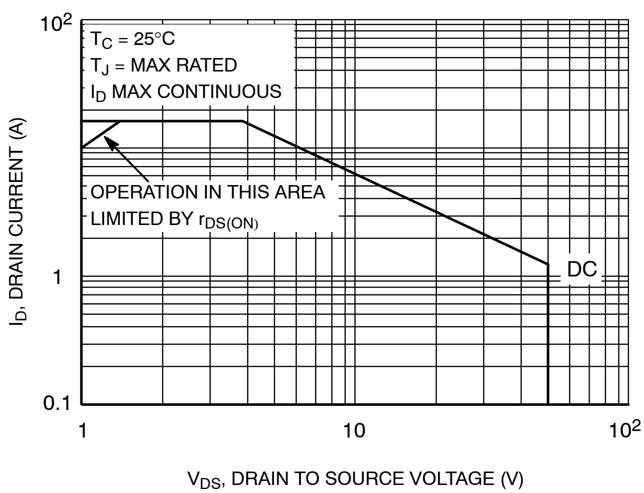


Figure 3. Forward Bias Safe Operating Area

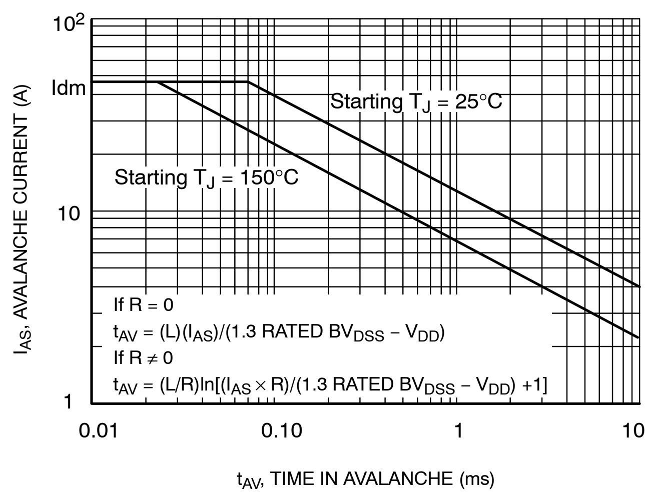


Figure 4. Unclamped Inductive Switching SOA (Single Pulse UIS SOA)

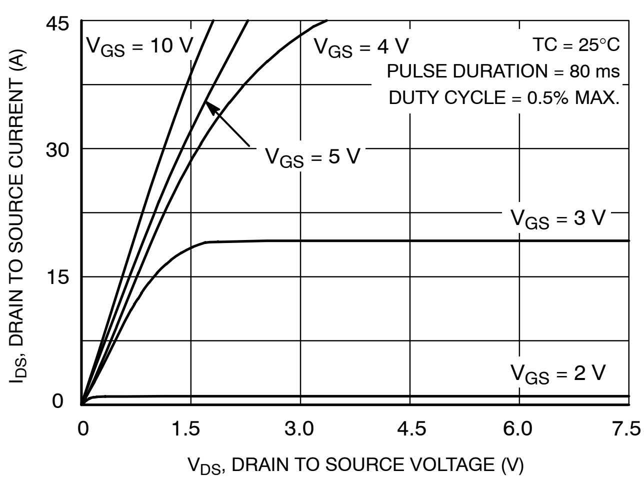


Figure 5. Saturation Characteristics

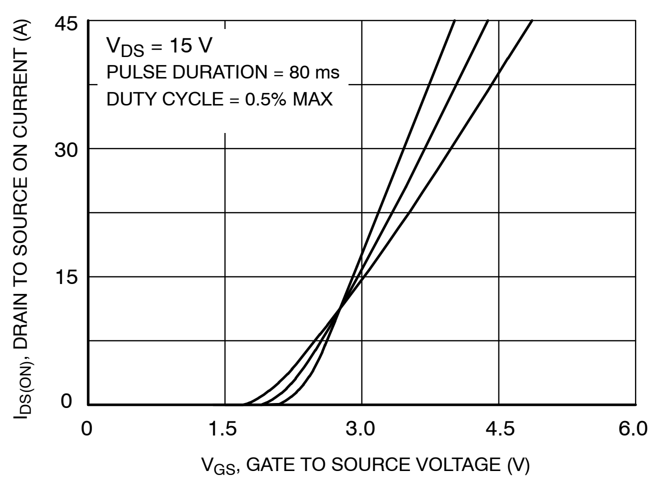


Figure 6. Transfer Characteristics

TYPICAL PERFORMANCE CURVES (Unless Otherwise Specified) (continued)

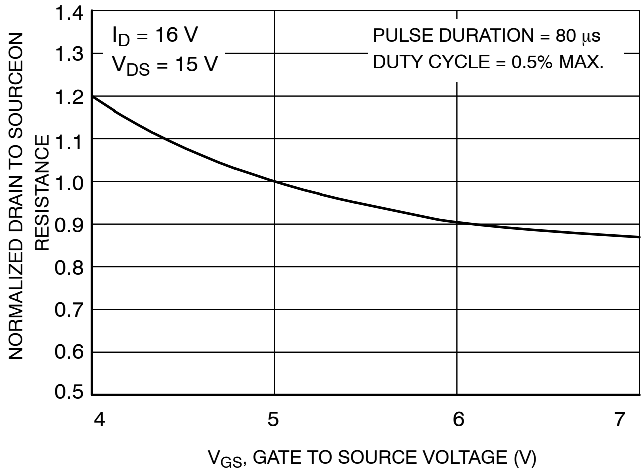


Figure 7. Drain to Source on Resitance vs Gate Voltageand Drain Current

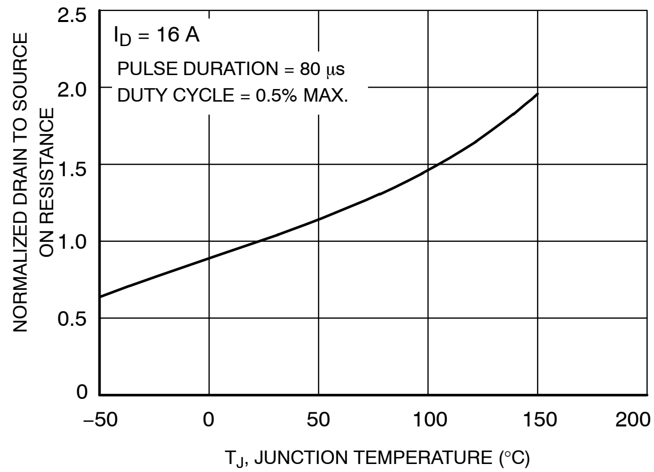


Figure 8. Normalized Drain to Source on Resistance vs. Junction Temperature

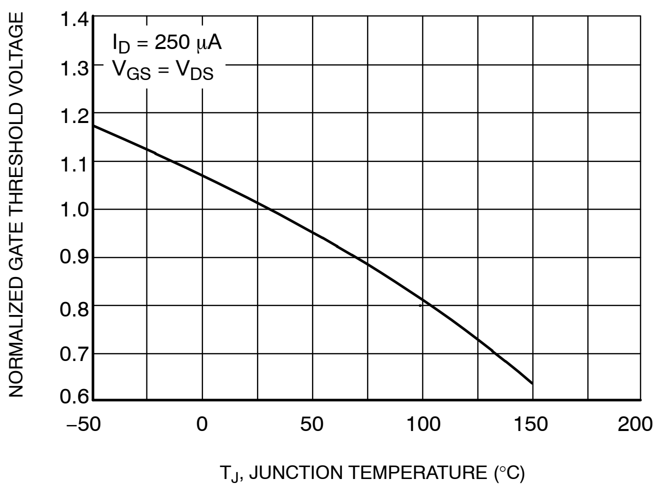


Figure 9. Normalized Gate Threshold vs Junction Temperature

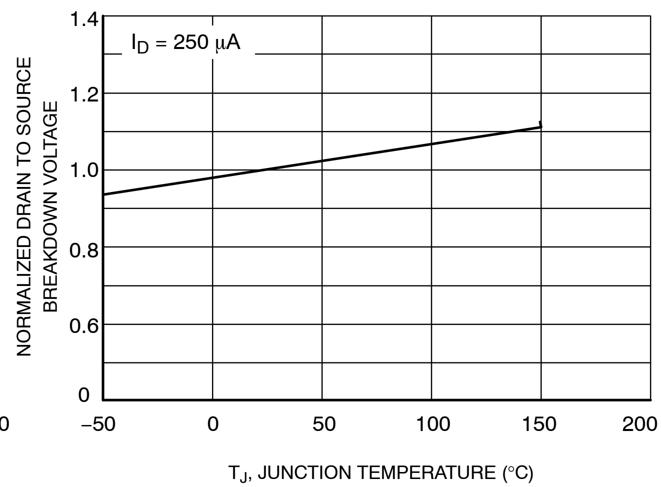


Figure 10. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

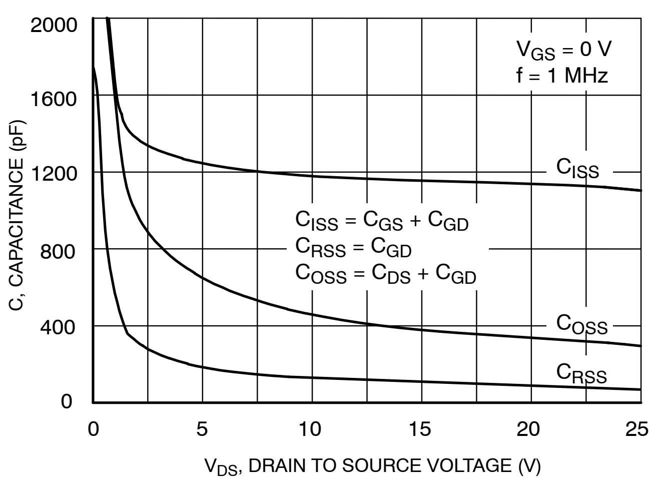


Figure 11. Capacitance vs Drain to Source Voltage

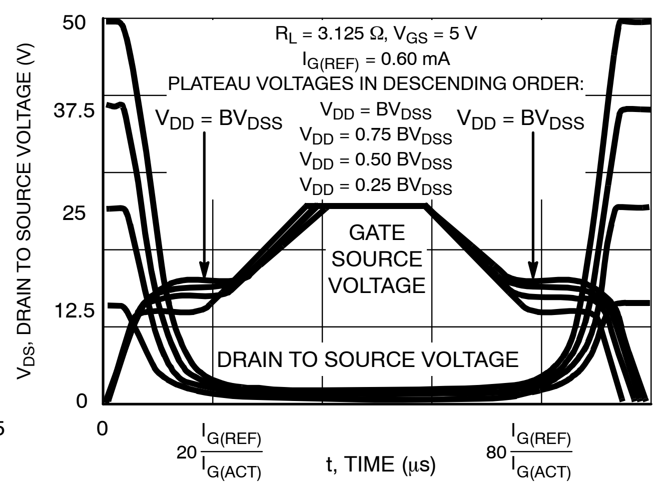


Figure 12. Normalized Switching Waveforms for Constant Gate Current

TEST CIRCUITS AND WAVEFORMS

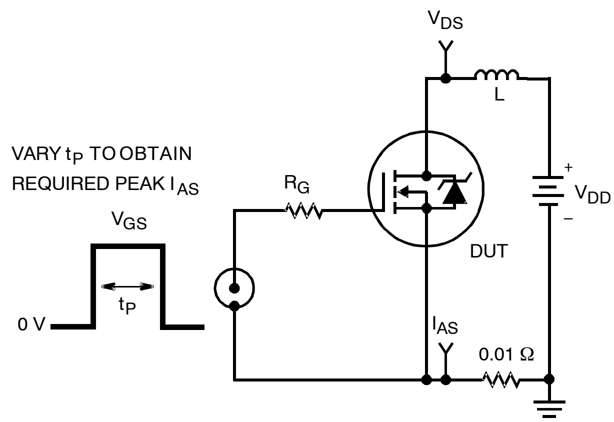


Figure 13. Unclamped Energy Test Circuit

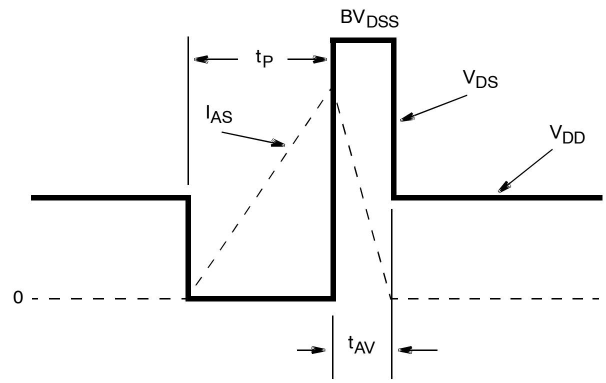


Figure 14. Unclamped Energy Waveforms

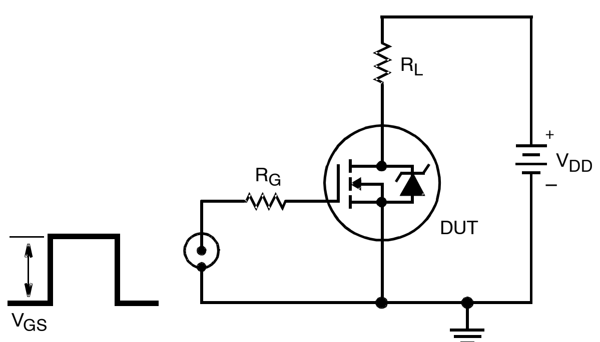


Figure 15. Switching Time Test Circuit

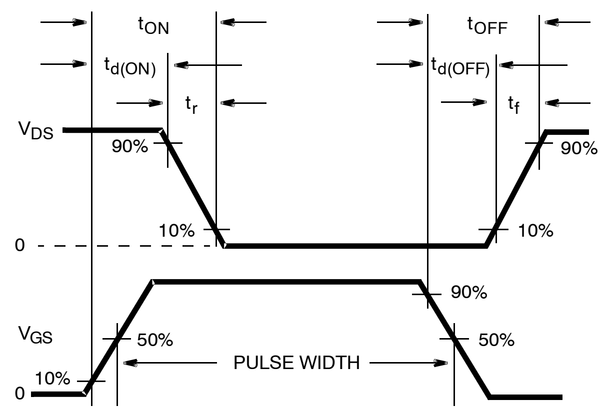


Figure 16. Resistive Switching Waveforms

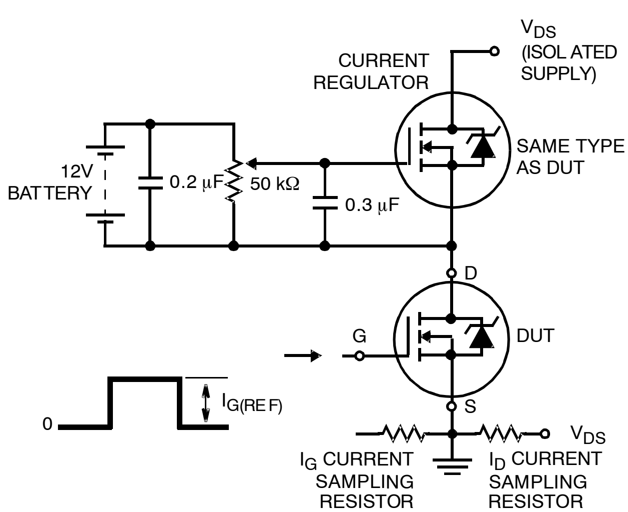


Figure 17. Gate Charge Test Circuit

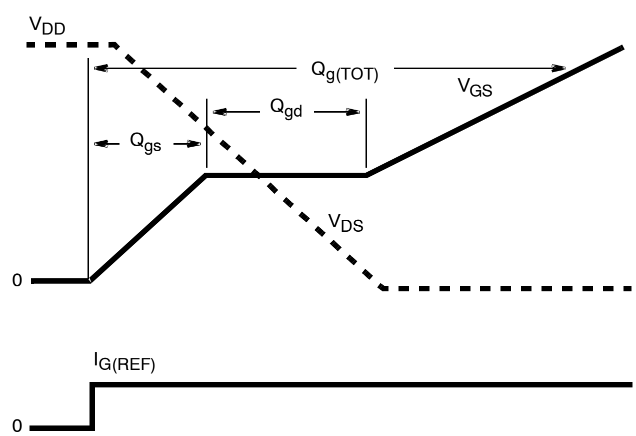


Figure 18. Gate Charge Waveforms

PSPICE ELECTRICAL MODEL

```
.SUBCKT RFD16N05L 2 1 3 ; REV 4/8/92

Ca 12 8 3.33e-9
Cb 15 14 3.11e-9
Cin 6 8 1.21e-9

Dbody 7 5 DBDMOD
Dbreak 5 11 DBKMOD
Dplcap 10 5 DPLCAPMOD

Ebreak 11 7 17 18 70.9
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evto 20 6 18 8 1

IT 8 17 1

Lgate 1 9 1.38e-9
Ldrain 2 5 1.0e-12
Lsource 3 7 1.0e-9

Mos1 16 6 8 8 MOSMOD M = 0.99
Mos2 16 21 8 8 MOSMOD M = 0.01

Rin 6 8 1e9
Rbreak 17 18 RBKMOD 1
Rdrain 5 16 RDSMOD 27.38e-3
Rgate 9 20 2.98
Rsource 8 7 RDSMOD 0.614e-3
Rvto 18 19 RVTOMOD 1

S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 8 19 DC 1
Vto 21 6 0.448

.MODEL DBDMOD D (IS = 1.34e-13 RS = 1.21e-2 TRS1 = 1.64e-3 TRS2 = 2.59e-6 +CJO = 1.13e-9
TT = 4.14e-8)
.MODEL DBKMOD D (RS = 8.82e-2 TRS1 = -2.01e-3 TRS2 = 7.32e-10)
.MODEL DPLCAPMOD D (CJO = 0.522e-9 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 2.054 KP = 24.73 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 1.01e-3 TC2 = 5.21e-8)
.MODEL RDSMOD RES (TC1 = 3.66e-3 TC2 = 1.46e-5)
.MODEL RVTOMOD RES (TC1 = -1.81e-3 TC2 = 1.41e-6)
.MODEL S1AMOD VSWITCH(RON = 1e-5 ROFF = 0.1 VON = -4.25 VOFF = -2.25)
.MODEL S1BMOD VSWITCH(RON = 1e-5 ROFF = 0.1 VON = -2.25 VOFF = -4.25)
.MODEL S2AMOD VSWITCH(RON = 1e-5 ROFF = 0.1 VON = -0.65 VOFF = 4.35)
.MODEL S2BMOD VSWITCH(RON = 1e-5 ROFF = 0.1 VON = 4.35 VOFF = -0.65)

.ENDS
```

NOTE: For further discussion of the PSPICE model, consult *A New PSPICE Sub−Circuit for the Power MOSFET Featuring Global Temperature Options*; written by William J. Hepp and C. Frank Wheatley.

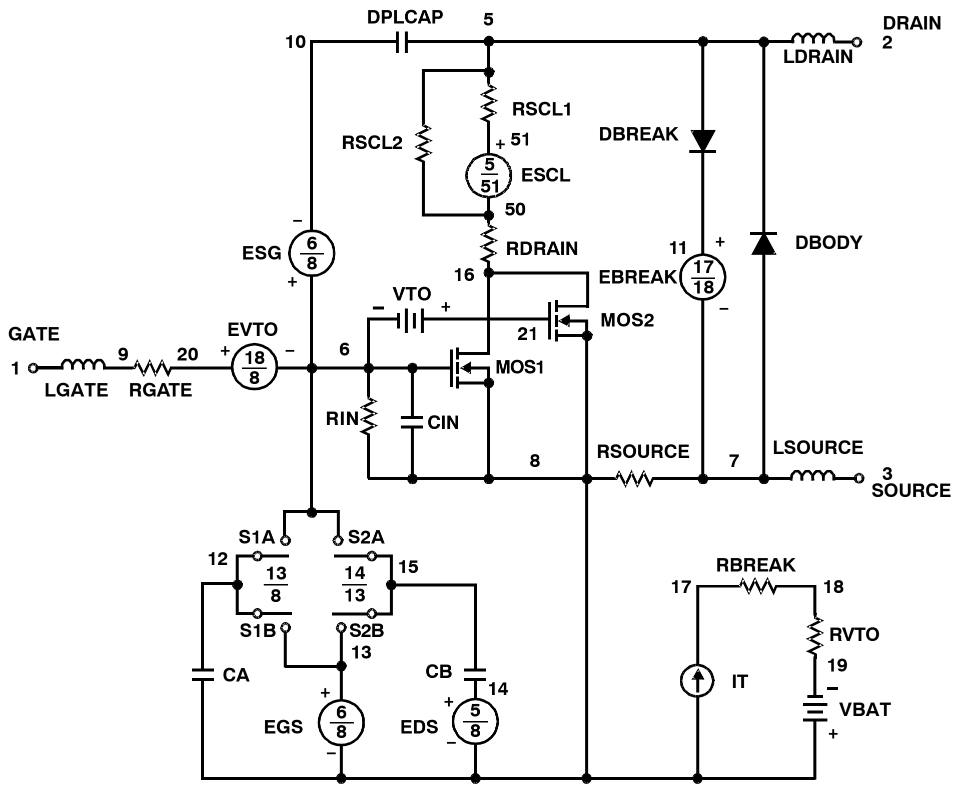
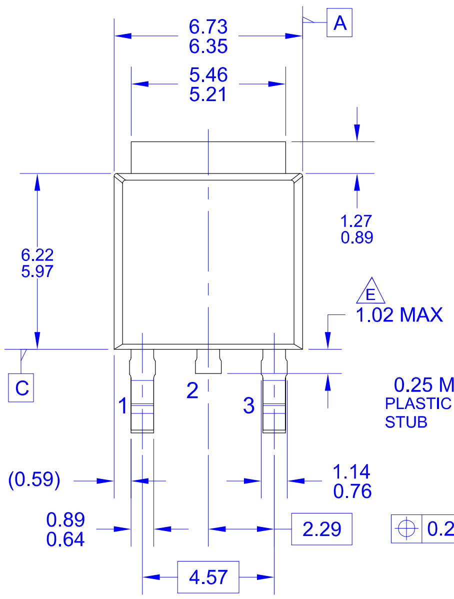

DPLCAP
5
10
DRAIN
2
LDRAIN
RSCL1
RSCL2
51
ESCL
DBREAK
50
RDRAIN
ESG
11
DBODY
16
EBREAK
VTO
MOS2
GATE
EVTO
21
1
9
20
6
MOS1
LGATE
RGATE
RIN
CIN
8
RSOURCE
7
LSOURCE
3
SOURCE
S1A
S2A
12
15
RBREAK
17
18
S1B
S2B
13
RVTO
19
CA
CB
14
IT
VBAT
EGS
EDS

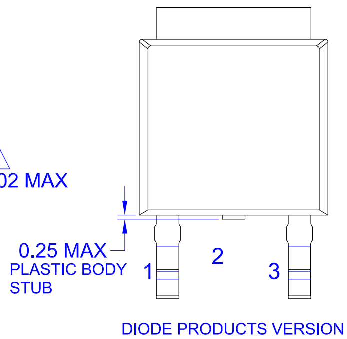
Figure 19.

DPAK3 (TO−252 3 LD)
CASE 369AS
ISSUE O

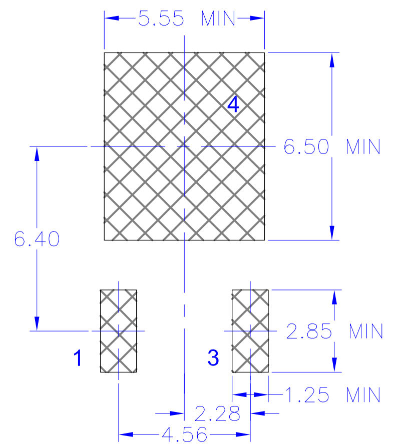
DATE 30 SEP 2016



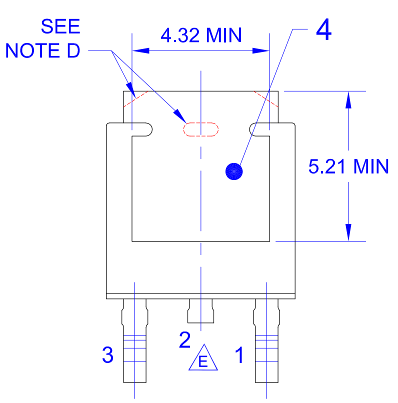
NON-DIODE PRODUCTS VERSION



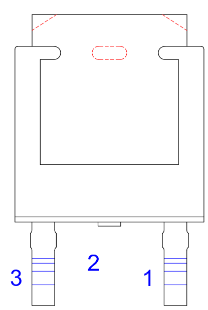
DIODE PRODUCTS VERSION



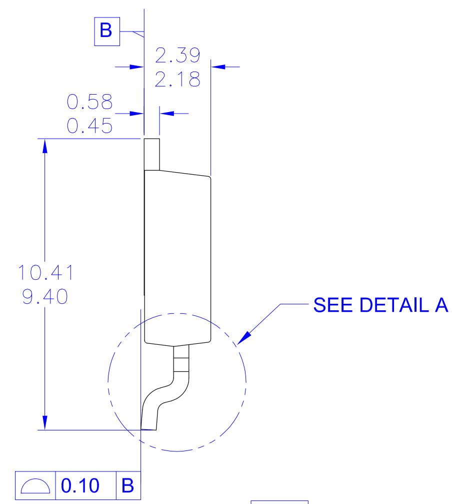
LAND PATTERN RECOMMENDATION

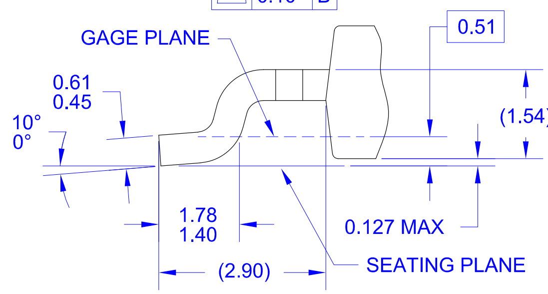


NON-DIODE PRODUCTS VERSION



DIODE PRODUCTS VERSION





DETAIL A
(ROTATED -90°)
SCALE: 12X

NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.

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DESCRIPTION:	**DPAK3 (TO−252 3 LD)**	**PAGE 1 OF 1**

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