

**56A, 30V, 0.016 Ohm, N-Channel, Logic Level UltraFET Power MOSFETs**



These N-Channel power MOSFETs are manufactured using the innovative UltraFET™ process.

This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA76129.

**Ordering Information**

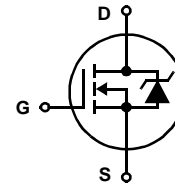
PART NUMBER	PACKAGE	BRAND
HUF76129P3	TO-220AB	76129P
HUF76129S3S	TO-263AB	76129S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF76129S3ST.

**Features**

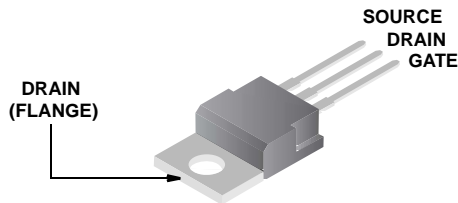
- Logic Level Gate Drive
- 56A, 30V
- Ultra Low On-Resistance,  $r_{DS(ON)} = 0.016\Omega$
- Temperature Compensating PSPICE® Model
- Temperature Compensating SABER® Model
- Thermal Impedance SPICE Model
- Thermal Impedance SABER Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

**Symbol**

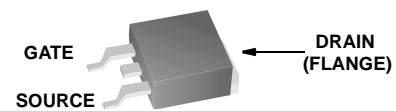


**Packaging**

JEDEC TO-220AB



JEDEC TO-263AB



# HUF76129P3, HUF76129S3S

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

		UNITS
Drain to Source Voltage (Note 1) . . . . .	$V_{DSS}$	30 V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1) . . . . .	$V_{DGR}$	30 V
Gate to Source Voltage . . . . .	$V_{GS}$	$\pm 16$ V
<b>Drain Current</b>		
Continuous ( $T_C = 25^\circ\text{C}$ , $V_{GS} = 10\text{V}$ ) (Figure 2) . . . . .	$I_D$	56 A
Continuous ( $T_C = 100^\circ\text{C}$ , $V_{GS} = 5\text{V}$ ) . . . . .	$I_D$	35 A
Continuous ( $T_C = 100^\circ\text{C}$ , $V_{GS} = 4.5\text{V}$ ) (Figure 2) . . . . .	$I_D$	34 A
Pulsed Drain Current . . . . .	$I_{DM}$	Figure 4
Pulsed Avalanche Rating . . . . .	$E_{AS}$	Figures 6, 17, 18
Power Dissipation . . . . .	$P_D$	105 W
Derate Above $25^\circ\text{C}$ . . . . .		0.83 W/ $^\circ\text{C}$
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$	-40 to 150 $^\circ\text{C}$
<b>Maximum Temperature for Soldering</b>		
Leads at 0.063in (1.6mm) from Case for 10s . . . . .	$T_L$	300 $^\circ\text{C}$
Package Body for 10s, See Techbrief 334 . . . . .	$T_{pkg}$	260 $^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTE:**

- $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$ .

## Electrical Specifications $T_A = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>OFF STATE SPECIFICATIONS</b>						
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$ (Figure 12)	30	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $T_C = 150^\circ\text{C}$	-	-	250	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 16\text{V}$	-	-	$\pm 100$	nA
<b>ON STATE SPECIFICATIONS</b>						
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$ (Figure 11)	1	-	3	V
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 56\text{A}$ , $V_{GS} = 10\text{V}$ (Figure 9, 10)	-	0.014	0.016	$\Omega$
		$I_D = 35\text{A}$ , $V_{GS} = 5\text{V}$ (Figure 9)	-	0.0175	0.021	$\Omega$
		$I_D = 34\text{A}$ , $V_{GS} = 4.5\text{V}$	-	0.0195	0.023	$\Omega$
<b>THERMAL SPECIFICATIONS</b>						
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)	-	-	1.20	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220 and TO-263	-	-	62	$^\circ\text{C}/\text{W}$
<b>SWITCHING SPECIFICATIONS (<math>V_{GS} = 4.5\text{V}</math>)</b>						
Turn-On Time	$t_{ON}$	$V_{DD} = 15\text{V}$ , $I_D \cong 34\text{A}$ , $R_L = 0.441\Omega$ , $V_{GS} = 4.5\text{V}$ , $R_{GS} = 6.8\Omega$ (Figures 15, 21, 22)	-	-	160	ns
Turn-On Delay Time	$t_{d(ON)}$		-	14	-	ns
Rise Time	$t_r$		-	90	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	28	-	ns
Fall Time	$t_f$		-	32	-	ns
Turn-Off Time	$t_{OFF}$		-	-	90	ns

# HUF76129P3, HUF76129S3S

## Electrical Specifications $T_A = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
<b>SWITCHING SPECIFICATIONS (<math>V_{GS} = 10\text{V}</math>)</b>							
Turn-On Time	$t_{ON}$	$V_{DD} = 15\text{V}$ , $I_D \cong 56\text{A}$ , $R_L = 0.268\Omega$ , $V_{GS} = 10\text{V}$ , $R_{GS} = 8.2\Omega$ (Figures 16, 21, 22)	-	-	62	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	11	-	ns	
Rise Time	$t_r$		-	30	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	68	-	ns	
Fall Time	$t_f$		-	35	-	ns	
Turn-Off Time	$t_{OFF}$		-	-	155	ns	
<b>GATE CHARGE SPECIFICATIONS</b>							
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0\text{V to } 10\text{V}$	$V_{DD} = 15\text{V}$ , $I_D \cong 35\text{A}$ , $R_L = 0.429\Omega$ $I_{g(REF)} = 1.0\text{mA}$ (Figures 14, 19, 20)	-	37	45	nC
Gate Charge at 5V	$Q_{g(5)}$	$V_{GS} = 0\text{V to } 5\text{V}$		-	19	23	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0\text{V to } 1\text{V}$		-	1.4	1.7	nC
Gate to Source Gate Charge	$Q_{gs}$			-	4.50	-	nC
Gate to Drain "Miller" Charge	$Q_{gd}$			-	10.30	-	nC
<b>CAPACITANCE SPECIFICATIONS</b>							
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$ (Figure 13)	-	1350	-	pF	
Output Capacitance	$C_{OSS}$		-	700	-	pF	
Reverse Transfer Capacitance	$C_{RSS}$		-	160	-	pF	

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 35\text{A}$	-	-	1.25	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 35\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	60	ns
Reverse Recovered Charge	$Q_{RR}$	$I_{SD} = 35\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	105	nC

## Typical Performance Curves

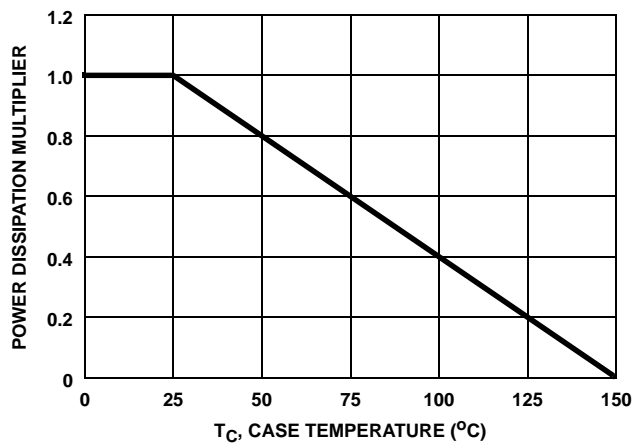


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

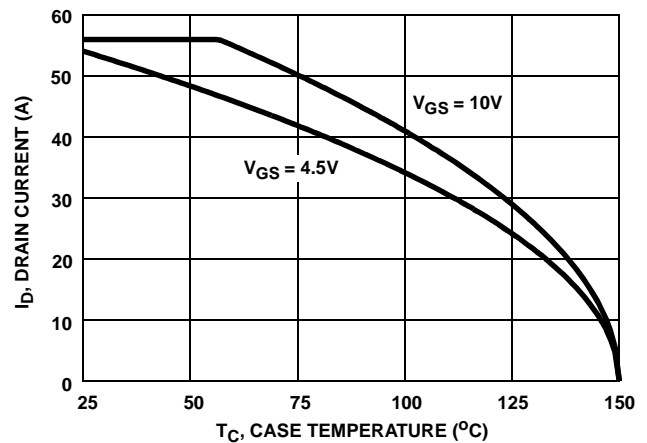


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

Typical Performance Curves (Continued)

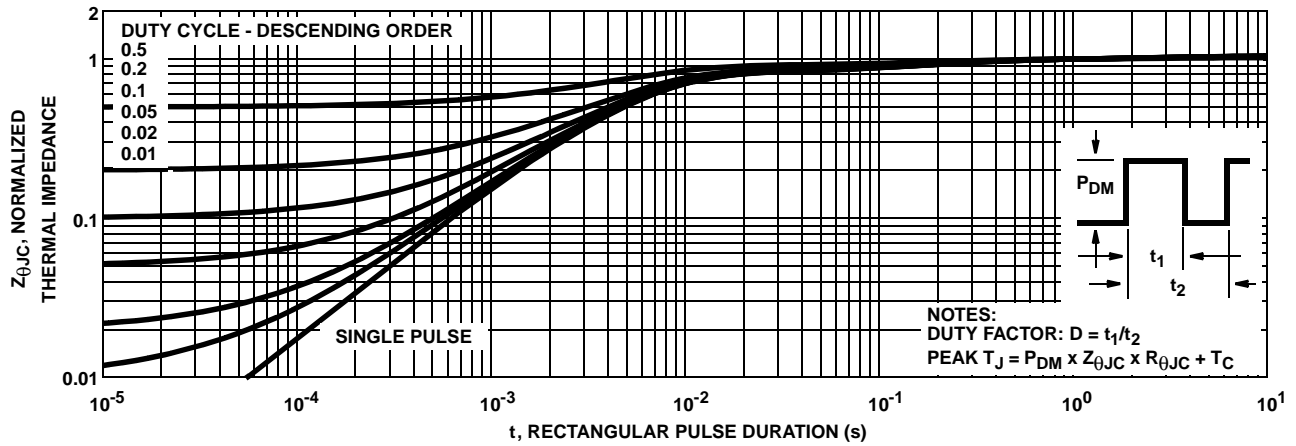


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

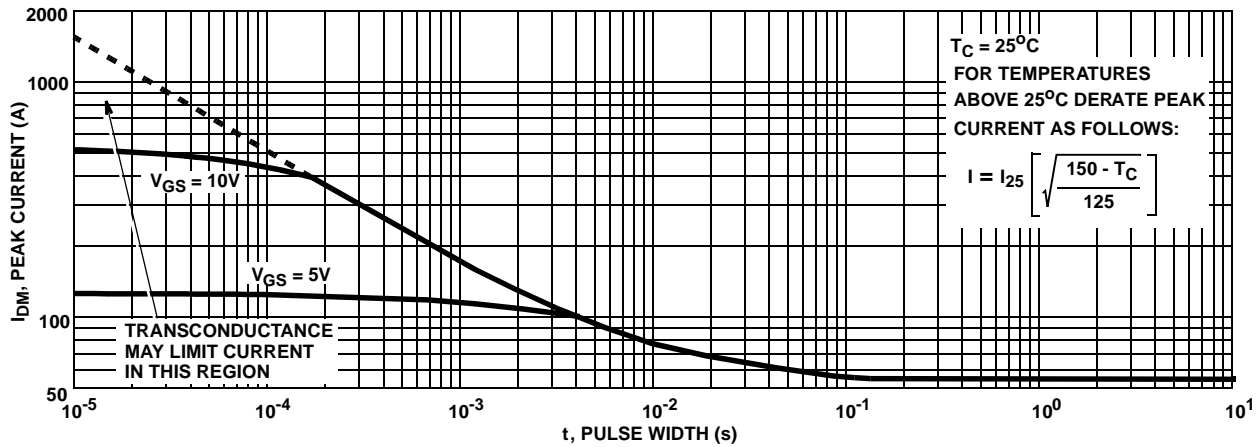


FIGURE 4. PEAK CURRENT CAPABILITY

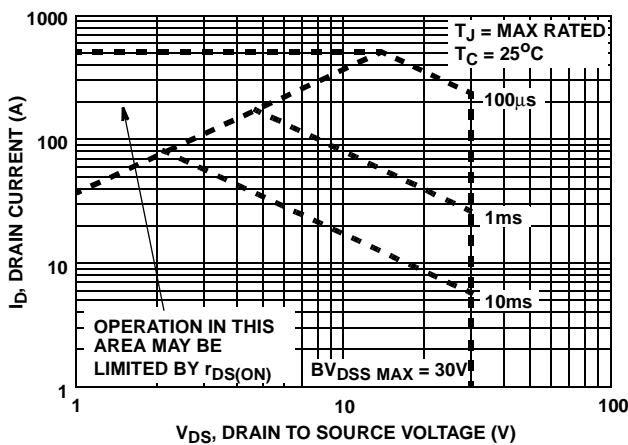
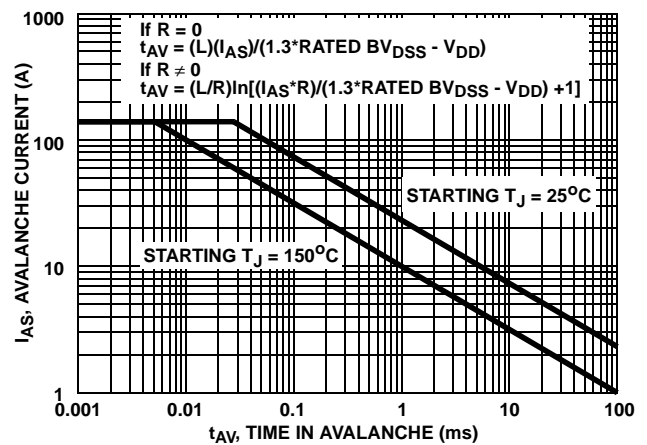


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

Typical Performance Curves (Continued)

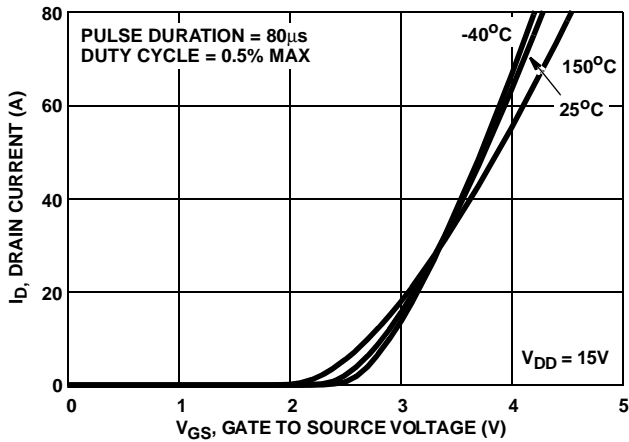


FIGURE 7. TRANSFER CHARACTERISTICS

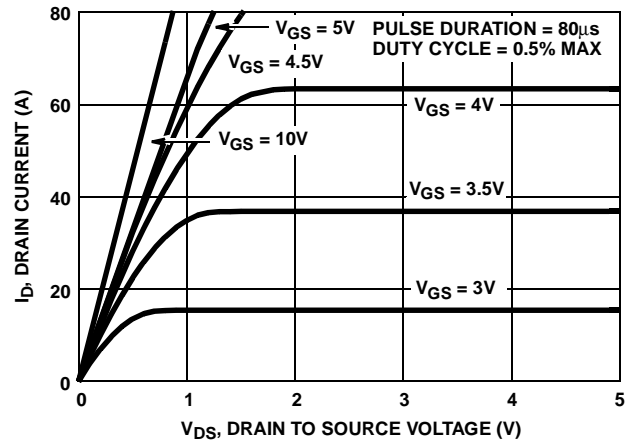


FIGURE 8. SATURATION CHARACTERISTICS

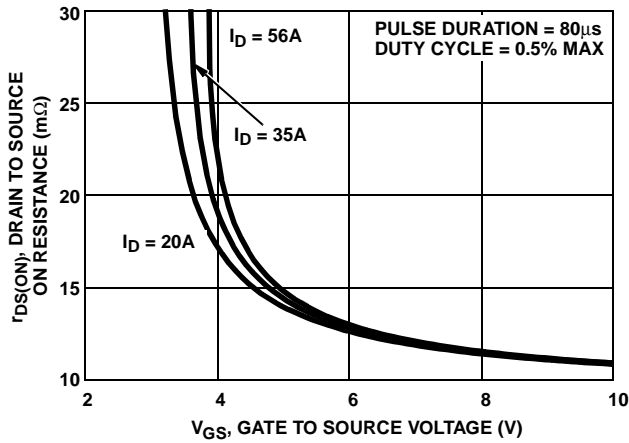


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

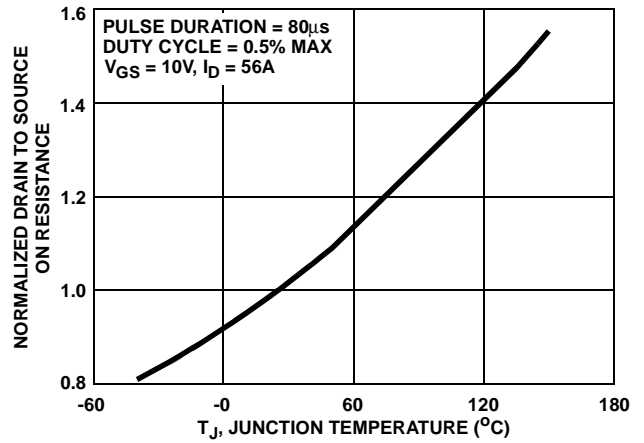


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

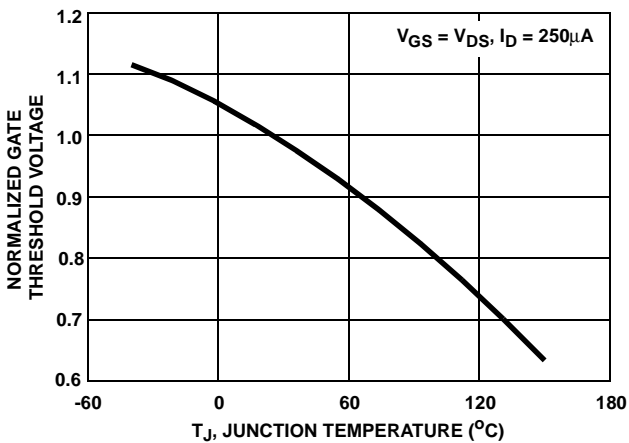


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

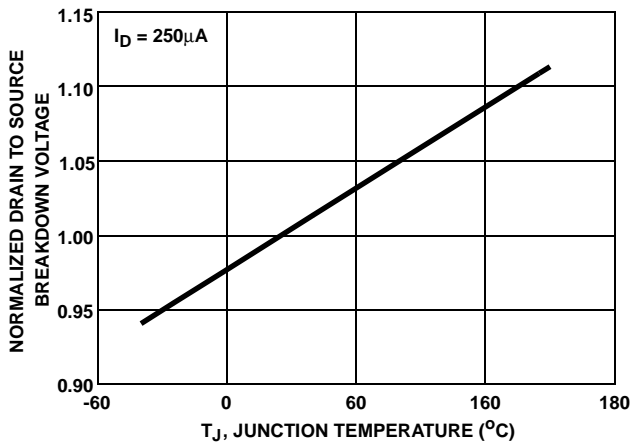


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

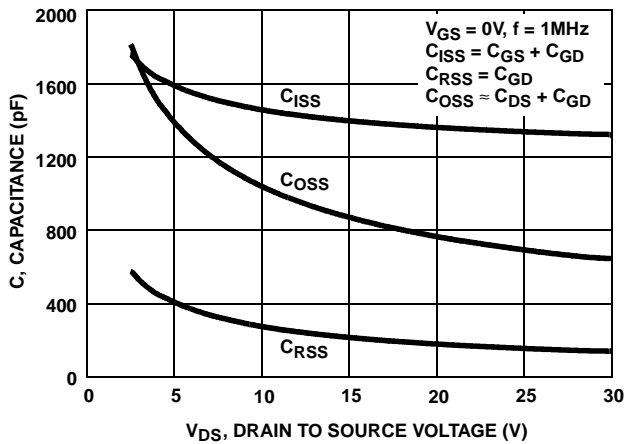
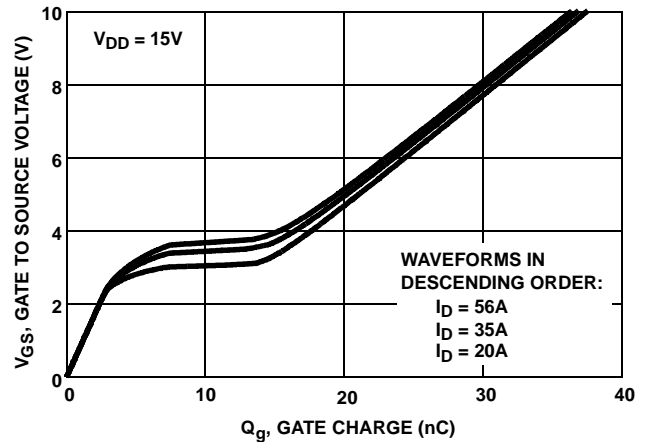


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes 7254 and 7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

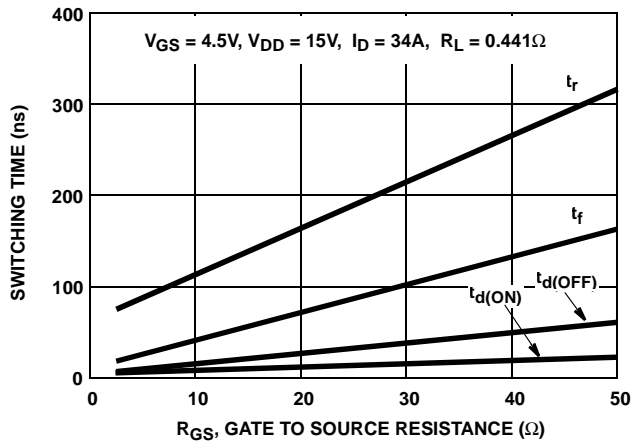


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

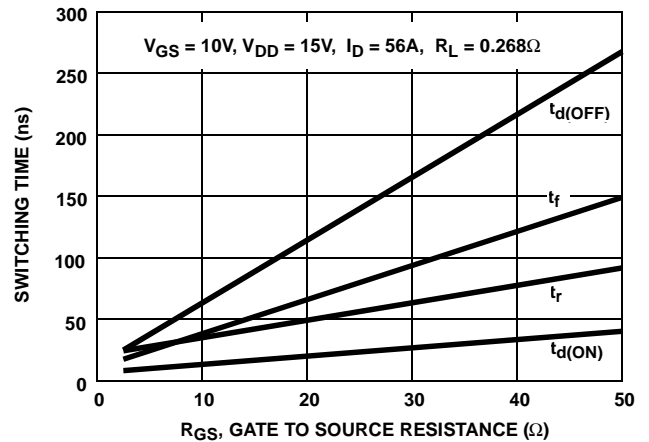


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

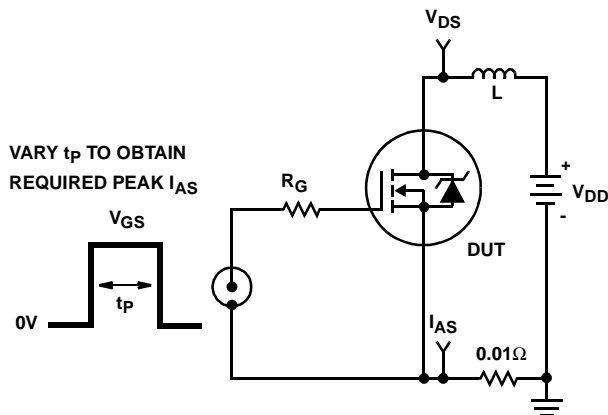


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

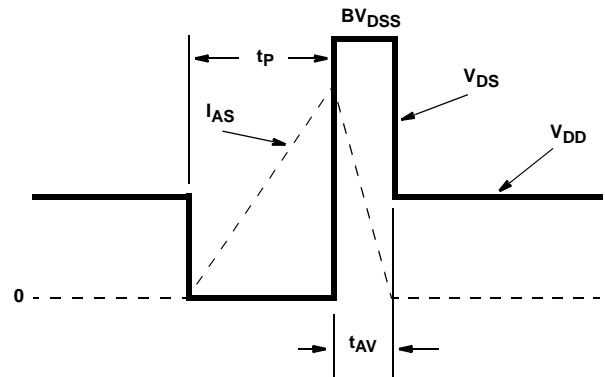


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

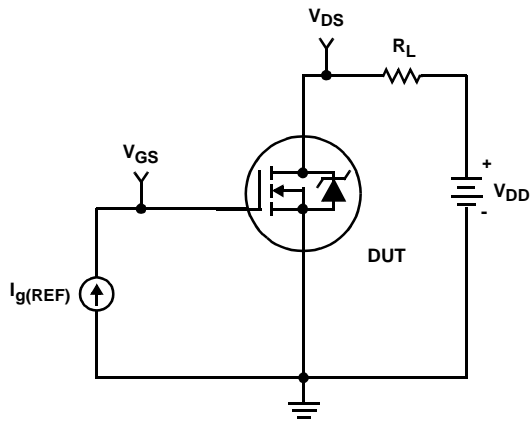


FIGURE 19. GATE CHARGE TEST CIRCUIT

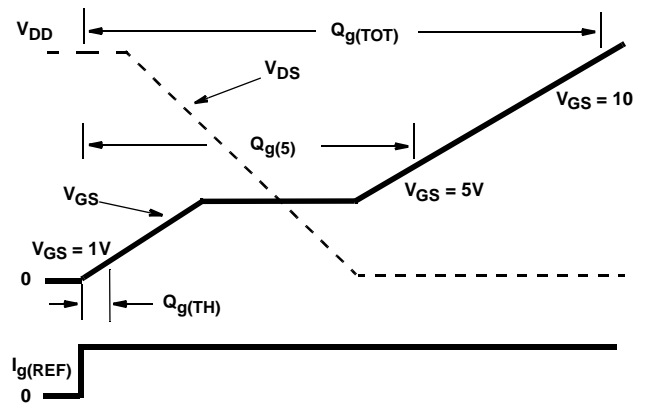


FIGURE 20. GATE CHARGE WAVEFORMS

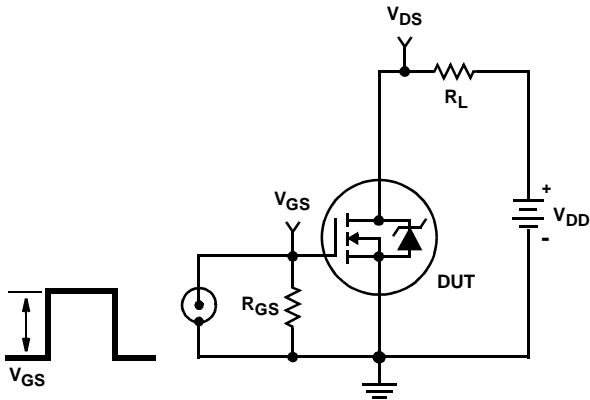


FIGURE 21. SWITCHING TIME TEST CIRCUIT

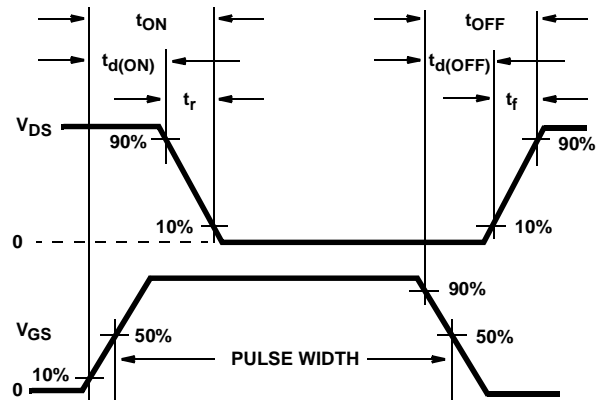


FIGURE 22. SWITCHING TIME WAVEFORM

**PSPICE Electrical Model**

SUBCKT HUF76129 2 1 3 ; REV August 1998

CA 12 8 1.95e-9  
 CB 15 14 2.06e-9  
 CIN 6 8 1.18e-9

DBODY 7 5 DBODYMOD  
 DBREAK 5 11 DBREAKMOD  
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 33.5  
 EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 6 10 6 8 1  
 EVTHRES 6 21 19 8 1  
 EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9  
 LGATE 1 9 4.02e-9  
 LSOURCE 3 7 3.45e-9

MMED 16 6 8 8 MMEDMOD  
 MSTRO 16 6 8 8 MSTROMOD  
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1  
 RDRAIN 50 16 RDRAINMOD 1.3e-3  
 RGATE 9 20 3.5  
 RLDRAIN 2 5 10  
 RLGATE 1 9 40.2  
 RLSOURCE 3 7 34.5  
 RSLC1 5 51 RSLCMOD 1e-6  
 RSLC2 5 50 1e3  
 RSOURCE 8 7 RSOURCEMOD 8e-3  
 RVTHRES 22 8 RVTHRESMOD 1  
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

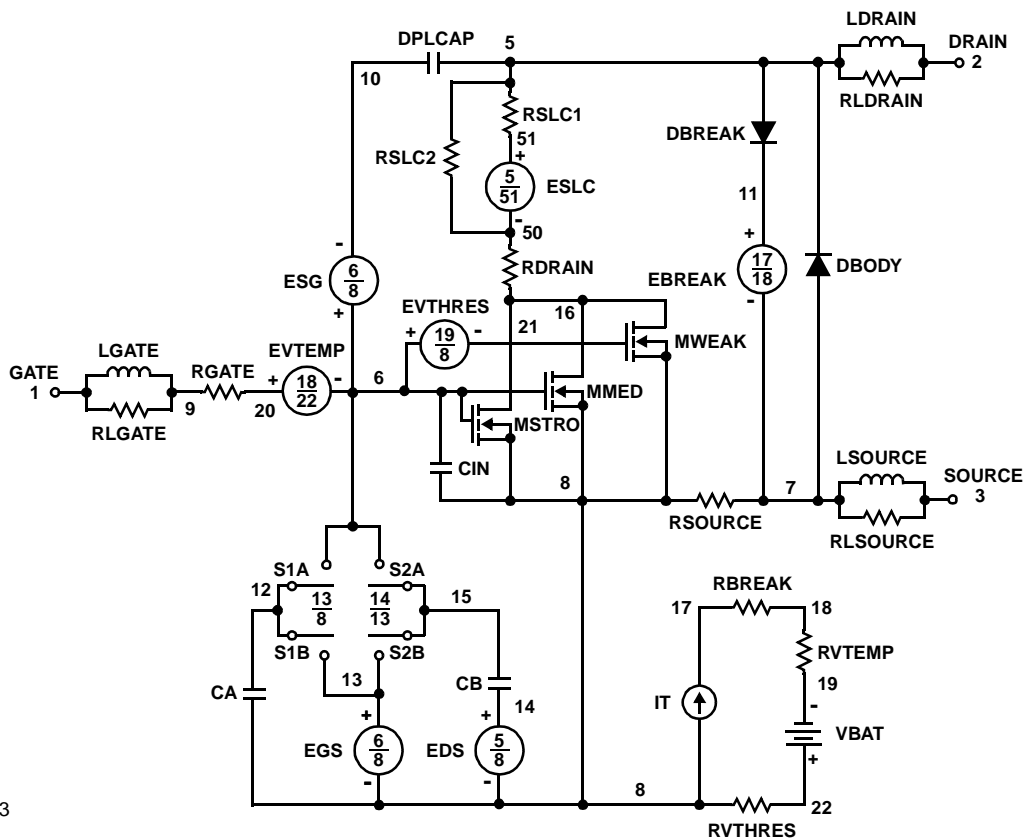
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51)/(1e-6\*1000),3.5))}

.MODEL DBODYMOD D (IS = 1e-12 IKF = 10 RS = 5.6e-3 TRS1 = 5e-4 TRS2 = 1e-6 CJO = 2.23e-9 TT = 2e-7 M = 4e-1 N = 9.9e-1 XTI = 4.75)  
 .MODEL DBREAKMOD D (RS = 1.5e- 1IS = 1e-14 TRS1 = 9e- 4TRS2 = -2e-5 IKF = 1e-1)  
 .MODEL DPLCAPMOD D (CJO = 1.12e- 9IS = 1e-3 0N = 10 M = 6.7e-1 VJ = 1.45)  
 .MODEL MMEDMOD NMOS (VTO = 2 KP = 5.75 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 3.6)  
 .MODEL MSTROMOD NMOS (VTO = 1.62 KP = 2e-2 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 36)  
 .MODEL MWEAKMOD NMOS (VTO = 1.62 KP = 2e-2 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 36)  
 .MODEL RBREAKMOD RES (TC1 = 9.8e- 4TC2 = -1e-10)  
 .MODEL RDRAINMOD RES (TC1 = 2e-2 TC2 = 1e-7)  
 .MODEL RSLCMOD RES (TC1 = 1e-6 TC2 = 1.05e-6)  
 .MODEL RSOURCEMOD RES (TC1 = 5e-4 TC2 = 1e-5)  
 .MODEL RVTHRESMOD RES (TC1 = -2e-3 TC2 = -1.1e-5)  
 .MODEL RVTEMPMOD RES (TC1 = -1.65e- 3TC2 = 1.45e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.3 VOFF = -2.0)  
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.0 VOFF = -4.3)  
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.8 VOFF = 0.5)  
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF = -0.8)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.







**SPICE Thermal Model**

REV August 1998

HUF76129

CTHERM1 th 6 1.10e-5  
 CHERM2 6 5 2.70e-2  
 CHERM3 5 4 3.90e-2  
 CHERM4 4 3 1.00e-2  
 CHERM5 3 2 2.30e-2  
 CHERM6 2 tl 1.80

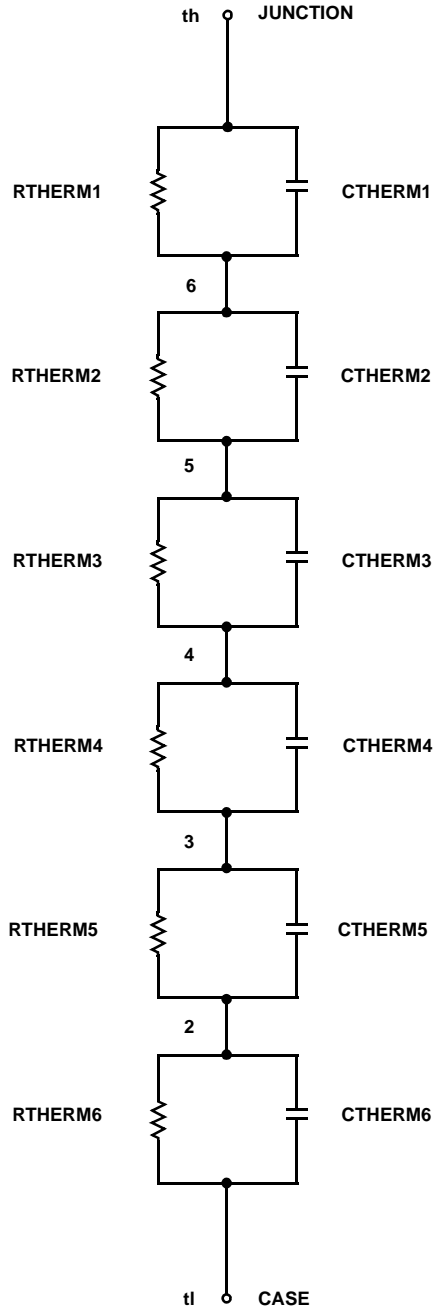
RHERM1 th 6 1.00e-4  
 RHERM2 6 5 5.00e-4  
 RHERM3 5 4 2.90e-2  
 RHERM4 4 3 4.80e-1  
 RHERM5 3 2 2.80e-1  
 RHERM6 2 tl 1.00e-1

**Saber Thermal Model**

Saber thermal model HUF76129

```
template thermal_model th tl
thermal_c th, tl
{
    ctherm.ctherm1 th c2 =1.10e-5
    ctherm.ctherm2 c2 c3 =2.70e-2
    ctherm.ctherm3 c3 c4 =3.90e-2
    ctherm.ctherm4 c4 c5 =1.00e-2
    ctherm.ctherm5 c5 c6 =2.30e-2
    ctherm.ctherm6 c6 tl=1.80

    rtherm.rtherm1 th c2 =1.00e-4
    rtherm.rtherm2 c2 c3 =5.00e-4
    rtherm.rtherm3 c3 c4 =2.90e-2
    rtherm.rtherm4 c4 c5 =4.80e-1
    rtherm.rtherm5 c5 c6 =2.80e-1
    rtherm.rtherm6 c6 tl=1.00e-1
}
```



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Bottomless <sup>TM</sup>	FAST <sub>r</sub> <sup>TM</sup>	OPTOPLANAR <sup>TM</sup>	STAR*POWER <sup>TM</sup>	
CoolFET <sup>TM</sup>	FRFET <sup>TM</sup>	PACMAN <sup>TM</sup>	Stealth <sup>TM</sup>	
CROSSVOLT <sup>TM</sup>	GlobalOptoisolator <sup>TM</sup>	POPT <sup>TM</sup>	SuperSOT <sup>TM</sup> -3	
DenseTrench <sup>TM</sup>	GTO <sup>TM</sup>	Power247 <sup>TM</sup>	SuperSOT <sup>TM</sup> -6	
DOMET <sup>TM</sup>	HiSeC <sup>TM</sup>	PowerTrench <sup>®</sup>	SuperSOT <sup>TM</sup> -8	
EcoSPARK <sup>TM</sup>	ISOPLANAR <sup>TM</sup>	QFET <sup>TM</sup>	SyncFET <sup>TM</sup>	
E <sup>2</sup> CMOS <sup>TM</sup>	LittleFET <sup>TM</sup>	QST <sup>TM</sup>	TinyLogic <sup>TM</sup>	
EnSigna <sup>TM</sup>	MicroFET <sup>TM</sup>	QT Optoelectronics <sup>TM</sup>	TruTranslation <sup>TM</sup>	
FACT <sup>TM</sup>	MicroPak <sup>TM</sup>	Quiet Series <sup>TM</sup>	UHC <sup>TM</sup>	
FACT Quiet Series <sup>TM</sup>	MICROWIRE <sup>TM</sup>	SILENT SWITCHER <sup>®</sup>	UltraFET <sup>®</sup>	

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

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