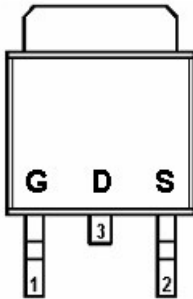


DESCRIPTION

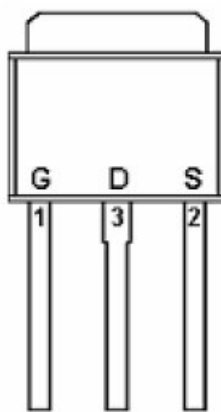
STN442D is used trench technology to provide excellent $R_{DS(on)}$ and gate charge. Those devices are suitable for use as load switch or in PWM applications.

PIN CONFIGURATION (D-PAK)

TO-252



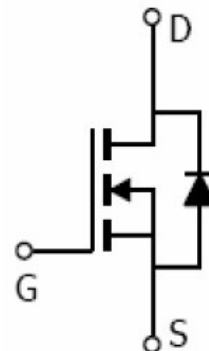
TO-251



FEATURE

- 60V/20.0A, $R_{DS(on)} = 24m\Omega$ (Typ.) @ $V_{GS} = 10V$
- 60V/20.0A, $R_{DS(on)} = 31m\Omega$ @ $V_{GS} = 4.5V$
- Super high density cell design for extremely low $R_{DS(on)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252, TO-251 package design

PART MARKING



Y: Year Code A: Process Code

**STN442D**

N Channel Enhancement Mode MOSFET

27.0A

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	VDSS	60	V
Gate-Source Voltage	VGSS	±20	V
Continuous Drain Current (TJ=150°C)	ID	27.0 20.0	A
Pulsed Drain Current	IDM	40	A
Continuous Source Current (Diode Conduction)	IS	22	A
Power Dissipation	PD	50 25	W
Operation Junction Temperature	TJ	175	°C
Storage Temperature Range	TSTG	-55/175	°C
Thermal Resistance-Junction to Ambient	RθJA	62	°C/W

ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250mA$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		2.5	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=48V, V_{GS}=0V$			1	μA
		$V_{DS}=48V, V_{GS}=0V$ $T_J=55^{\circ}C$			5	
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$ $V_{GS}=4.5V, I_D=20A$		30 22	37 28	$m\Omega$
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=20A$		60		S
Diode Forward Voltage	V_{SD}	$I_S=1.0A, V_{GS}=0V$		0.7	1.0	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=10V, V_{DS}=30V$ $I_D=20A$			30	nC
Gate-Source Charge	Q_{gs}				10	
Gate-Drain Charge	Q_{gd}				12	
Input Capacitance	C_{iss}	$V_{DS}=20V, V_{GS}=0V$ $F=1MHz$		1080		pF
Output Capacitance	C_{oss}			180		
Reverse Transfer Capacitance	C_{rss}			58		
Turn-On Time	$t_{d(on)}$ t_r	$V_{DD}=20V, R_L=4\Omega$ $I_D=5.0A, V_{GEN}=10V$ $R_G=1\Omega$		20		nS
Turn-Off Time	$t_{d(off)}$ t_f			25		
				40		
				42		

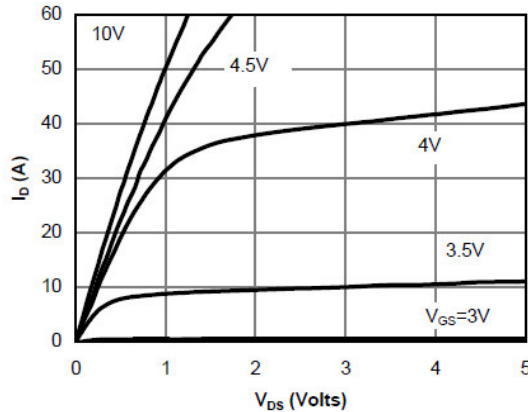
TYPICAL CHARACTERISTICS


Fig 1: On-Region Characteristics (Note E)

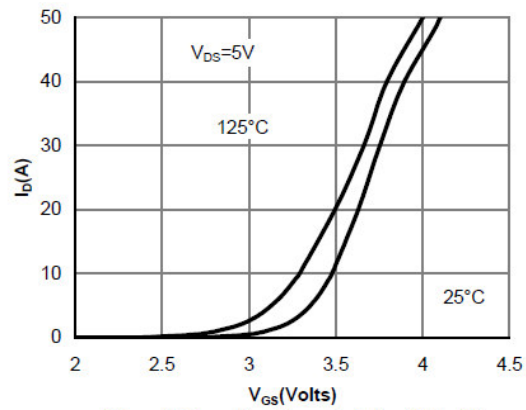


Figure 2: Transfer Characteristics (Note E)

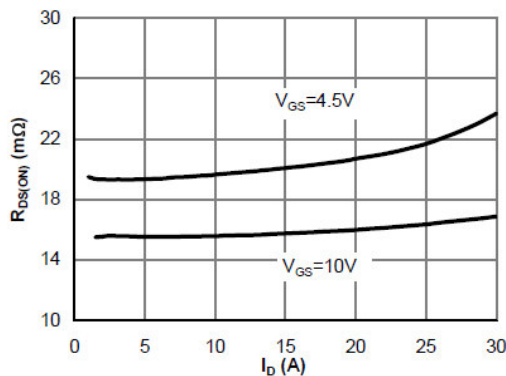


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

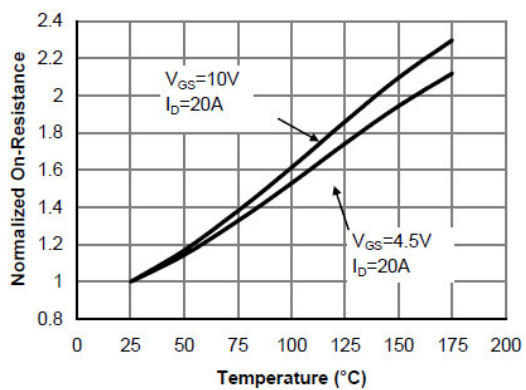


Figure 4: On-Resistance vs. Junction Temperature (Note E)

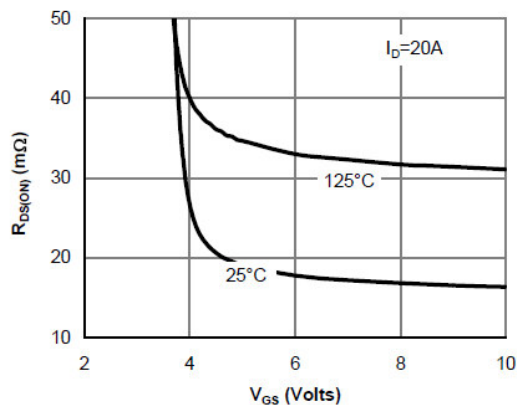


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

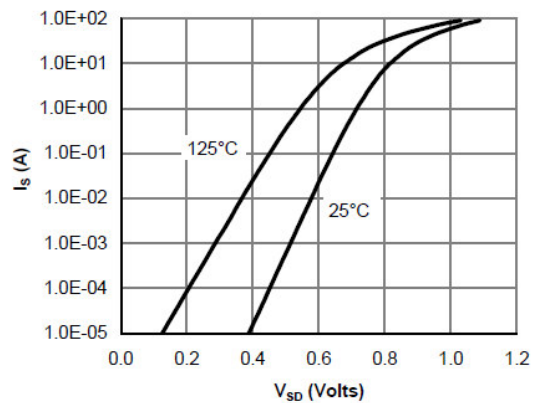


Figure 6: Body-Diode Characteristics (Note E)

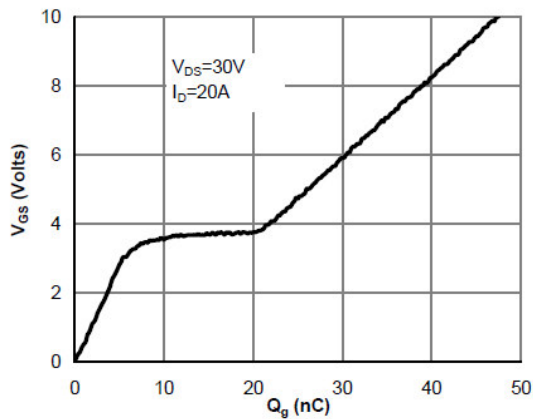
TYPICAL CHARACTERISTICS


Figure 7: Gate-Charge Characteristics

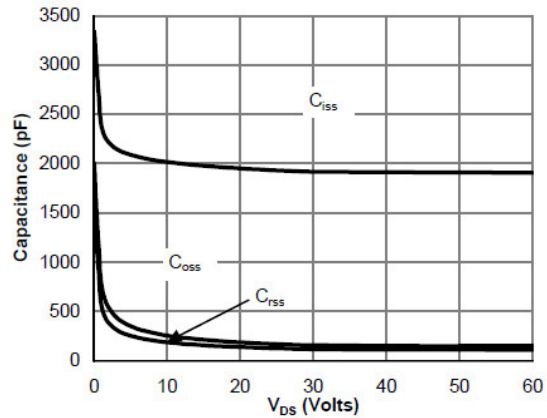


Figure 8: Capacitance Characteristics

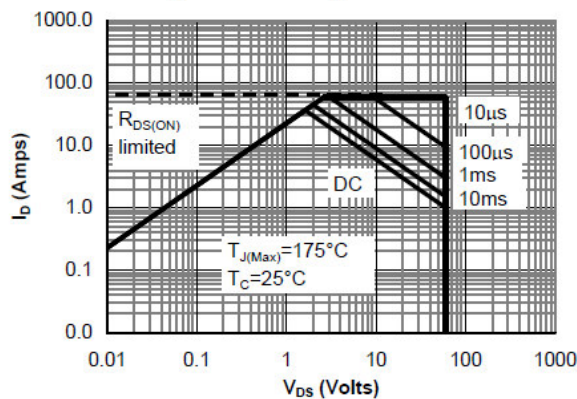


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

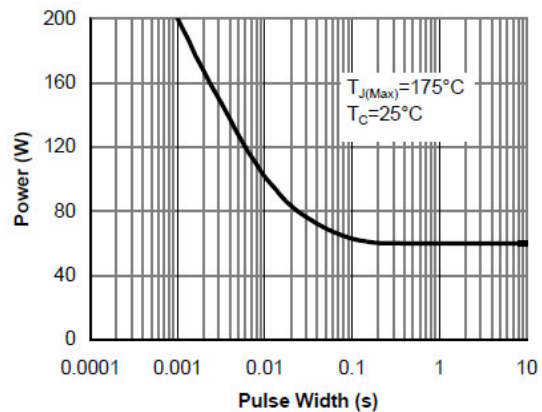


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

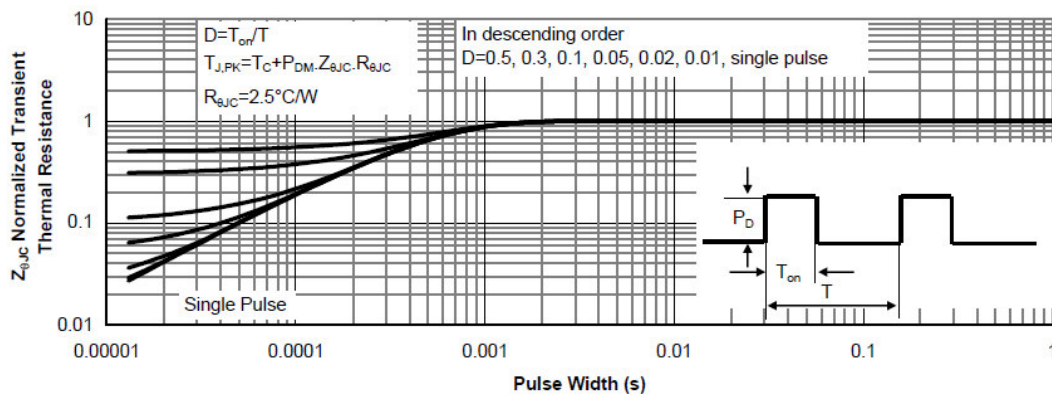


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

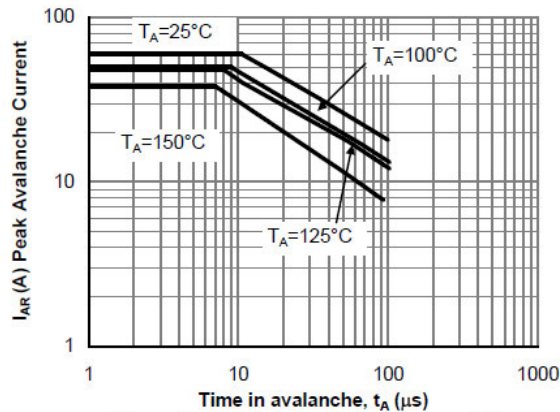
TYPICAL CHARACTERISTICS


Figure 12: Single Pulse Avalanche capability (Note C)

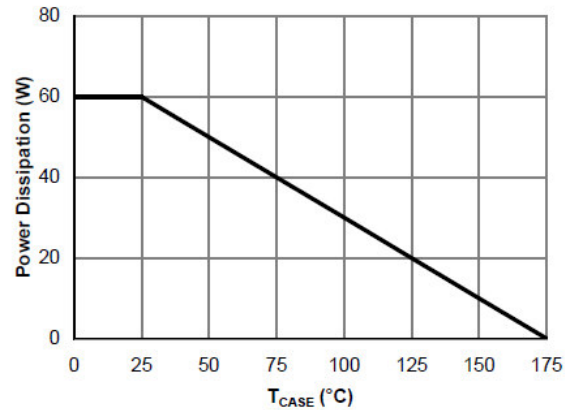


Figure 13: Power De-rating (Note F)

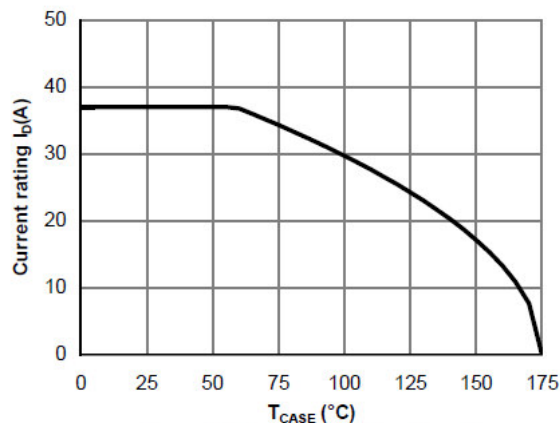


Figure 14: Current De-rating (Note F)

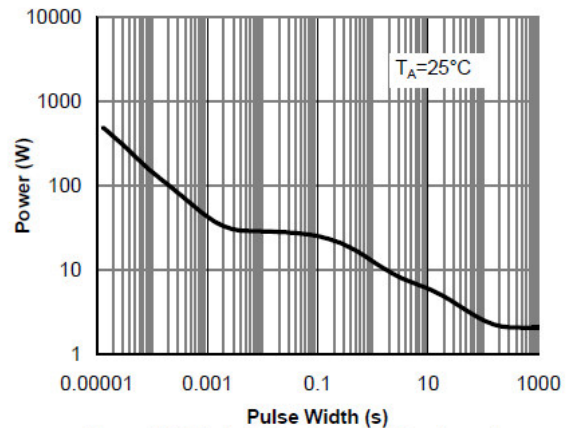


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

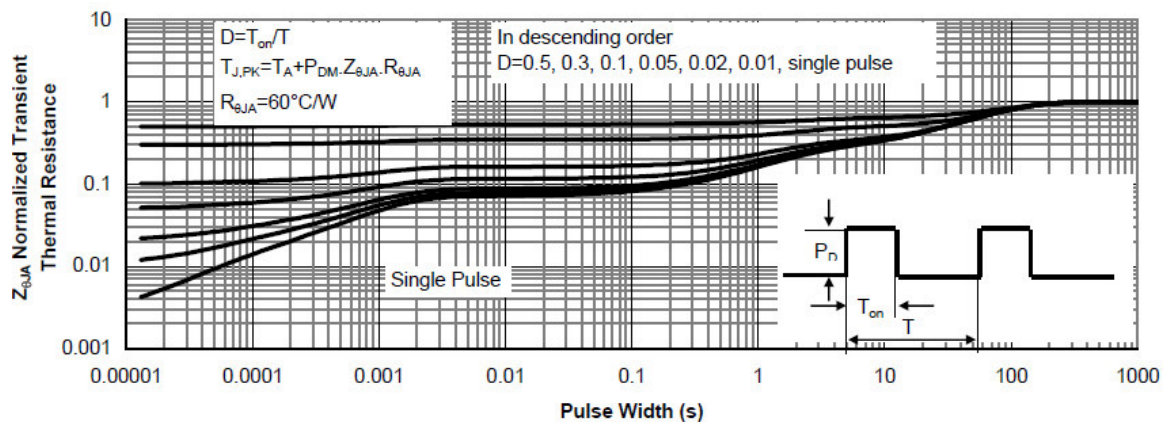
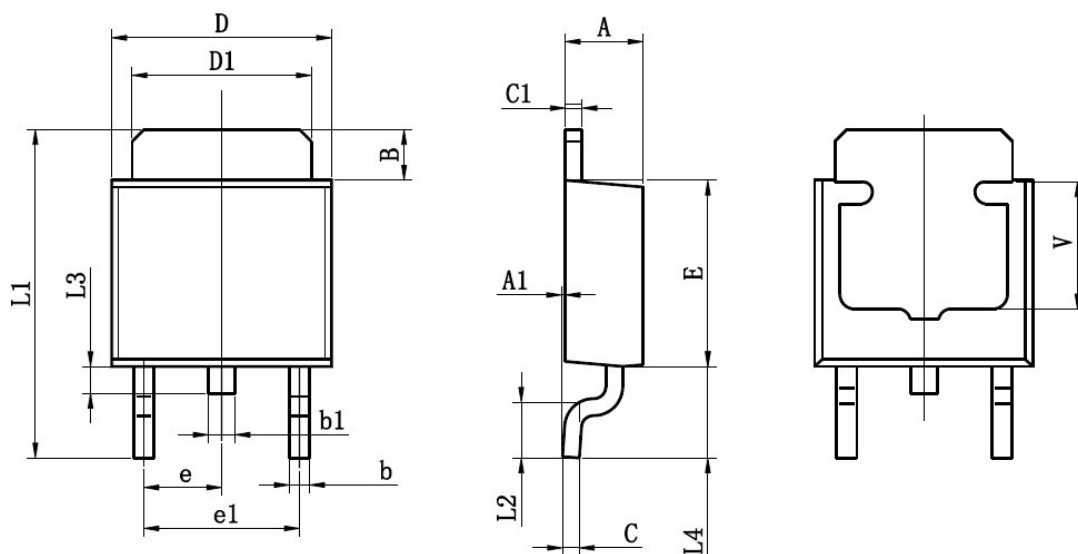


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

T

TO-252-2L PACKAGE OUTLINE SOP-8P


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300TYP		0.091TYP	
e1	4.500	4.700	0.177	0.185
L1	9.500	9.900	0.374	0.390
L2	1.400	1.780	0.055	0.070
L3	0.650	0.950	0.026	0.037
L4	2.550	2.900	0.100	0.114
V	3.80REF		0.150REF	