UC3855A/B High Performance Power Factor Preregulator

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ABSTRACT

The trend in power converters is towards increasingly higher power densities. Usually, the method to achieve this is to increase the switching frequency, which allows a reduction in the filter component's size. Raising the switching frequency however, significantly increases the system switching losses which generally precludes operating at switching frequencies greater than 100 kHz.

1 Introduction

In order to increase the switching frequency while maintaining acceptable efficiency, several soft switching techniques have been developed [1,2,3]. Most of these resonant techniques increase the semiconductor current and/or voltage stress, leading to larger devices and increased conduction losses due to greater circulating current. A new class of converters has been developed [4], however, that allow an increase in switching frequency without the associated increase in switching losses, while overcoming most of the disadvantages of the resonant techniques. Zero voltage transition (ZVT) converters operate at a fixed frequency while achieving zero voltage turn-on of the main switch and zero current turn-off of the boost diode. This is accomplished by employing resonant operation only during switch transitions. During the rest of the cycle, the resonant network is essentially removed from the circuit and converter operation is identical to its nonresonant counterpart.

This technique allows a improvement in efficiency over the traditional boost converter, as well as operating the boost diode with reduced stress (due to controlled di/dt at turn-off). Soft-switching of the diode also reduces EMI, an important system consideration.

Active power factor correction programs the input current of the converter to follow the line voltage and power factors of 0.999 with THD of 3% are possible. The Unitrode UC3855A/B IC incorporates power factor correction control circuitry capable of providing high power factor with several enhancements relating to current sensing and ZVT operation of the power stage.

The UC3855 incorporates all of the control functions required to design a ZVT power stage with average current mode control. Average current mode control has been chosen for its ability to accurately program the input current while avoiding the slope compensation and poor noise immunity of other methods [5,6].

1.1 ZVT Technique

1.1.1 ZVT Boost Converter Power Stage

The ZVT boost converter operates the same as a conventional boost converter throughout its switching cycle except during the switch transitions. Figure 1 shows the ZVT boost power stage. The ZVT network, consisting of Q_{ZVT} , D2, L_r, and C_r, provides active snubbing of the boost diode and main switch. The ZVT circuit operation has been described in [4, 7, 8] and are reviewed here for completeness. Referring to Figure 2, the following timing intervals can be defined:

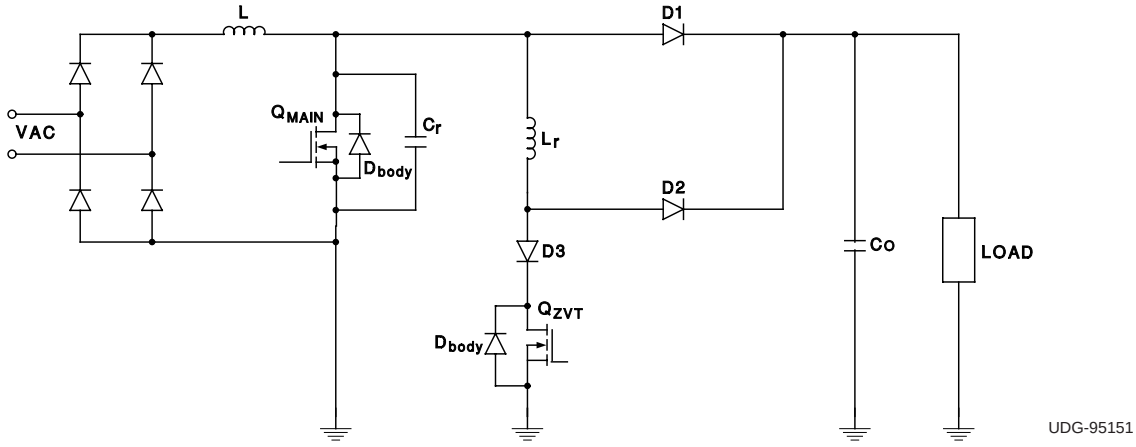


Figure 1. Boost Converter with ZVT Power Stage

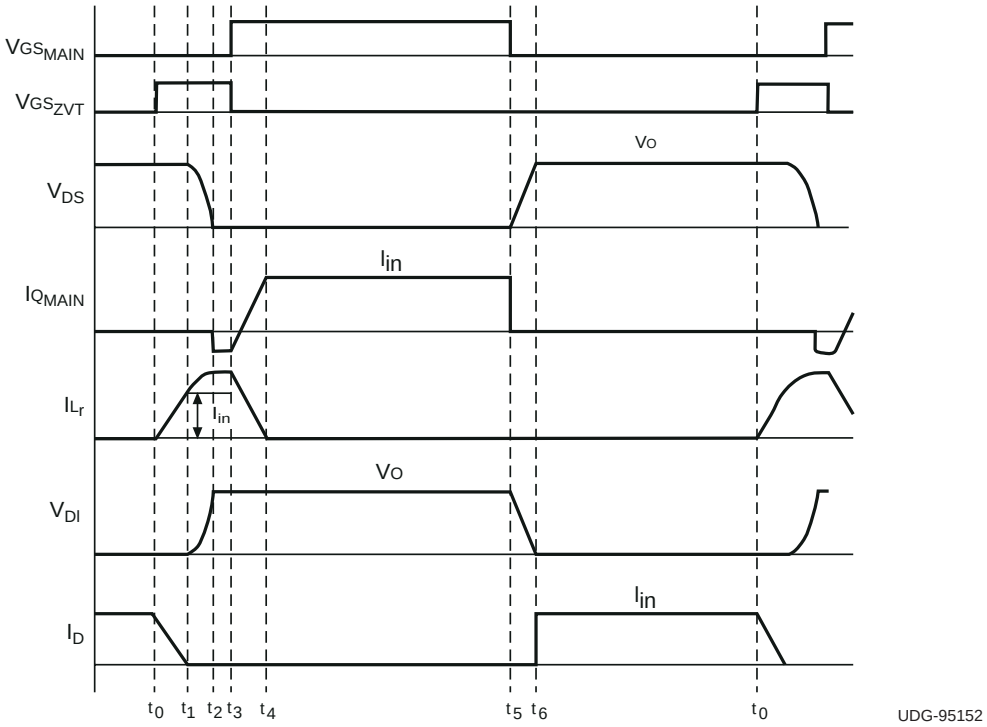


Figure 2. ZVT Timing Diagram

1.1.2 ZVT Timing

1.1.2.1 $t_0 - t_1$

During the time prior to t_0, the main switch is off and diode D1 is conducting the full load current. At t_0, the auxiliary switch (Q_{ZVT}) is turned on. With the auxiliary switch on, the current in L_r ramps up linearly to I_{IN}. During this time the current in diode D1 is ramping down. When the diode current reaches zero the diode turns off (i.e. soft switching of D1). In the practical circuit some reverse recovery of the diode occurs since the diode needs time to remove the junction charge. The voltage across the ZVT inductor is V_O, and therefore the time required to ramp up to Iin is:

$$t_{01} = \frac{I_{IN}}{\left(\frac{V_O}{L_r}\right)}$$

1.1.2.2 $t_1 - t_2$

At t_1, the L_r current has reached I_{IN} and L_r and C_r begins to resonate. This resonant cycle discharges C_r until its voltage equals zero. The dv/dt of the drain voltage is controlled by C_r (C_r is the combination of the external C_{DS} and C_{OSS}). The current through L_r continues to increase while C_r discharges. The time required for the drain voltage to reach zero is 1/4 of the resonant period. At the end of this period the body diode of the main switch turns on.

$$t_{12} = \frac{\pi}{2} \times \sqrt{L_r C_r}$$

1.1.2.3 $t_2 - t_3$

At the beginning of this interval the switch drain voltage has reached 0 V and the body diode is turned on. The current through the body diode is being driven by the ZVT inductor. The voltage across the inductor is zero and therefore the current freewheels. At this time, the main switch can be turned on to achieve zero voltage switching.

1.1.2.4 $t_3 - t_4$

At t_3, the UC3855 senses that the drain voltage of Q_{MAIN} has fallen to zero and turns on the main switch while turning off the ZVT switch. After the ZVT switch turns off, the energy in L_r is discharged linearly through D2 to the load.

1.1.2.5 $t_4 - t_5$

At t_4, the current in D2 goes to zero. When this occurs, the circuit is operating like a conventional boost converter. In a practical circuit however, L_r resonates with C_{OSS} of the ZVT switch driving the node at the anode of D1 negative (since the opposite end of L_r is clamped to zero). This effect is discussed in the ZVT circuit design section.

1.1.2.6 $t_5 - t_6$

This stage is also exactly like a conventional boost converter. The main switch turns off. The Q_{MAIN} drain-to-source node capacitance charges to V_O and the main diode begins to supply current to the load. Since the node capacitance initially holds the drain voltage to zero, the turn off losses are significantly reduced.

It can be seen through the above description that the operation of the converter differs from the conventional boost only during the turn-on switch transitions. The main power stage components experience no more voltage or current stress than normal, and the switch and diode both experience soft switching transitions. Having significantly reduced the switching losses, the operating frequency can be increased without an efficiency penalty. The diode also operates with much lower losses and therefore operates at a lower temperature, increasing reliability. The soft switching transitions also reduce EMI, primarily caused by hard turn-off of the boost diode.

1.1.3 Control Circuit Requirements

In order to maintain zero voltage switching for the main switch, the ZVT switch must be on until the voltage on C_r resonates to zero. This can be accomplished by using a fixed delay equal to t_{ZVT} at low line and maximum load.

$$t_{ZVT} = \frac{I_{IN(p)} \times L_r}{V_O} + \frac{\pi}{2} \times \sqrt{L_r \times C_r}$$

However, this would give a longer than necessary delay at lighter load or higher line conditions, and therefore would increase the ZVT circuit conduction loss and increase the peak current stress. The UC3855 allows for a variable t_{ZVT} by sensing when the Q_{MAIN} drain voltage has fallen to zero. Once the voltage falls below the ZVS pin threshold voltage (2.5 V), the ZVT gate drive signal is terminated and the main switch gate drive goes high. The control waveforms are shown in Figure 3. The switching period begins when the oscillator begins to discharge, and the ZVT gate drive goes high at the beginning of the discharge period. The ZVT signal stays high until the ZVS pin senses the zero voltage condition or until the discharge period is over (the oscillator discharge time is the maximum ZVT pulse width). This allows the ZVT switch to be on only for as long as necessary.

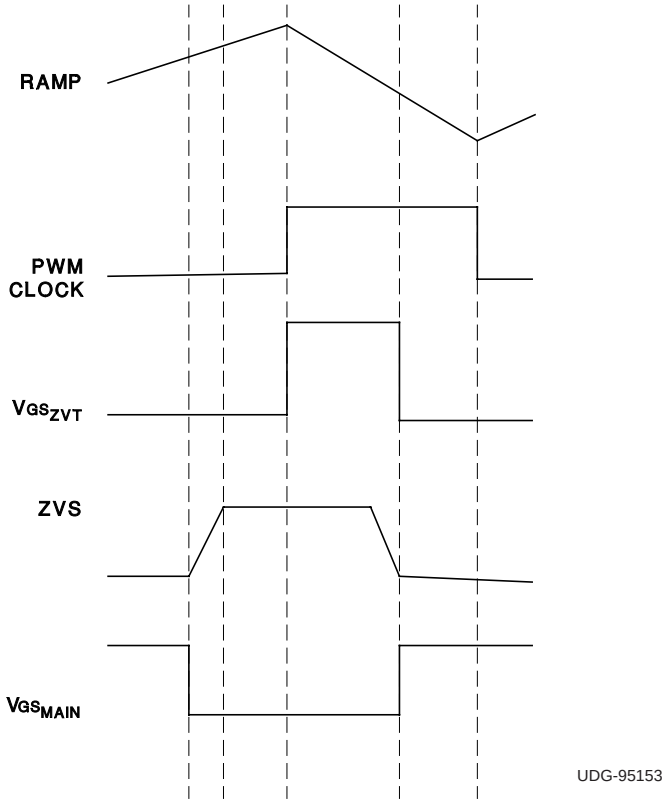


Figure 3. ZVT Control Waveforms

2 Control Circuit Operation and Design

Figure 4 shows the UC3855A/B block diagram (pin numbers correspond to DIL−20 packages). It shows a controller which incorporates the basic PFC circuitry, including average current mode control, and the drive circuitry to facilitate ZVT operation. The device also has current waveform synthesizer circuitry to simplify current sensing, as well as overvoltage and overcurrent protection. In the following sections the control device is broken down into functional blocks and individually reviewed.

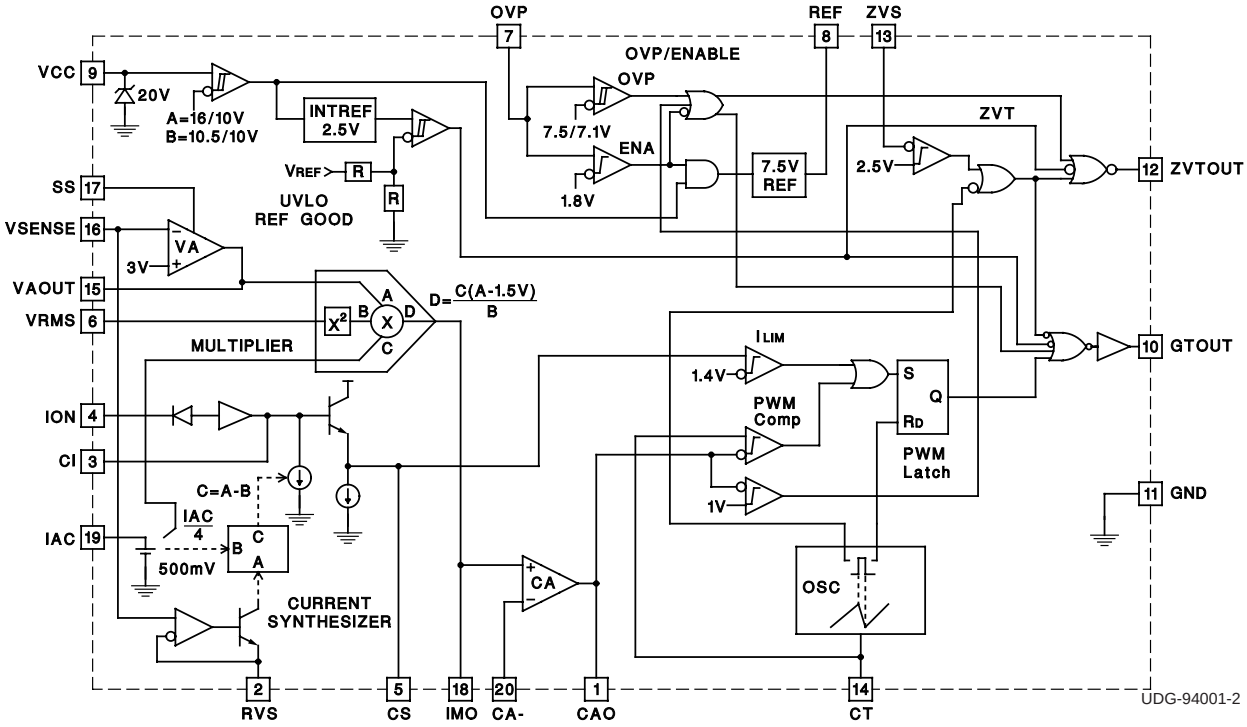


Figure 4. UC3855 Controller Block Diagram

2.1 Comparison with UC3854A/B

The PFC section of the UC3855A/B is identical to the UC3854A/B. Several common design parameters are highlighted below to illustrate the similarities.

FUNCTION	UC3854A/B	UC3855A/B
Enable	Dedicated pin	Incorporated into OVP
Design range for VRMS	1.5 V to 4.7 V	1.5 V to 4.7 V
VREF for VA	3 V	3 V
Maximum VA output voltage	6 V	6 V
Offset voltage at IAC	0.5 V	0.7 V
Multiplier gain	$\frac{IAC(VA - 1.5)}{V_{RMS}^2 \times IMO}$	$\frac{IAC(VA - 1.5)}{V_{RMS}^2 \times IMO}$

New features incorporated into the UC3855A/B include:

- ZVT control circuitry
- Overvoltage protection
- Current synthesizer

2.2 Oscillator

The oscillator contains an internal current source and sink and therefore only requires an external timing capacitor (CT) to set the frequency. The nominal charge current is set to 500 μA and the discharge current is 8 mA. The discharge time is approximately 6% of the total period, which defines the maximum ZVT time. CT is calculated by:

$$CT = \frac{1}{11200 \times f_S}$$

2.3 ZVT Control Circuit

As stated in the ZVT Technique section, the UC3855A/B provides the control logic to ensure ZVT operation over all line and load conditions without using a fixed delay. The ZVS pin senses the MOSFET drain voltage and is an input to the ZVT drive comparator. The other comparator input is internally biased to 2.5 V. When the ZVS input is above 2.5 V (and the PWM clock signal is present) the ZVT drive signal can go high. Pulling the ZVS pin low terminates the ZVT drive signal and turn on the main switch output (recall that the maximum ZVT output signal is equal to the oscillator discharge time). The network used to sense the node voltage is shown in Figure 5. R12 pulls up the pin to a maximum of 7.5 V, and C6 provides filtering.

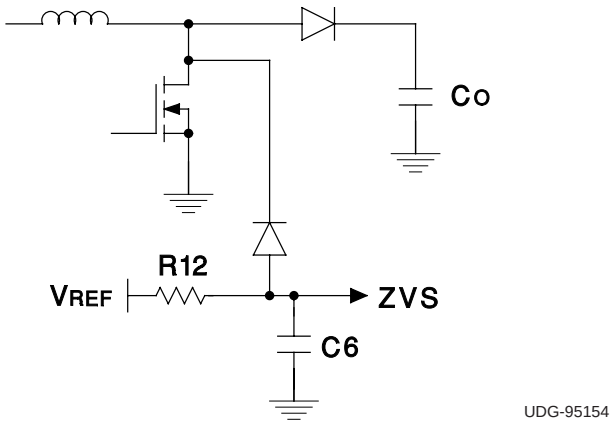


Figure 5. ZVS Sensing Circuit

The RC time constant should be fast enough to reach 2.5 V at maximum duty cycle. The drain voltage is limited by the node capacitance which slows down the dv/dt across the main MOSFET, which reduces the high speed requirement on the ZVS circuit. The maximum ZVS pin voltage should be limited to VREF, otherwise the ZVS circuitry can become latched and does not operate properly.

An alternative method for ZVS operation, is to sense the drain voltage through a simple voltage divider. This voltage still has to be filtered (and clamped) however, so as not to inject noise into the ZVS pin.

Refer back to Figure 3 for the timing waveforms.

3 Gate Drives

The main drive can source 1.5 A_{PK} and the ZVT drive is 0.75 A_{PK}. The main switch drive impedance requirements are reduced due to ZVT operation. At turn-on the drain voltage is at zero volts and therefore the Miller capacitance effect is not an issue, and during turn-off, the dv/dt is limited by the resonant capacitor. Since the ZVT MOSFET is generally at least two die sizes smaller than the main switch, its drive requirements are met with a lower peak current capability.

3.1 Multiplier/Divider Circuit

The multiplier section of the UC3855A/B is identical to the UC3854A/B. It incorporates input voltage feedforward (through the V_{RMS} input) to eliminate loop gain dependence on the input voltage. There are only three parameters (V_{VRMS}, I_{IAC}, and R_{IMO}) that need to be defined to properly set up the device.

3.1.1 VRMS

The multiplier programs the line current and therefore effects the power drawn from the line. The VRMS pin is programmed by looking at the system power limits. Referring to the block diagram (Figure 4), the multiplier output equation is:

$$I_{IMO} = \frac{I_{IAC} \times \left(V_{EA} - 1.5\right)}{V^2_{VRMS}}$$

The power limit function is set by the maximum output voltage of the voltage loop error amplifier, V_{EA} (6 V). The power limiting function is easily explained by looking at what happens for a given value of V_{EA} . If the AC line decreases by a factor of two, the feedforward voltage effect (V^2_{VRMS}) decreases to one fourth. This increases multiplier output current (and therefore line current) by two. The power drawn from the line has therefore remained constant. Conversely, if the load increases and the line stays constant, V_{EA} increases, causing more line current to be drawn. It can be seen then, that V_{EA} is a voltage proportional to input power.

Normally the multiplier is set to limit maximum power at low line, corresponding to maximum error amplifier output voltage. The multiplier equation can be solved for the feedforward voltage that corresponds to maximum error amplifier voltage and maximum multiplier current (internally limited to 2 times I_{IAC}).

$$V^2_{VRMS} = \frac{I_{IAC} \times \left(V_{EA} - 1.5\right)}{2 \times \left(I_{IAC}\right)}$$

$$V^2_{VRMS} = 1.5$$

Knowing the VRMS voltage at low line defines the voltage divider from the line to VRMS pin. This feedforward voltage must be relatively free of ripple in order to reduce the amount of second order harmonic that is present at the multiplier input (which in turn would cause 3rd order harmonics in the input current) [9]. The filtering produces a dc voltage at the VRMS pin. Since the input voltage is defined in terms of its RMS value, the dc to RMS factor (0.9) must be taken into account [9]. For example, if the low line voltage is 85 V, the attenuation required is:

$$\frac{85\ V_{RMS} \times (0.9)}{1.5 \times V_{DC}} = 51 : 1$$

At a high line of 270 V, this corresponds to V_{VRMS} = 4.76 V. The common mode range of the VRMS input is 0 V to 5.5 V. The calculated range is therefore within the accepted limits.

A two pole filter is recommended to provide adequate attenuation without degrading the feedforward transient response. A single pole filter requires a pole at too low of a frequency to still allow VRMS to respond quickly enough to changes in line voltage.

The filter poles can be calculated once the distortion contribution from V_{RMS} is determined. If the feedforward circuit's contribution to the total distortion is limited to 1.5%, the required attenuation of the filter can be calculated. Recall that the percentage of 2nd harmonic in a full wave rectified sinewave is approximately 66.7% of the dc value. The percentage of second harmonic translates to the same percent 3rd harmonic distortion in the input current waveform [9]. Therefore, the filter attenuation required is:

$$\frac{1.5\%}{66.7\%} = 0.0025$$

The individual stages should have an attenuation of $\sqrt{0.0225}$ or 0.15. For a single stage filter:

$$A_V = \frac{f_C}{f} \Rightarrow f_C = 120\ Hz(0.15) = 18\ Hz$$

Referring to Figure 6 the components correspond to R9A = R9B = 390 kΩ, R10 = 120 kΩ, and R11 = 18 kΩ with C4 = 0.082 µF and C5 = 0.47 µF.

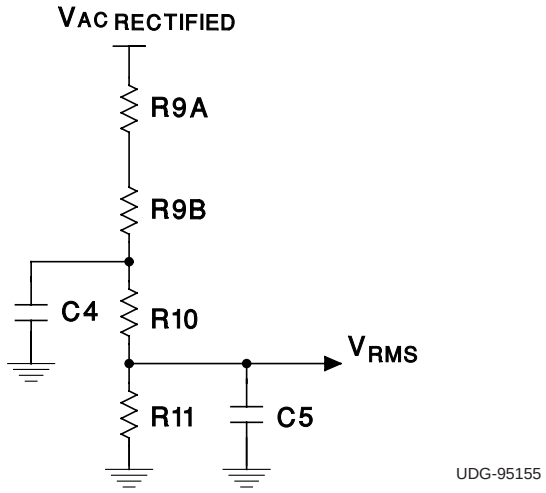


Figure 6. V_{RMS} Circuit

3.1.2 I_{IAC}

The value of I_{IAC} is chosen to be 500 µA at high line. This value is somewhat arbitrary, however it should be kept below 1 mA to stay within the linear region of the multiplier. This corresponds to a total resistance of approximately 766 kΩ from the line to IAC pin.

3.1.3 R_{IMO}

The multiplier output resistor can be calculated by recognizing that at low line and maximum load current, the multiplier output voltage equals 1 V (in order to stay below the overcurrent trip point). This also corresponds to the maximum sense voltage of the current transformer. The multiplier current under this condition is equal to 1 V/R_{IMO}, and can be equated with the multiplier equation which yields:

$$\frac{1\ V}{R_{IMO}} = \frac{I_{IAC} \times \left(V_{EA} - 1.5\right)}{V^2_{VRMS}}$$

At low line I_{IAC} equals 156 µA (if low line = 85 V and I_{IAC} was set to 500 µA at 270 V), V_{EA} is at its maximum of 6 V, and V_{VRMS} is 1.5 V. Therefore R_{IMO} equals 3.2 kΩ.

3.2 Current Synthesizer

Current sensing is simplified due to the current synthesis function built into the UC3855A/B. Switch current is the same as inductor current when the switch is on and can be sensed using a single current transformer. The current synthesizer charges a capacitor (CI) with a current proportional to the switch current when the switch is on. During the switch off-time, the inductor current waveform is reconstructed by the controller. To get an accurate measure of the inductor current then, all that is required is to reconstruct the down slope of the inductor current, which is given by:

$$\frac{\Delta i}{\Delta t} = \frac{V_{OUT} - V_{AC}}{L}$$

Discharging CI with a current proportional to $V_{OUT} - V_{AC}$ allows reconstruction of the inductor current waveform. The capacitor down slope is:

$$\frac{\Delta Vi}{\Delta t} = \frac{I_{DIS}}{CI}$$

The UC3855A/B develops I_{DIS} by subtracting $I_{IAC}/4$, from a current proportional to V_{OUT}. The voltage at the RVS pin is regulated at 3 V and therefore picking the RVS resistor sets the current proportional to V_{OUT}.

$$I_{DIS} = \frac{3\ V}{R_{RVS}} - \frac{I_{IAC}}{4}$$

The ratio of the current in $R_R$vs to $I_{IAC}/4$ should equal the ratio of V_{OUT} to V_{AC}. Therefore if I_{IAC} / 4 is 125 μA, the current through R_{RVS} should be set to 130 μA.

$$R_{RVS} = \frac{3\ V}{130\ \mu A} = 23\ k\Omega,\ use\ 22\ k\Omega$$

Equating inductor current slope with capacitor voltage slope, and recognizing that maximum slope occurs when V_{AC} equals zero, CI can be solved for:

$$CI = \frac{3 \times L \times N}{R_{RVS} \times V_{OUT} \times R_S}$$

where N is the current transformer (CT) turns ratio, (N_S / N_P) and R_S is the current sense resistor.

The current synthesizer has approximately 20 mV of offset. This offset can cause distortion at the zero crossing of the line current. To null out this offset, a resistor can be connected between VREF and the IMO pin. The resistor value is calculated based on R_{IMO} and the offset at the output of the synthesizer. For a 20-mV offset and R_{IMO} = 3.3 kΩ a resistor from V_{REF} to IMO of 1.2 MΩ cancels the offset.

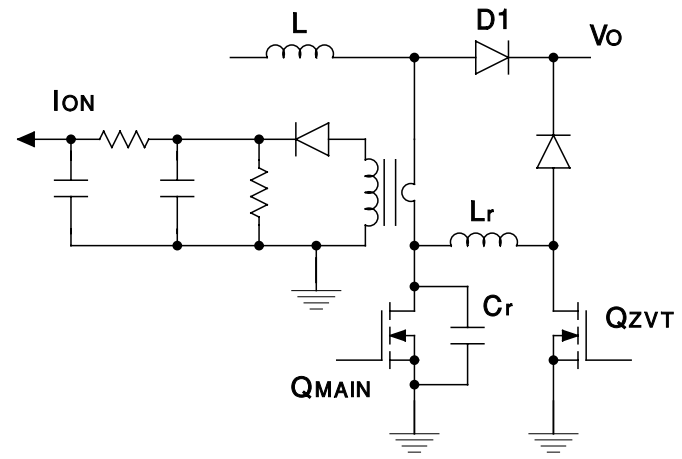
3.3 Current Sensing

3.3.1 Current Transformer

As was seen in the previous section, synthesizing inductor current with the UC3855A/B is quite simple. Only switch current needs to be sensed directly, and this is most efficiently done with a current sense transformer. Resistive sensing at this power level would result in excessive power dissipation.

Several issues should be kept in mind when implementing the current transformer. At frequencies of a couple hundred kilohertz, core reset needs to be addressed. Contributing to the difficulty is the very high duty cycles inherent in a power factor correction circuit. In addition, the ZVT circuit can complicate the sensing/reset function. When the ZVT circuit turns on, it draws current from the line. In order to minimize line current distortion, this current should be measured. Placing the resonant inductor after the current transformer ensures that the ZVT circuit current is measured. Similarly, when the main switch turns off, current continues to flow into the resonant capacitor. While it is important to measure this current, if the capacitor is connected to the drain of the MOSFET, below the current transformer, this current *eats* into the minimal reset time available at line zero crossings, where duty cycles are approaching 100%. This configuration is shown in Figure 7A. If the current transformer does not have enough time to reset, it can begin to saturate and lose accuracy, even if complete saturation is avoided, causing distortion at the zero crossings. A better configuration is shown in Figure 7B. In this circuit, the capacitor current is measured when it discharges during the ZVT circuit on time. Since this occurs at the beginning of the switching cycle, the current transformer does not lose any of its reset time. Connecting C_r above the current transformer does not adversely affect the MOSFET dv/dt control. Since the device is controlling average current, it does not matter whether the capacitor current is measured at the beginning or end of the switching cycle.

Figure 7 also shows that filtering is added to the transformer secondary in order to reduce noise filtering. The bandwidth of this filter should be low enough to reduce switching noise without degrading the switch current waveform.



7A.

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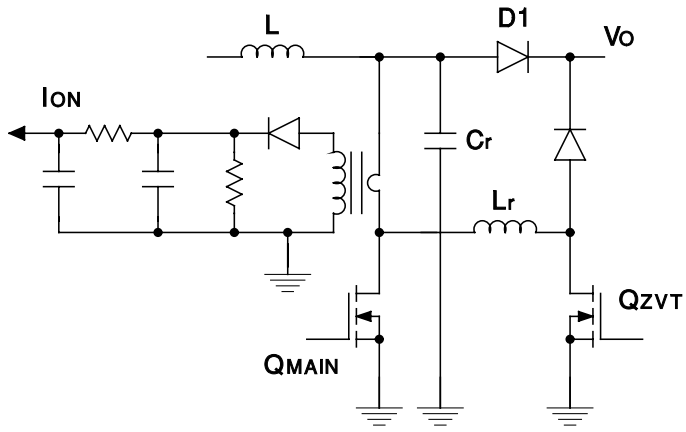

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7B.

Figure 7. Curent Transformer Sensing

In addition to position and reset considerations, actual current transformer construction must be considered. Using current transformers that have been designed and manufactured for operation at 20 kHz will not give good performance at switching frequencies of 100 kHz and greater. Low frequency designs generally have too much leakage inductance to be used for high frequency operation and can cause inaccurate sensing and/or noise problems.

3.3.2 Resistive Sensing

Resistive sensing is still possible with the UC3855A/B. Since both inputs to the current error amplifier are available to the user, resistive sensing is easy to implement. Figure 8 shows the typical configuration. The common mode range of the current error amplifier is −0.3 V to 5.0 V. The R_{IMO} value remains the same as was calculated above if the maximum signal level remains at 1 V. This also allows the resistively sensed signal to be fed into I_{ON} from the junction of R_{SENSE} and R_I and used for peak current limiting. A filter to eliminate the gate drive current effects is recommended. It is recommended that the RVS resistor still be connected and a resistor connected from CS to ground in order to eliminate the possibility of noise being injected into these high impedance nodes.

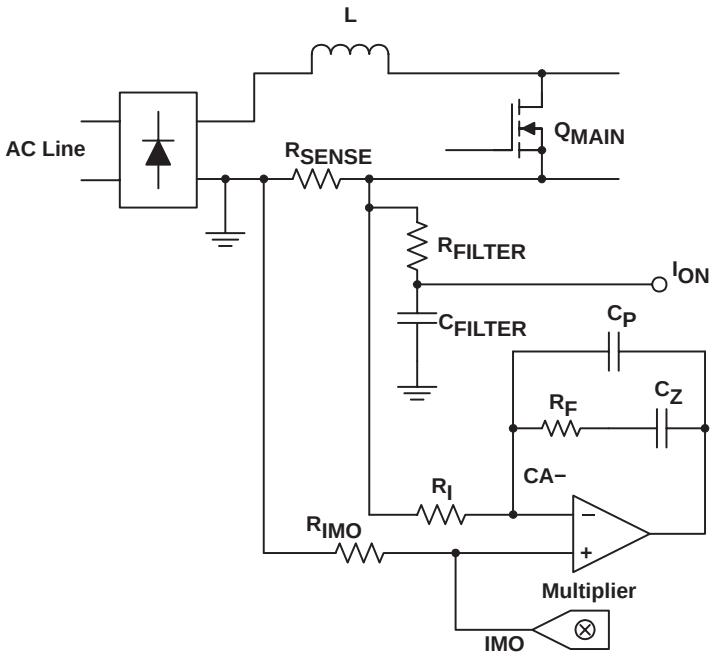
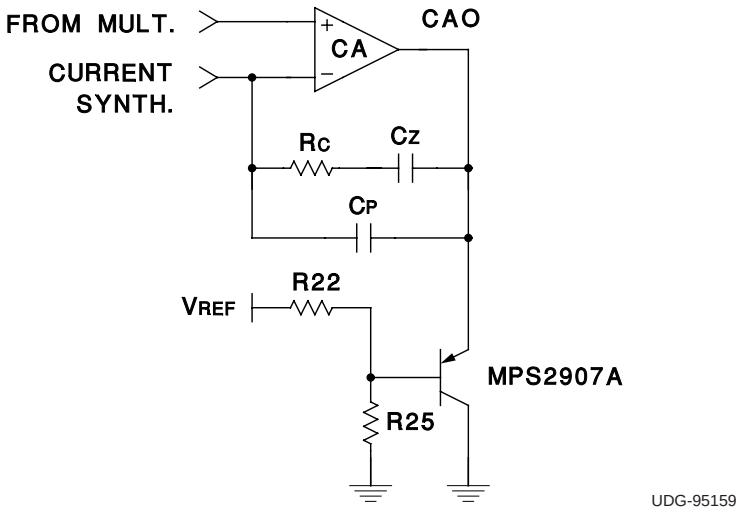


Figure 8. Resistive Sensing

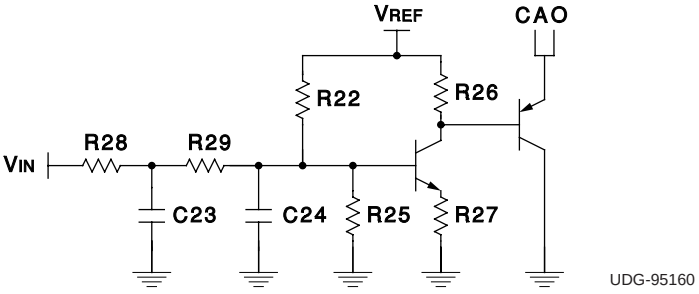
3.4 Current Error Amplifier

The current error amplifier ensures that the input current drawn from the line follows the sinusoidal reference. The positive input to the amplifier is the multiplier output. The negative input is connected to the output of the current synthesizer (CS) through a resistor (usually the same value as R_{IMO}). The output of the current error amplifier is compared to the sawtooth waveform at the PWM comparator and terminates the duty cycle accordingly. At zero crossings of the line, the duty cycle is at its maximum. Since the duty cycle is approaching 100%, proper reset of the current transformer becomes increasingly difficult. Standard PWM controllers terminate the duty cycle during the oscillator discharge time, however, due to the ZVT operation, the UC3855A/B is capable of achieving 100% on-time. If the duty cycle is allowed to approach 100%, the current transformer begins to saturate and cause the current error amplifier to believe that less current is being drawn from the line than is being commanded. This causes the current amplifier to overcompensate, causing line current distortion at the zero crossings. In addition, if the current transformer saturates, the current limiting function is lost. For these reasons it is recommended that the output of the current amplifier be clamped externally, to limit the maximum duty cycle. Figure 9 shows a typical clamp circuit.

The clamp circuit in Figure 9A performs quite well (see Table 1), however if better performance is required, or if it is required to operate over a wide line range, the circuit in Figure 9B can be used. This circuit adjusts the clamp voltage to be inversely proportional to line voltage.



A. Current error amplifier clamp circuit.

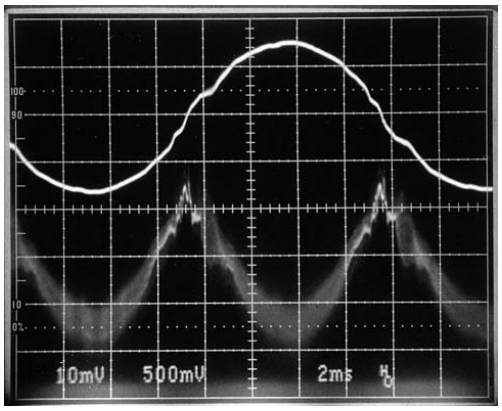


B. Clamp circuit with input voltage compensation.

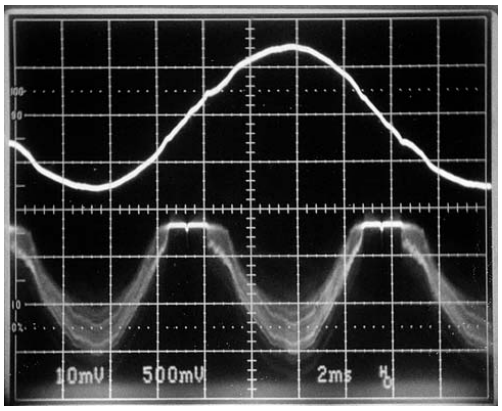
Figure 9. Clamp Circuit

The procedure for setting the clamp voltage is quite easy. If during initial startup the current amplifier clamp is set to a relatively low value (≈ 4 V) the system operates but with excessive zero crossing distortion. Once the system is operating, the clamp voltage can be increased until the current transformer is not saturating, and line current has an acceptable level of THD. Once the clamp voltage is set, operation with other devices are repeatable. In the experimental breadboard built for universal line operation and 500-W output, the single stage clamp was set to 5.6 V (at low line and maximum load) and an acceptable level (< 10%) of THD was measured over all line and load conditions. The clamp voltage is being set below the peak of the PWM comparator ramp (nominally 6.5 V) to limit D_{MAX}. Setting the clamp voltage too low causes excess zero crossing distortion due to the amplifier not being able to command enough line current.

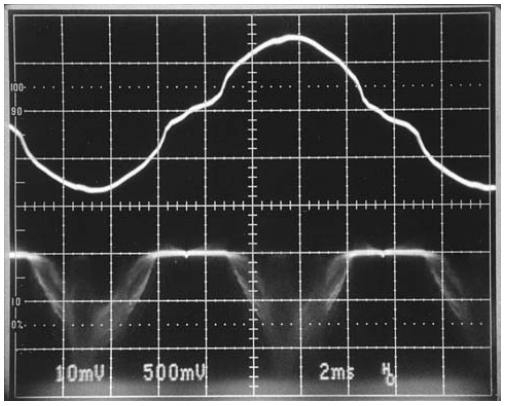
Figures 10A and 10B show the current amplifier operation with and without the clamp, while Figure 10C shows the effect of clamping the amplifier output voltage too low (top waveform is line current, bottom is V_{CAO}). Setting the clamp too high has the same effect as having no clamp.



A. Without clamp.



B. With clamp.



C. Too much clamp.

Figure 10. C/A Clamp Effects on I Line

The procedure for setting the two stage clamp circuit is the same except that the voltage contribution from the line must be factored in. The line voltage only has to contribute 100 mV to 200 mV of clamp voltage for line compensation.

At very light or no load conditions, the average current drawn from the line is lower than can normally be commanded by the current error amplifier. To prevent an overvoltage condition from occurring, the device goes into a pulse skipping mode if the output voltage of the error amplifier goes below ≈ 1 V. Pulse skipping can also occur at high line and low load conditions. When C_{AO} goes below 1 V, the pulse skipping comparator is activated. The output of the comparator goes to an input of an OR gate in the OVP/ENABLE circuit, causing the output of that OR gate to go high. This signal prevents the ZVT and main gate drives from going high.

The procedure for compensating the current error amplifier is covered in the Design Procedure section (IV).

3.5 Voltage Error Amplifier

The output voltage is sensed by the VSENSE input to the voltage error amplifier and compared to an internally generated reference of 3 V. The output of the amplifier, V_{EA}, (at a given input voltage) varies proportionally with output power. The output voltage range for the voltage error amplifier is approximately 0.1 V to 6 V. The output of the amplifier is one of the multiplier inputs, and an input voltage below 1.5 V inhibits the multiplier output. The design procedure for compensating the voltage loop is outlined in the Design Procedure section.

3.6 Protection Circuitry

3.6.1 OVP/ENABLE

The UC3855A/B combines the enable and OVP function into one pin. It requires a minimum of 1.8 V to enable the device, and below this voltage, the reference is held low and the oscillator is disabled. A voltage above 7.5 V interrupts the gate drive. The resistor divider should be sized for 7.5 V when an over voltage condition is reached, this allows startup at a reasonable line voltage. For example, if an overvoltage condition is defined as an output voltage exceeding 450 V, then the voltage divider from V_{OUT} to the OVP pin is 60:1. This divider allows startup at a line voltage of 76 V_{RMS} (108 V_{PK}).

3.6.2 Current Limit

The UC3855A/B has pulse by pulse current limiting. The multiplier power limit determines the maximum average power drawn from the line. However, during transients or overload conditions, a peak current limiting function is necessary. This function is implemented by sensing the switch current and feeding this value into ION, to a current limiting comparator that terminates the gate drive signal if the switch current signal exceeds 1.5 V (nominal).

3.7 Soft Start

In order to ensure a smooth, controlled startup, the UC3855A/B provides a soft-start (SS) function. The SS pin sources 15 μA into an external capacitor. This capacitor limits the supply voltage to the voltage loop error amplifier, which effectively limits the output voltage of the amplifier and therefore the maximum commanded output voltage. This allows the output voltage to ramp up in a controlled fashion.

3.7.1 Undervoltage Lockout

The UC3855A has a 15.5 V (nominal) turn-on threshold with 6 V of hysteresis while the UC3855B turns on at 10.5 V with 0.5 V of hysteresis.

4 Typical Application

A typical application is designed in order to illustrate the design procedure and highlight the design parameters that need to be defined. The design specifications are:

- V_{IN} = 85 − 270 VAC
- VO = 410 VDC
- $P_{O(max)}$ = 500 W
- F_S = 250 kHz
- Eff > 95%
- Pf > 0.993
- THD < 12%

The above specifications represent a common universal input voltage, medium power application. The switching frequency of 250 kHz is now possible due to the soft switching, zero voltage transitions. The Pf and THD numbers correspond to achievable line correction with the UC3855.

4.1 Design Procedure

This design procedure is a summary of what was presented in [8]. However, several values have been changed in order to consolidate component values and/or specify more readily available parts.

4.2 Power Stage Design

4.2.1 Inductor Design

The power stage inductor design in a ZVT converter is identical to the conventional boost converter. The inductance required is determined by the amount of switching ripple desired, and allowing more ripple reduces the inductor value. The worst case for peak current occurs at low line, maximum load. Peak power is equal to twice the average power and V_{PK} is $\sqrt{2}\,V_{RMS}$. To calculate input current, assume an efficiency of 95%.

$$I_{PK} = \frac{2 \times P_{IN}}{\sqrt{2} \times V_{IN(min)}} = \frac{\sqrt{2} \times \left(\frac{500}{0.95}\right)}{85} = 8.7\ A\ (60\ Hz\ component)$$

A good compromise between current ripple and peak current is to allow a 20% ripple to average ratio. This also keeps the peak switch current less than 10 A.

$$\Delta I_L = 0.2 \times (8.7\ A) = 1.7\ A_{pp}$$

Rearranging the conversion ratio for the boost converter to solve for D yields :

$$D = \frac{V_O - V_{IN}}{V_O} = \frac{410 - \sqrt{2} \times 85}{410} = 0.71$$

We can now calculate the required inductance.

$$L = \frac{V_{IN} \times D \times T_S}{\Delta I} = \frac{\sqrt{2} \times 85\ V \times (0.71 \times 4\ \mu s)}{1.7\ A} = 200\ \mu H$$

4.2.2 Output Capacitor Selection

The value of output capacitor effects both hold-up time and output voltage ripple. If hold up time (t_H) is the main criteria, the following equation gives a value for C_O:

$$C_O = \frac{2 \times P_O \times t_H}{V_O{}^2 - V^2_{MIN}}$$

In this example a compromise between holdup time and capacitor size was made and a capacitor value of 440 µF was selected. The capacitor bank consists of two 220 µF, 450 V_{DC} capacitors in parallel.

4.2.3 Power MOSFET & Diode Selection

The main MOSFET selected is an Advanced Power Technology's APT5020BN (or equivalent). This is a 500-V, 23-A device, with $R_{DS(on)}$ = 0.20 Ω (25°C) and C_{OSS} » 500 pF in a TO−247 package. A 5.1-Ω resistor is placed in series with the gate to damp any parasitic oscillations at turn-on with a Schottky diode and 2.7-Ω resistor in parallel with the resistor to speed up turn-off. A Schottky is also placed from GTOUT to ground to prevent the pin from being driven below ground, and should be placed as close to the device as possible.

The boost diode selected is the International Rectifier HFA15TB60, a 15-A, 600-V ultrafast diode (or equivalent). Recall that a converter employing ZVT benefits from soft switching of the diode. With ZVT, the boost diode has a negligible impact on switching losses, and therefore a slower diode could potentially be used. However, there are still valid reasons for using an ultra fast diode in this application.

The ZVT inductor is sized according to the recovery time of the diode, and a slower diode requires a larger inductor. This requires a correspondingly longer Q_{ZVT} on-time, which increases conduction loss. A larger inductor also requires a longer time to discharge. To ensure complete discharge of the resonant inductor, the main switch minimum on-time should be approximately equal to the ZVT circuit on-time. This yields:

$$D_{MIN} = \frac{t_{01} + t_{12} + t_{rr}}{T}$$

D_{MIN} effects the minimum allowable output voltage for the boost converter to continue operating. The ZVT circuit on-time is a strong function of t_{rr}, and therefore choosing an ultra fast diode keeps the resonant circuit losses to a minimum and cause the least impact on the output voltage. The effective system duty cycle is primarily a function of the main switch on-time, since for a large portion of the resonant circuit's on-time, the voltage at the anode of the boost diode is held up by the resonant capacitor.

These considerations suggest a diode with a recovery time less than 75 ns. Average output current in this design is less than 1.2 A with a peak current of 9.2 A. The conduction loss associated with the diode is approximately 2.2 W.

While an ultra fast diode is being used, the diode is operating with significantly reduced switching losses. This increases the overall system efficiency and reduce the peak stress of the diode.

4.3 ZVT Circuit Design

4.3.1 Resonant Inductor

The ZVT circuit design is straightforward. The circuit is performing an active snubber function and, as such, the inductor is designed to provide soft turn off of the diode. The ZVT capacitor is selected to provide soft switching of the MOSFET.

The resonant inductor controls the di/dt of the diode by providing an alternate current path for the boost inductor current. When the ZVT switch turns on, the input current is diverted from the boost diode to the ZVT inductor. The inductor value can be calculated by determining how fast the diode can be turned off. The diode's turn-off time is given by its reverse recovery time. Calculating an exact value for L_r is difficult due to the variation in reverse recovery characteristics within the actual circuit as well as variations in how reverse recovery is specified from manufacturer to manufacturer. An example of circuit conditions effecting the reverse recovery is the natural snubbing action of the resonant capacitor, which limits the dv/dt at the anode of the diode. A good initial estimate is to allow the inductor current to ramp up to the diode current within three times the diode's specified reverse recovery time. One constraint on the maximum inductance value is its affect on the minimum duty cycle. As was shown in the diode selection section, the L−C time constant effects D_{MIN} and therefore $V_{O(min)}$. Making L_r too large also increases the conduction time of the ZVT MOSFET, increasing the resonant circuit conduction losses. As the value of L_r is reduced, the diode experiences more reverse recovery current, and the peak current through the inductor and ZVT MOSFET increases. As the peak current is increased, the amount of energy stored in the inductor also increases ($E = 1/2 \times L \times I^2$). This energy should be kept to a minimum in order to reduce the amount of parasitic ringing in this node at turn-off.

The reverse recovery of the diode is partially a function of its turn-off di/dt. If a controlled di/dt is assumed, the reverse recovery time of this diode can be estimated to be approximately 60 ns. If the inductor limits the rise time to 180 ns ($3 \times t_{rr}$), the inductance can be calculated.

$$\frac{di}{dt} = \frac{I_{INp}}{3 \times t_{rr}} = 53\ A/\mu s$$

$$I_{INp} = I_{pk} + \frac{1}{2}\Delta I$$

$$L_r = \frac{V_O}{\left(\frac{di}{dt}\right)} = \frac{410\ V}{53\ A/\mu s} = 7.7\ \mu H$$

The inductor design is limited by core loss and resultant temperature rise, not saturating flux density. This is due to the high ac current component and the relatively high operating frequency. A good design procedure is outlined in [10] and is beyond the scope of this review. Several points are mentioned however. The core material should be a good high frequency, low loss material such as gapped ferrite or molypermalloy powder (MPP). Powder iron cores generally are not acceptable in this application. The less expensive Magnetics Kool Mu material, although exhibiting higher losses than the MPP material, can also be used. The higher loss material actually tends to damp the resonant ringing at the turn off of the ZVT switch. The inductor winding construction is also optimized by keeping interwinding capacitance to a minimum. This reduces the node capacitance at turn off and reduces the amount of damping required.

The inductor current can by found by analyzing the resonant circuit formed by L_r and C_r and recognizing that the resonant cycle begins when the current reaches Iin.

$$I_{L_r} = I_{IN} + \frac{V_O}{Z_n} \times \sin \omega t$$

where

$$Z_n = \sqrt{\frac{L_r}{C_r}},\ \omega = \sqrt{\frac{1}{L_r \times C_r}}$$

The peak current then is equal to I_{IN} plus the output voltage divided by the resonant circuit's characteristic impedance. Decreasing L_r or increasing C_r increases the peak current. The inductor was designed using a Magnetics, Inc. MPP core 55209 with 33 turns for an inductance of 8 μH. The inductor should be constructed with Litz wire or several strands of small magnet wire to minimize high frequency effects.

4.3.2 Resonant Capacitor

The resonant capacitor is sized to ensure a controlled dv/dt of the main switch. The effective resonant capacitor is the sum of the MOSFET capacitance and the external node capacitance. The APT5020BN has approximately 500 pF of output capacitance, and an external capacitance of 500 pF was added across the device. This capacitor limits the dv/dt at turn-off and consequently reduces the Miller effect. In addition, it reduces turn-off losses since the switch current is diverted to the capacitor. The capacitor must be a good high frequency capacitor, and low ESR and ESL are required. It must also be capable of handling the relatively large charging current at turn-off. Two good choices are polypropolene film or a ceramic material.

This combination of L and C yields a resonant quarter cycle of:

$$\frac{\pi}{2}\sqrt{L_r \times C_r} = 140\ ns$$

The resonant circuit's impact on the output voltage can now be calculated. Recall that to ensure discharge of the resonant inductor at high line:

$$D_{MIN} = \frac{t_{01} + t_{12} + t_{rr}}{T}$$

and for a boost converter:

$$V_{O(\min)} = \frac{V_{IN(pk)}}{1 - D_{MIN}}$$

Substituting (1) into (2) and solving for V_O produces:

$$V_{O(\min)} = \frac{\left(L_r \times I_{IN(p)} + V_{IN(p)} \times T\right.}{\left(T - t_{rr} - \frac{\pi}{2} \times \sqrt{L_r \times C_r}\right)}$$

Equation (3) can be solved using the previously established values and yields a minimum output voltage of 405 V. This suggests a design value of 410 V for V_O.

4.3.3 ZVT Switch and Rectifier Selection

The ZVT switch also experiences minimal turn-on loss due to the discharge of its drain-to-source capacitance. However, it does not experience high current and voltage overlap since the turn-on current is limited by the resonant inductor. The switch does experience turn-off and conduction losses however. Although the peak switch current is actually higher than the main switch current, the duty cycle is small, keeping conduction losses low. The ZVT switch is one or two die sizes smaller than the main switch due to the low average drain current. The ZVT switch on-time is :

$$t_{ZVT} = \frac{I_{IN(p)} \times L_r}{V_O} + \frac{\pi}{2} \times \sqrt{L_r C_r}$$

The peak ZVT switch current is equal to the peak ZVT inductor current. A conservative approximation of the switch RMS current is made by assuming a square wave signal. The RMS of the current is approximated by:

$$I_{RMS} \approx I_{LR(pk)} \times \sqrt{\frac{t_{ZVT}}{T}}$$

This corresponds to a peak of approximately 14 A at maximum load and maximum ZVT on-time, however, the RMS is only 3.9 A. An appropriate device in this application is the Motorola MTP8N50E, a 500-V, 8-A device with an $R_{DS(ON)}$ of 0.8 Ω. As with the main MOSFET, a 5.1-Ω resistor is placed in series with the gate to damp any parasitic oscillations at turn on and a Schottky diode and resistor is placed in parallel with the resistor to speed up turn-off. A Schottky is also placed from ZVTOUT to ground to prevent the pin from being driven below ground. This diode should be placed as close to the device as possible.

The rectifiers needed for the ZVT circuit also experience relatively low RMS current. Diode D2 returns the energy stored in the resonant inductor during t_{ZVT} to the load. D2 should be an ultra-fast recovery diode and is usually chosen to be of similar speed as D1. The diode selected for D2 is a Motorola MURH860; a 600-V device with a $t_{rr} \approx 35$ ns.

Diode D3 blocks current from flowing up through the Q_{ZVT} body diode when the inductor resets, it sees the same peak and RMS current as Q_{ZVT}. D3 should be a fast recovery diode to decouple the drain to source capacitance of Q_{ZVT} from the resonant inductor. Energy stored in the D3 anode node capacitance resonates with the ZVT inductor when the ZVT switch turns off. Minimizing this effect reduces the amount of snubbing required at this node. The diode chosen here was the MUR460. This is a 600-V, 4-A device with $t_{rr} \approx 75$ ns.

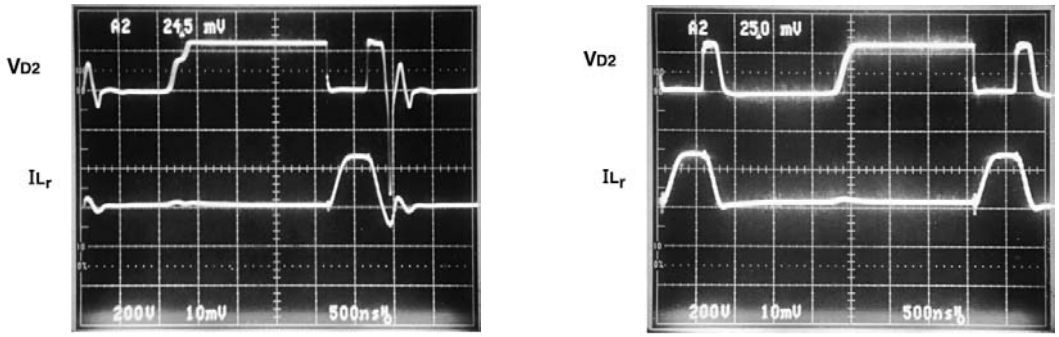
To summarize, both diodes in the ZVT circuit experience low RMS current. The main selection criteria in addition to the blocking voltage (in both cases equal to V_O) is reverse recovery time. Choosing devices with fast recovery times reduces parasitic oscillations, losses, and EMI.

4.3.4 ZVT Snubber Circuit

The ZVT circuit requires some method for damping the parasitic oscillations that occur after the ZVT inductor current goes to zero. Figure 10A shows the ZVT inductor current and diode D2 anode voltage without adequate damping. The figure shows that as the inductor current begins to discharge (when Q_{ZVT} turns off) to the output, the anode voltage is at V_{OUT} (since D2 is conducting). As the inductor current passes through zero, the voltage rings negative since the opposite end of the inductor is clamped to 0 V through the main switch body diode. The anode voltage can easily ring negatively to twice the output voltage. This increases the reverse voltage stress on the diode to three times the output voltage! Keeping the energy in the node capacitance to a minimum and using fast recovery diodes reduces the ringing and improve the circuit performance.

Several methods of damping this oscillation have been proposed [4,7]. In this circuit two methods, the saturable reactor and resistive damping were investigated. A 51-Ω, 10-W noninductive resistor was connected through a diode from ground to the anode of D2. The saturable reactor was placed in series with the resonant inductor and implemented with 8 turns on a Toshiba saturable core SA 14 x 8 x 4.5. The resistive damping method prevents the node from oscillating. However, it does not prevent current from flowing in D2 while D1 is conducting (due to the dv/dt across L_r when Q_{MAIN} turns off). If current flows through D2 during this time it experiences reverse recovery current when Q_{ZVT} turns on. The saturable reactor prevents this current flow due to its high impedance. L_S also decouples L_r from the node capacitance, which prevents the node from oscillating.

The saturable reactor works well without the resistive damping and was the method chosen in this design. With the saturable reactor damping the circuit properly, the resistive damping can be eliminated. However, since L_S is designed to saturate each switching cycle, the core loss is largely material dependent and can cause significant temperature rise of the core. In this circuit, heatsinking of the core was required. An alternative design was also tried using the larger MS 18 x 12 x 4.5 which ran cooler although it also required heatsinking. Optimization of this circuit can significantly reduce the losses in the ZVT circuit. In this design, damping network losses were approximately 2 W. Figure 10B shows the same circuit condition with the node damped with L_S.



A. Waveforms without damping. B. Waveforms with proper damping.

Figure 11. ZVT Ringing Waveforms

4.3.5 ZVS Circuit

The ZVS circuit components are chosen next. In this example, a 1-kΩ resistor is used to pull up the ZVS pin. The capacitor chosen is 500 pF. This combination requires approximately 200 ns to charge up to the 2.5-V threshold.

$$t = R \times C \times I_n\left(\frac{1 - V_{THRESHOLD}}{V_{REF}}\right)$$

4.4 Oscillator Frequency

Calculate CT:

The switching frequency selected is 250 kHz.

$$CT = \frac{1}{11200 \times 250\ kHz} = 357\ pF,\ use\ 330\ pF$$

4.5 Multiplier/Divider Circuit

Calculate the V_{RMS} resistor divider:

Set V_{RMS} = 1.5 V at low line (85 V_{RMS})

$$divider = \frac{85\ V_{RMS} \times 0.9}{1.5\ V_{DC}} = 51 : 1$$

The voltage divider can be solved if one of the resistors is defined (since there are two equations and three unknowns). Letting the lower resistor in the divider = 18 kΩ:

R_{TOTAL} = 18 kΩ x 51 = 918 kΩ

Letting R10 = 120 kΩ, gives:

R9 = 918 kΩ − 120 kΩ − 18 kΩ = 780 kΩ

R9 is split into two resistors (each 390 kΩ) to reduce their voltage stress.

Calculate the capacitor values to place the filter poles at 18 Hz:

$$C5 = \frac{1}{2 \times \pi \times f_P \times R11} = \frac{1}{2 \times \pi \times 18\ Hz \times 18\ k\Omega} = 0.49\ \mu F,\ use\ 0.4$$

$$C4 = \frac{1}{2 \times \pi \times f_P \times R_{EQ}} = \frac{1}{2 \times \pi \times 18\ Hz \times 117\ k\Omega} = 75\ nF,\ use\ 0.08$$

where R_{EQ} = R9||(R10 + R11) = 117 kΩ

In order to consolidate capacitor values C4 could be chosen to be 0.1 µF without degrading the system performance.

Calculate the IAC resistor:

Set I_{IAC} = 500 µA at high line.

$$R = \frac{\sqrt{2} \times 270\ V}{500\ \mu A} = 764\ K\Omega$$

Use 2, 390 kΩ resistors in series to reduce voltage stress.

4.5.1 Calculate R_{IMO}

At low line I_{IAC} = 156 µA and the output of the multiplier should equal 1 V. With low line and maximum load, V_{EA} is at its maximum of 6 V, therefore, using the multiplier output equation:

$$\frac{1V}{R_{IMO}} = \frac{I_{IAC} \times \left(V_{EA} - 1.5\right)}{V_{VRMS}{}^2}$$

$$R_{IMO} = \frac{1.5^2}{156\ \mu A \times (6 - 1.5)} = 3.2\ k\Omega,\ use\ 3.3\ k\Omega$$

A 1000-pF capacitor is placed in parallel with R_{IMO} for noise filtering. Since the voltage across R_{IMO} is the output of the multiplier and is the reference for the current error amplifier, the RC pole frequency should be placed well above the 120-Hz multiplier signal.

4.6 Current Synthesizer

First, chose a turns ratio for the current transformer. The current transformer is designed to produce 1 V at peak input current. This allows sufficient margin before the current limit trip point (1.4 V) is reached. If I_{PK} = 9.5 A a turns ratio of 50 : 1 would be appropriate. This turns ratio keeps the sense network losses less than 150 mW and allow the use of a 1/4-watt resistor. Solving for the sense resistor yields:

$$R_S = \frac{1\ V}{\frac{I_{SW}}{N}} = \frac{1\ V}{\frac{9.5}{50}} \approx 5.1\ \Omega$$

Recall from the previous current synthesizer section that R_{VS} = 22 kΩ. The current synthesizer capacitor can now be calculated:

$$CI = \frac{3 \times L \times N}{R_{VS} \times V_{OUT} \times R_S} = \frac{3 \times 200\ \mu H \times 50}{22\ k\Omega \times 410\ V \times 5.1\ \Omega} = 633\ pF,\ use\ 680\ pF$$

4.7 Control Loop Design

4.7.1 Small Signal Model

The small signal model of the ZVT PFC boost converter is similar to the standard PFC boost converter model. The two converters operate exactly the same throughout most of the switching cycle and only during the switching transitions is there any difference. This allows the design of the control loops to proceed following the standard techniques outlined in [9].

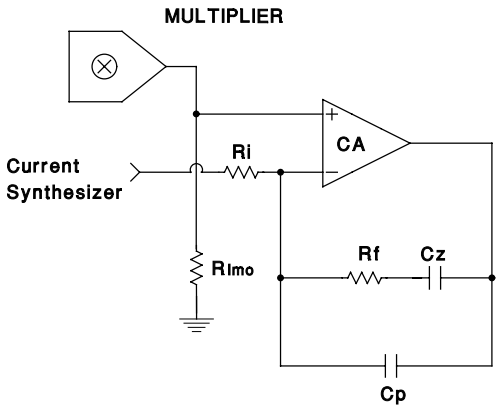
4.7.2 Current Loop Design

Excellent references on the current loop design are found in [5,9,11]. The design of the average current mode control loop begins with choosing a cross-over frequency. In this example the switching frequency is 250 kHz, so the unity gain cross over frequency could be chosen to be as high as 40 kHz (1/6 of the switching frequency). In this circuit however, the cross over is chosen to be 10 kHz. Since the main job of the current loop is to track the line current, a 10 kHz bandwidth is quite adequate for this application.

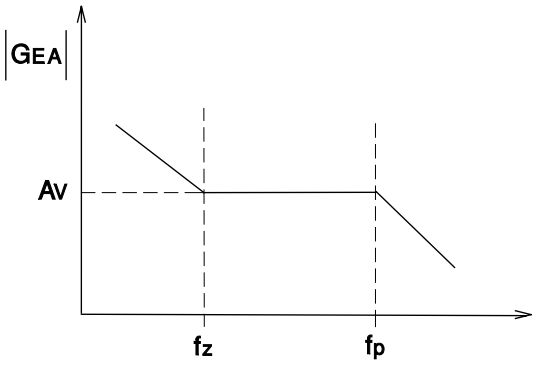
Once the cross over frequency (f_C) is known, the next thing to do is calculate the gain of the power stage. The small signal model of the power stage including the current sense network is given below. This model does not include the sampling effect at one half the switching frequency [12] but is a good approximation at the frequencies of interest.

$$G_{ID(s)} = \frac{V_O \times R_{SENSE}}{S \times L \times V_{SE}}$$

The UC3855A/B has an oscillator ramp of 5.2 V_{PP} (V_{SE}). The R_{SENSE} term, is the attenuation from actual input current to sensed current (i.e. it includes the current transformer turns ratio). Using the previously determined component values and solving for the power stage gain at f_C yields a gain of 0.63 at 10 kHz. In order to have a gain of 1 at f_C, the error amplifier must have a gain of 1/0.63 at 10 kHz. The error amplifier is shown in Figure 12A with the frequency response in Figure 12B. The resistor R_I is equal to 3.3 kΩ so the feedback resistor is chosen to be 5.6 kΩ. A zero is placed at the cross over frequency to give a phase margin of 45 degrees. To reduce switching noise a pole is placed at one-half the switching frequency. The following summarizes the design procedure.



A. Current loop error amplifier.



B. Current error amplifier schematic.

Figure 12. Current Error Amplifier Schematic

1. $|G_{id}(s)| = \dfrac{410\ V \times 0.10}{2 \times \pi \times 10\ kHz \times 200\ \mu H \times 5.2} = 0.63$

2. $G_{EA} = \dfrac{1}{|G_{id}(s)|} = 1.58 \rightarrow A_V = \dfrac{R_f}{R_i}$

$$\therefore R_f = \frac{R_I}{|G_{id}(s)|} \approx 5.6\ k\Omega$$

3. $f_Z = f_C = \dfrac{1}{2 \times \pi \times R_f \times C_Z}$

$$C_Z = \frac{1}{2 \times \pi \times 10\ kHz \times 5.6\ k\Omega} \approx 2200\ pF$$

4. $f_P = \dfrac{1}{2 \times \pi \times R_f\left(\frac{C_Z \times C_P}{C_Z + C_P}\right)} = \dfrac{1}{2 \times \pi \times R_f \times C_P}$

$$C_P = \frac{1}{2 \times \pi \times 5.6\ k\Omega \times 125\ kHz} \approx 220\ pF$$

4.7.3 Voltage Loop Design

The design of the voltage loop follows the procedure given in [5]. The first step is to determine the amount of ripple on the output capacitor.

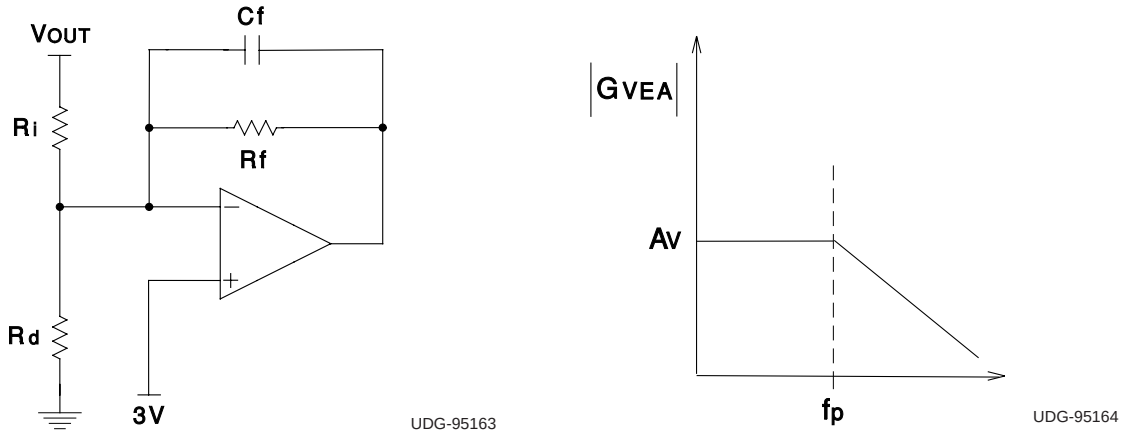
$$V_{O(pk)} = \frac{P_{IN} \times X_{CO}}{V_O}$$

$$V_{O(pk)} = \frac{525}{2 \times \pi \times 120 \times 410\,\mu \times 410} = 4.14\ V_{PK} = 8.3\ V_{PP}$$

In order to meet the 3% THD specification, the distortion due to output ripple voltage feeding through the voltage error amplifier is limited to 0.75%. This allows 1.5% from the multiplier and 0.75% from miscellaneous sources. A 1.5% second harmonic on the error amplifier results in 0.75% 3rd harmonic distortion at the input. At full load, the peak error amplifier ripple voltage allowed is:

$$V_{EA(pk)} = \%RIPPLE \times V_{VEA} = 0.015 \times (6 - 1) = 0.075\ V$$

The error amplifier gain at 120 Hz is the allowable error amplifier ripple voltage divided by the output ripple voltage, or 0.009 (−41 dB). The error amplifier input resistor was chosen to be 1.36 MΩ to keep power dissipation low and allow a small value for the compensation capacitor. Two 681-kΩ resistors in series are used to reduce the voltage stress. The voltage error amplifier schematic is shown in Figure 13, with the 120-Hz gain determined by the integrator function of C_F and R_I. This network has a single pole role off and the capacitor value is easily found to give the desired gain at 120 Hz.



A. Voltage loop error amplifier. B. Voltage amplifier gain plot.

Figure 13. Voltage Error Amplifier

$$C_F = \frac{1}{2 \times \pi \times f \times G_{VEA} \times R_I}$$

$$C_F = \frac{1}{2 \times \pi \times 120\ Hz \times 0.009 \times 1.36\ M\Omega} \approx 0.1\,\mu F$$

The crossover frequency can now be calculated recognizing that a pole (due to the combination of C_f and R_f) is placed at the cross over frequency to provide adequate phase margin. The pole placement determines the phase margin since the power stage has a single pole response with the associated 90 degree phase lag. If the error amplifier pole is placed at the crossover frequency, the overall loop gain has a 45 degree phase margin. The power stage gain is given by:

$$G_{PS}(s) = \frac{V_O}{V_{VEA}} = \frac{P_{IN}}{\Delta V_{VEA} \times V_O \times (S \times C_O)}$$

The voltage loop gain (T_V) is the product of the power stage gain and the error amplifier gain. To find the cross over frequency, solve for f and set equal to 1.

$$T_V = 1 = G_{PS(s)} \times G_{VEA(s)}$$

The error amplifier gain is:

$$G_{VEA} = \frac{-j}{2 \times \pi \times f \times R_j \times C_f} = \frac{-j \times 1.17}{f}$$

$$\therefore T_V = 1 = \frac{-j \times 92.6}{f} \times \left(\frac{-j \times 1.17}{f}\right) = \frac{108}{f^2}$$

The cross over frequency then is approximately 11 Hz, so the resistor, R_f, can be calculated to place the pole at f.

$$R_f = \frac{1}{2 \times \pi \times 11\,Hz \times 0.1\,\mu F} \approx 140\,k\Omega$$

Finally, the resistor R_D (10 kΩ) sets the dc output voltage to 410 V.

4.8 OVP/ENABLE

An output voltage exceeding 450 V is defined as an overvoltage condition. To trip the OVP comparator at 450 V requires a divider of:

$$\frac{7.5\,V}{450\,V} = 60:1$$

Setting the lower resistor in the divider = 33 kΩ, the top resistor then is 2 MΩ, two 1-MΩ resistors are used in series to reduce the voltage stress. A 10-nF capacitor is placed in parallel with the 33-kΩ resistor for noise filtering.

With this divider the converter starts at 76 V_{RMS}, which allows startup well below low line.

5 Experimental Results

The example converter was constructed to demonstrate circuit performance. The circuit performed well and was tested over the full line and load ranges.

Figure 14 shows efficiency data for the ZVT vs. a conventional boost converter, which was derived by simply removing the ZVT components. The conventional circuit needed to be cooled with a fan in order to stabilize the power semiconductor temperatures. It can be seen from the data that the ZVT circuit has a significant advantage over the conventional converter at low line. At higher line voltages the advantage is reduced until the two power stages converge at high line. This is understandable and consistent with the other reported data [4,13]. At low line, the higher input current contributes to higher switching losses in the conventional converter. The ZVT converter however, does not experience increased switching losses (conduction losses increase for both converters at low line).

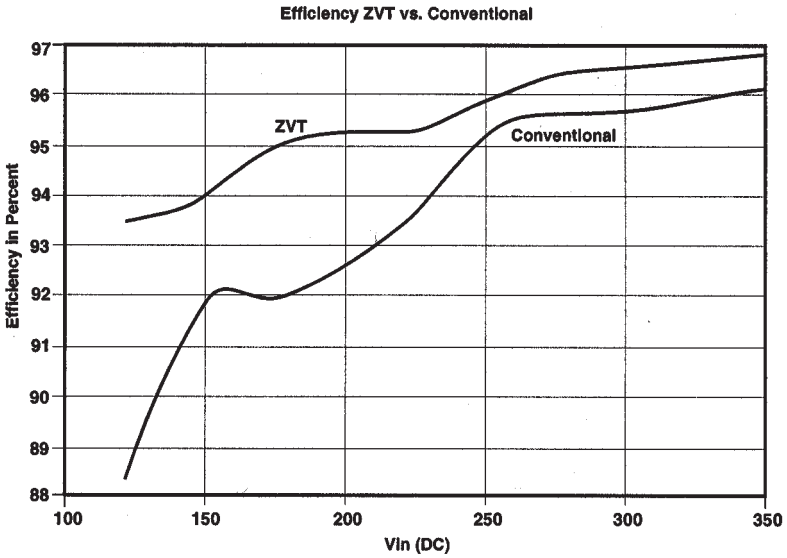


Figure 14. Efficiency Data

Figure 15 shows the ZVT and main switch gate drives as well as the main switch drain to source voltage. The ZVT gate drive goes high prior to the main switch and drives the drain voltage to zero before the main switch turns on. It should also be noted that the drain to source voltage waveform is very clean with no overshoot or ringing, which reduces EMI and voltage stress on the device. The ZVT circuit waveforms are shown in Figure 16. Current in L_r is shown in the top trace. The waveforms are well damped with a peak current of approximately 6 A. The current synthesizer waveforms are shown in Figure 17. The top waveform is the reconstructed waveform at CI and the bottom waveform is inductor current. The waveforms show good agreement. Any error between the reconstructed and actual waveform are greatest at high line and is primarily caused by slight offset voltage errors in the synthesizer circuit.

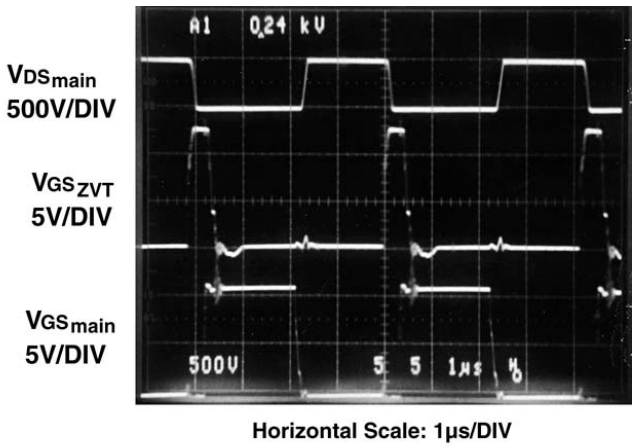


Figure 15. ZVT Waveforms

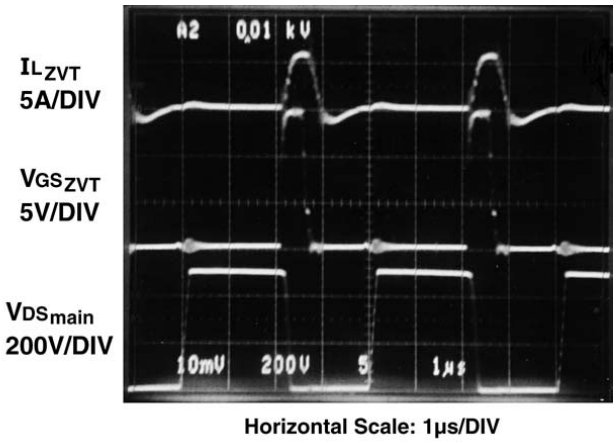


Figure 16. Power Stage Waveforms

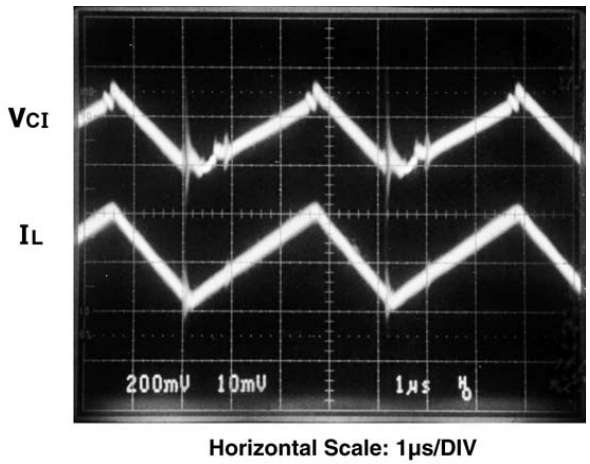


Figure 17. Current Synthesizer Waveforms

Figure 18 shows the input line current at low line and maximum load, the THD and power factor are well within acceptable limits. Table 1 gives THD and power factor (pf) measurements for several line and load conditions with the single stage current error amplifier clamp circuit. Table 2 shows THD and pf with the two stage clamp circuit shown in Figure 9B.

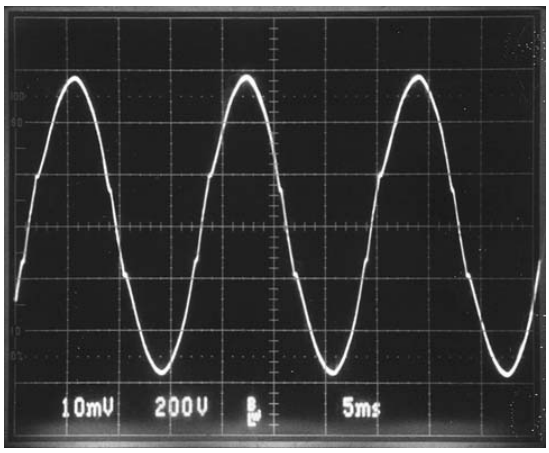


Figure 18. Line Current

Table 1. THD and P_F vs. Line with Single Stage Error Amplifier Clamp Circuit

LINE (VAC)	% THD	Pf
100	6.3	0.998
120	4.5	0.999
200	8.9	0.996
230	10	0.995

Table 2. THD and P_F vs. Line with Two Stage Error Amplifier Clamp Circuit

LINE (VAC)	% THD	Pf
100	4.95	0.999
120	5.30	0.998
200	5.45	0.998
230	5.83	0.998

Table 3. Power Stage Vendors

L1,L2	Magnetics, Butler, PA (412) 282−8282
Spike Killer	Toshiba, Westboro, MA (508) 836−3939
Qmain	APT, Bend, OR (503) 382−8028
D1	International Rectifier, El Segundo, CA (310) 322−3331
QZVT, D2, D3, D4	Motorola, Phoenix, AZ (602) 244−3550

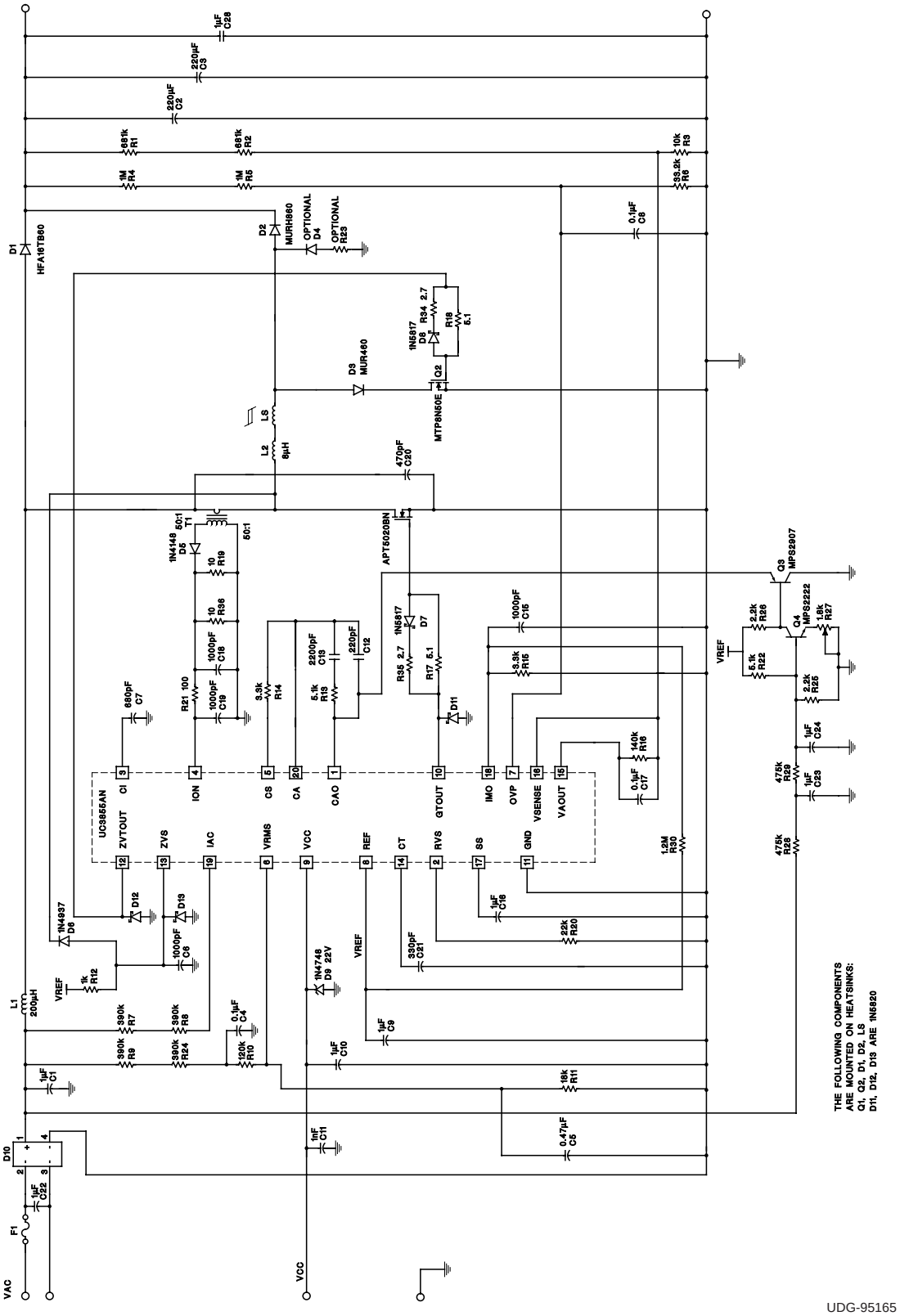


Figure 19. UC3855A/B Typical Application

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