

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

This product is n-Channel MOS Field Effect Transistor designed high current switching application.

FEATURE

- Low On-Resistance
 $R_{DS(on)1} = 14 \text{ m}\Omega$ Typ. ($V_{GS} = 10 \text{ V}$, $I_D = 18 \text{ A}$)
 $R_{DS(on)2} = 22 \text{ m}\Omega$ Typ. ($V_{GS} = 4 \text{ V}$, $I_D = 18 \text{ A}$)
- Low C_{iss} $C_{iss} = 1250 \text{ pF}$ Typ.
- Built-in G-S Protection Diode

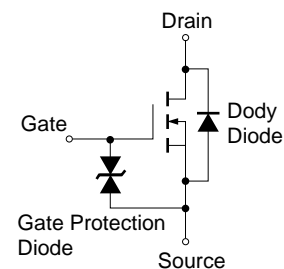
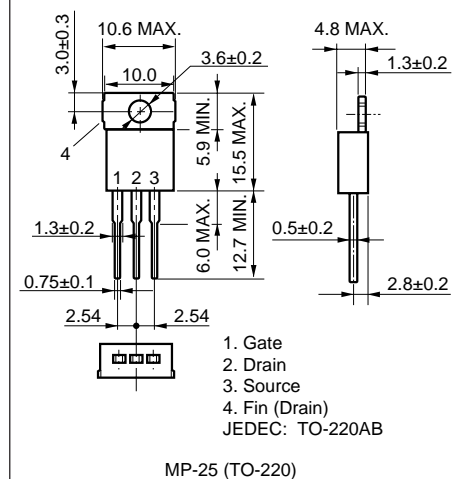
ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Maximum Voltages and Currents

Drain to Source Voltage	V_{DSS}	30	V
Gate to Source Voltage	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 35	A
Drain Current (Pulse)*	$I_{D(Pulse)}$	± 140	A
Maximum Power Dissipation			
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_T	1.5	W
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_T	60	W
Maximum Temperature			
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \text{ to } +125$	$^\circ\text{C}$

* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

PACKAGE DIMENSIONS in millimeters



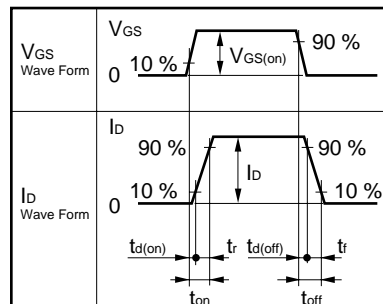
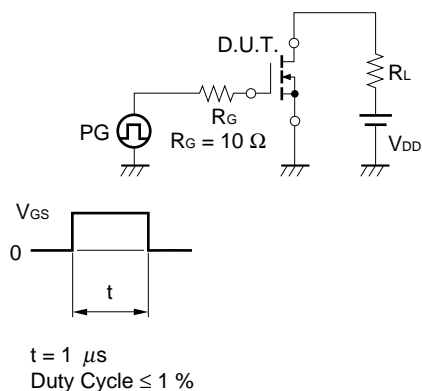
The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device acutally used, an additional protection circuit is externally required if voltage exeeding the rated voltage may be applied to this device.

The information in this document is subject to change without notice.

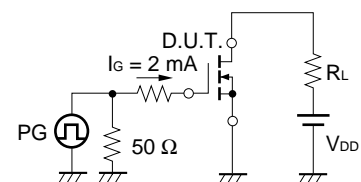
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Drain to Source On-State Resistance	R _{DS(on)1}		14	20	mΩ	V _{GS} = 10 V, I _D = 18 A
	R _{DS(on)2}		22	33	mΩ	V _{GS} = 4 V, I _D = 18 A
Gate to Source Cutoff Voltage	V _{GS(off)}	1.0	1.5	2.0	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	8.0	25		S	V _{DS} = 10 V, I _D = 18 A
Drain Leakage Current	I _{DSS}			10	μA	V _{DS} = 30 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0
Input Capacitance	C _{iss}		1250		pF	V _{DS} = 10 V, V _{GS} = 0, f = 1 MHz
Output Capacitance	C _{oss}		900		pF	
Reverse Transfer Capacitance	C _{rss}		460		pF	
Turn-on Delay Time	t _{d(on)}		40		ns	I _D = 18 A, V _{GS(on)} = 10 V V _{DD} = 15 V, R _G = 10 Ω
Rise Time	t _r		430		ns	
Turn-off Delay Time	t _{d(off)}		160		ns	
Fall Time	t _f		220		ns	
Total Gate Charge	Q _G		50		nC	I _D = 35 A, V _{DD} = 24 V, V _{GS} = 10 V
Gate to Source Charge	Q _{GS}		4.5		nC	
Gate to Drain Charge	Q _{GD}		21		nC	
Body Diode Forward Voltage	V _{F(S-D)}		1.0		V	I _F = 35 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		65		ns	I _F = 35 A, V _{GS} = 0, di/dt = 100 A/μs
Reverse Recovery Charge	Q _{rr}		90		nC	

Test Circuit 1 Switching Time

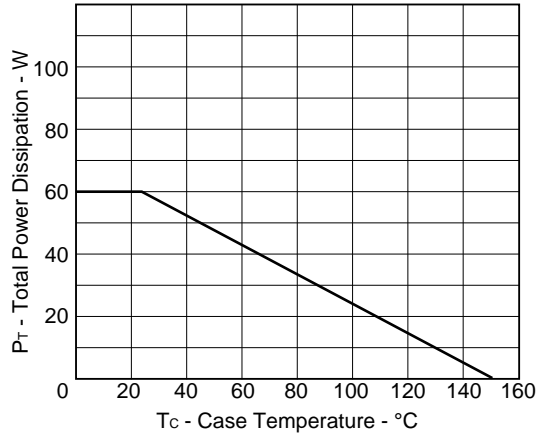


Test Circuit 2 Gate Charge

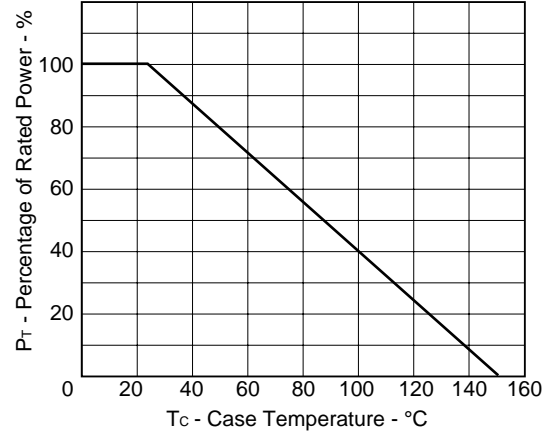


ELECTRICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$)

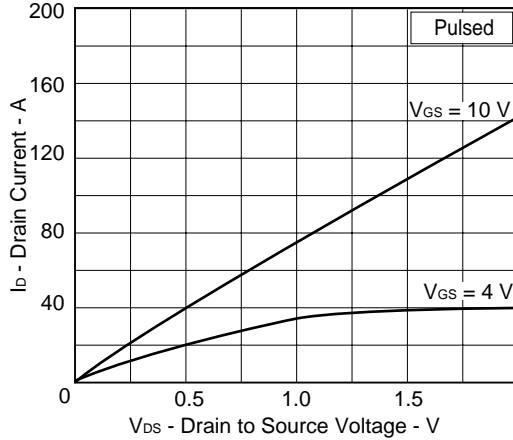
TOTAL POWER DISSIPATION vs.
CASE TEMPERATURE



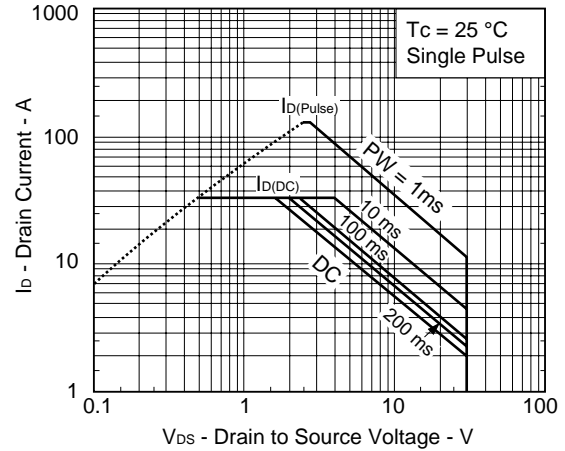
DERATING FACTOR OF FORWARD BIAS
SAFE OPERATING AREA



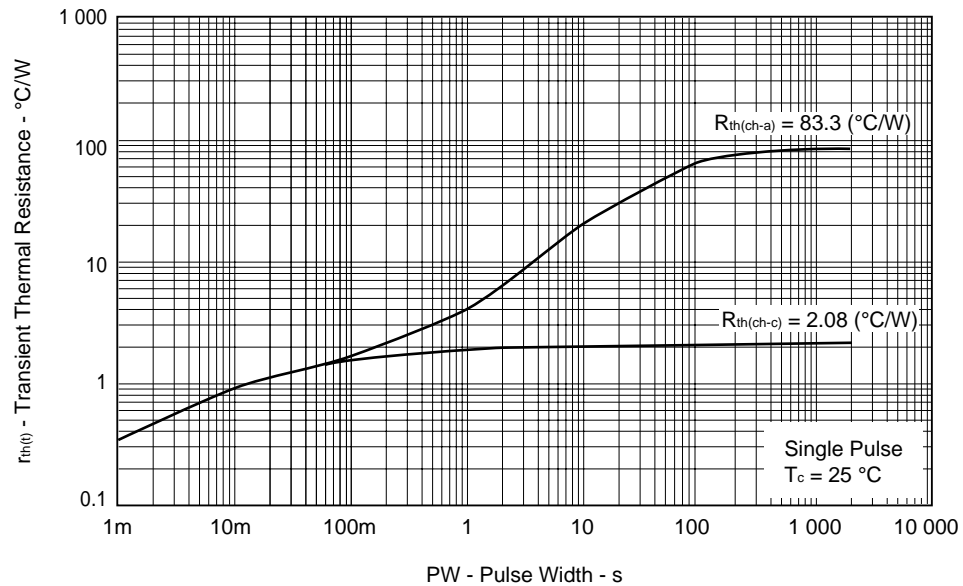
DRAIN CURRENT vs. DRAIN TO
SOURCE VOLTAGE

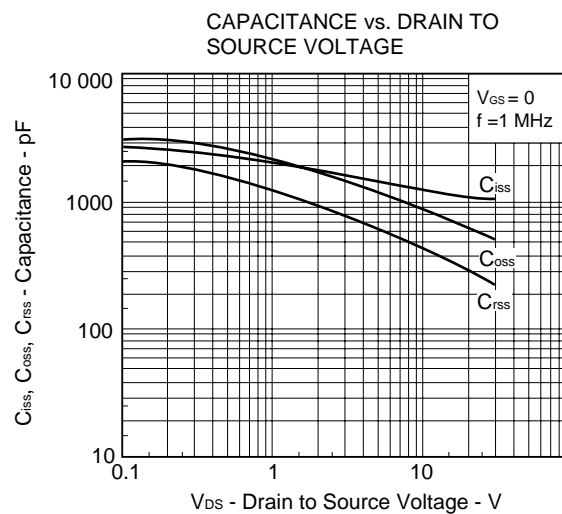
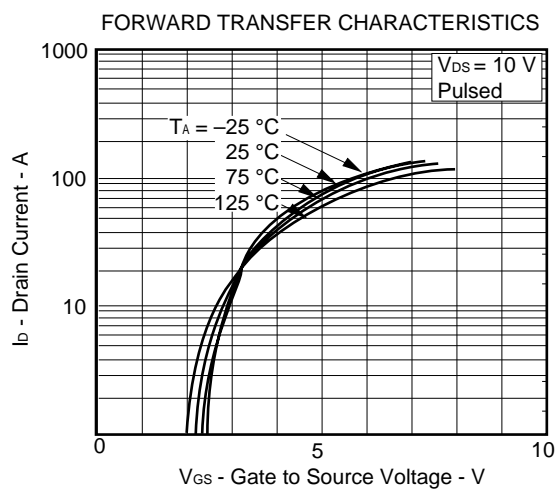
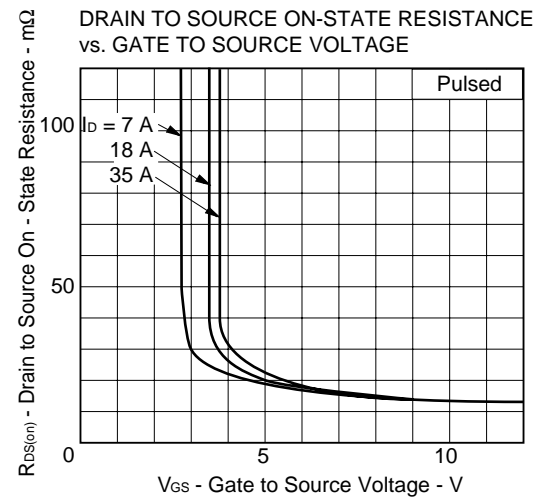
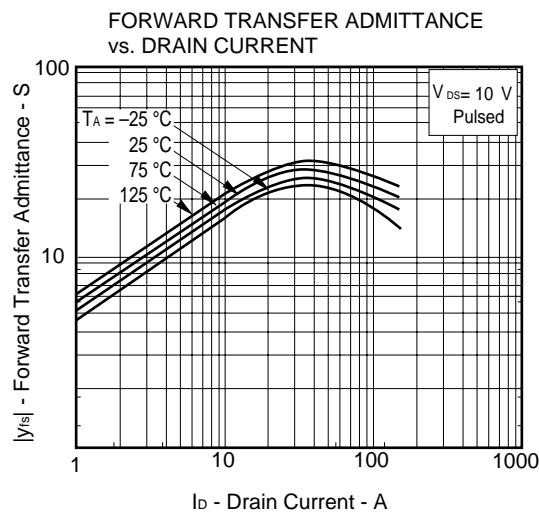
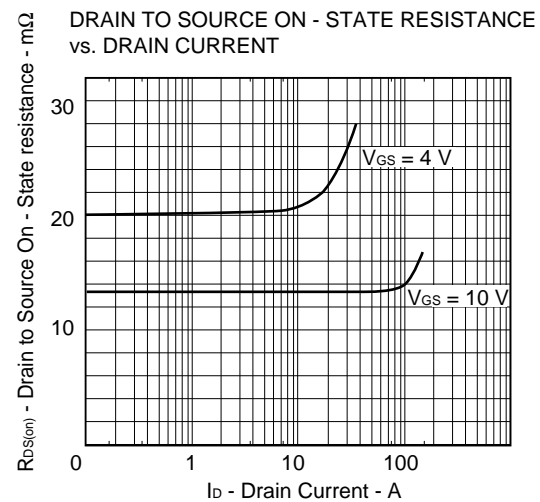
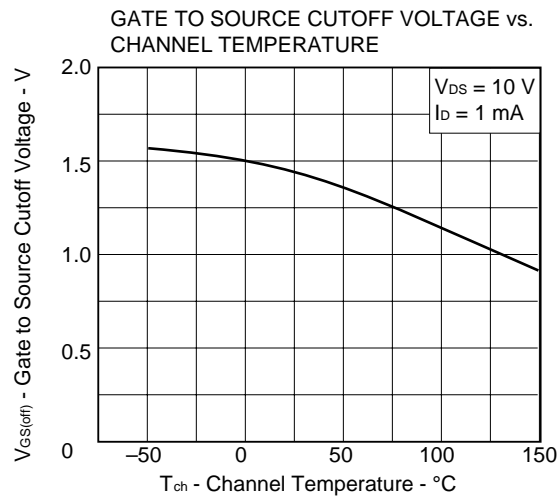


FORWARD BIAS SAFE OPERATING AREA

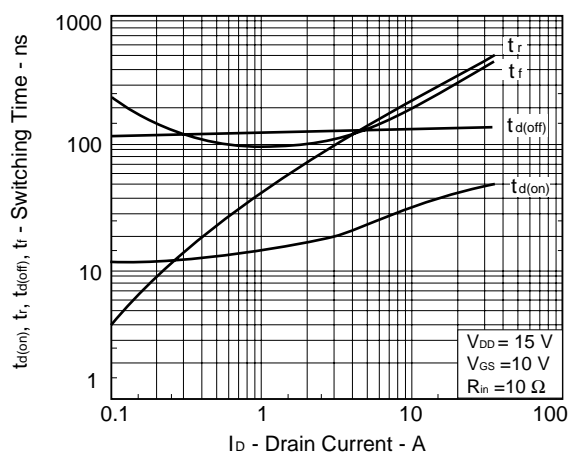


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

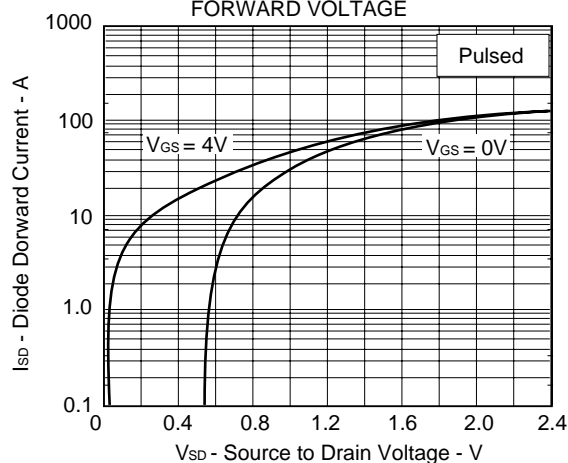




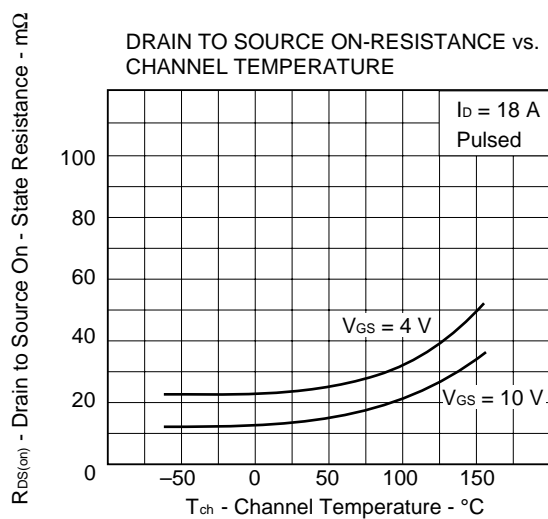
SWITCHING CHARACTERISTICS



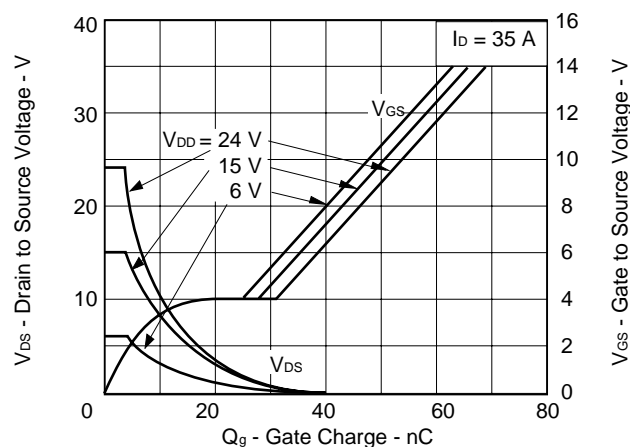
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



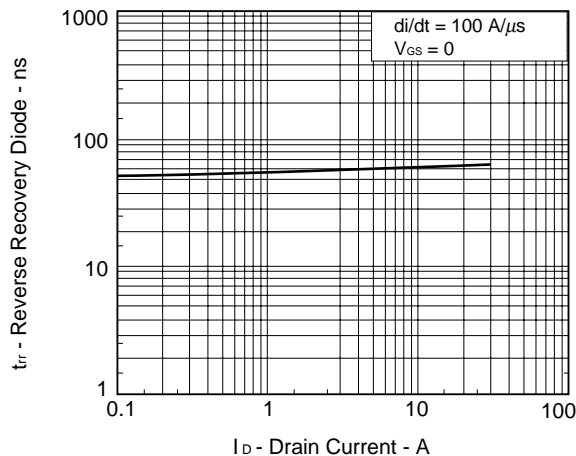
DRAIN TO SOURCE ON-RESISTANCE vs. CHANNEL TEMPERATURE



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REVERSE RECOVERY TIME vs. DRAIN CURRENT



ELECTRICAL REFERENCE (T_A = 25 °C)

Document Name	Document No.
NEC semiconductor device reliability/quality control system	C11745E
Quality grade on NEC semiconductor devices	C11531E
Semiconductor device mounting technology manual	C10535E
Semiconductor device package manual	C10943X
Guide to quality assurance for semiconductor devices	MEI-1202
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

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Anti-radioactive design is not implemented in this product.

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