

TSM7401

20V N-Channel MOSFET w/ESD Protected

SOP-8

Pin Definition:

1. Source
2. Source
3. Source
4. Gate
- 5, 6, 7, 8. Drain

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (m Ω)	I_D (A)
20	25 @ $V_{GS} = 4.5V$	4.5
	30 @ $V_{GS} = 2.5V$	3.5
	65 @ $V_{GS} = 1.8V$	2.0

Features

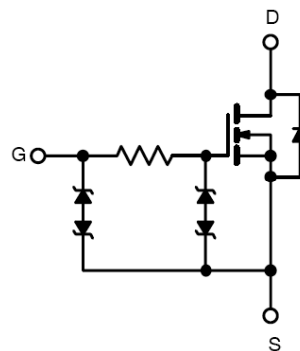
- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance
- ESD Protect 2KV

Application

- Specially Designed for Li-on Battery Packs
- Battery Switch Application

Ordering Information

Part No.	Package	Packing
TSM7401CS RL	SOP-8	2.5Kpcs / 13" Reel

Block Diagram


N-Channel MOSFET

Absolute Maximum Rating ($T_a = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current	I_D	8	A
Pulsed Drain Current	I_{DM}	30	A
Continuous Source Current (Diode Conduction) ^{a,b}	I_S	1.4	A
Maximum Power Dissipation	P_D	$T_a = 25^\circ C$	W
		$T_a = 75^\circ C$	
Operating Junction Temperature	T_J	+150	$^\circ C$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Case Thermal Resistance	$R\theta_{JF}$	30	$^\circ C/W$
Junction to Ambient Thermal Resistance (PCB mounted)	$R\theta_{JA}$	50	$^\circ C/W$

Notes:

a. Pulse width limited by the Maximum junction temperature

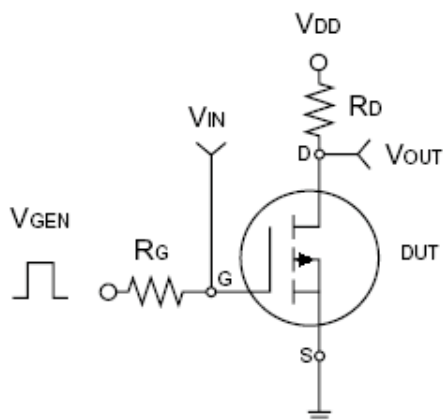
b. Surface Mounted on FR4 Board, $t \leq 5$ sec.

Electrical Specifications (Ta = 25°C unless otherwise noted)

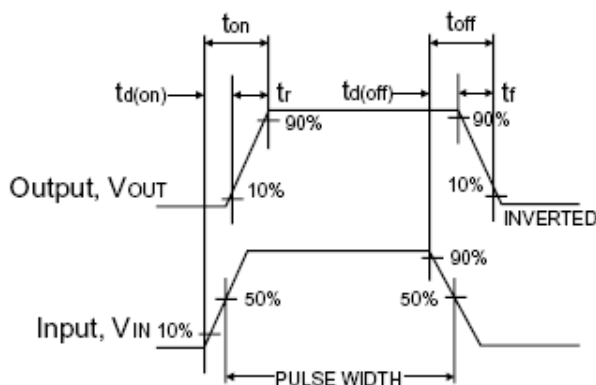
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	20	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	0.6	0.8	1.0	V
Gate Body Leakage	$V_{GS} = \pm 12V, V_{DS} = 0V$	I_{GSS}	--	--	± 10	μA
Zero Gate Voltage Drain Current	$V_{DS} = 16V, V_{GS} = 0V$	I_{DSS}	--	--	1.0	μA
On-State Drain Current	$V_{DS} = 5V, V_{GS} = 4.5V$	$I_{D(ON)}$	30	--	--	A
Drain-Source On-State Resistance	$V_{GS} = 4.5V, I_D = 4.5A$	$R_{DS(ON)}$	--	17	25	m Ω
	$V_{GS} = 2.5V, I_D = 3.5A$		--	21	30	
	$V_{GS} = 1.8V, I_D = 2.0A$		--	34	65	
Forward Transconductance	$V_{DS} = 10V, I_D = 4.5A$	g_{fs}	--	30	--	S
Diode Forward Voltage	$I_S = 2A, V_{GS} = 0V$	V_{SD}	--	0.6	1.2	V
Dynamic ^b						
Total Gate Charge	$V_{DS} = 10V, I_D = 4.5A,$ $V_{GS} = 4.5V$	Q_g	--	15	20	nC
Gate-Source Charge		Q_{gs}	--	3.4	--	
Gate-Drain Charge		Q_{gd}	--	1.2	--	
Input Capacitance	$V_{DS} = 10V, V_{GS} = 0V,$ $f = 1.0MHz$	C_{iss}	--	950	--	pF
Output Capacitance		C_{oss}	--	450	--	
Reverse Transfer Capacitance		C_{rss}	--	135	--	
Switching ^c						
Turn-On Delay Time	$V_{DD} = 10V, R_L = 10\Omega,$ $I_D = 1A, V_{GEN} = 4.5V,$ $R_G = 6\Omega$	$t_{d(on)}$	--	140	200	nS
Turn-On Rise Time		t_r	--	210	250	
Turn-Off Delay Time		$t_{d(off)}$	--	3700	4800	
Turn-Off Fall Time		t_f	--	2000	2600	

Notes:

- pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$
- For DESIGN AID ONLY, not subject to production testing.
- Switching time is essentially independent of operating temperature.



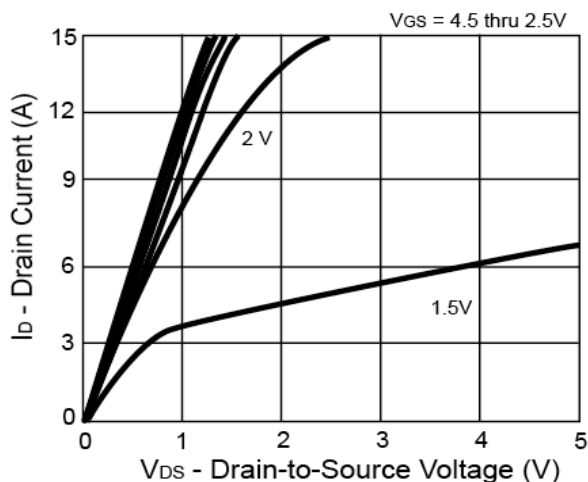
Switching Test Circuit



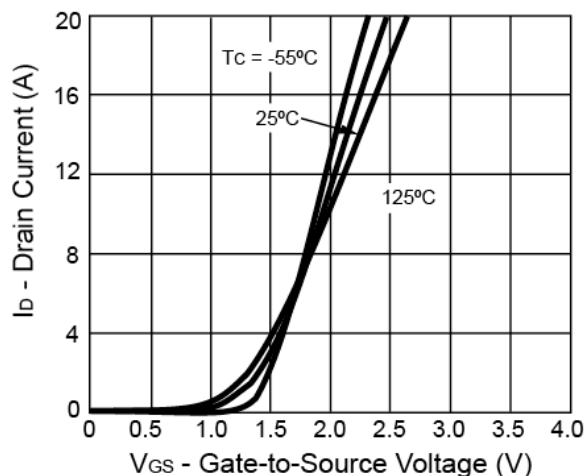
Switchin Waveforms

Electrical Characteristics Curve ($T_a = 25^\circ\text{C}$, unless otherwise noted)

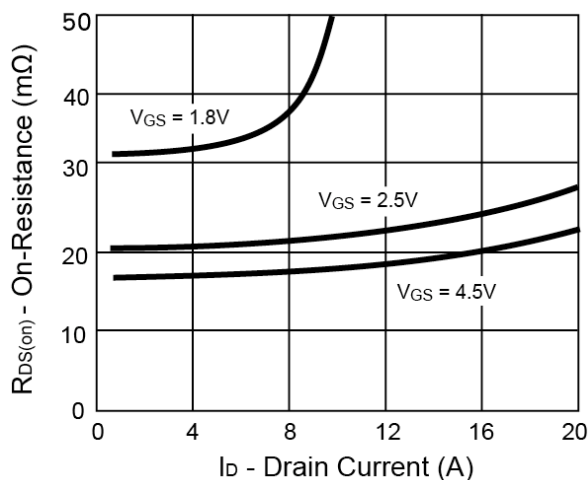
Output Characteristics



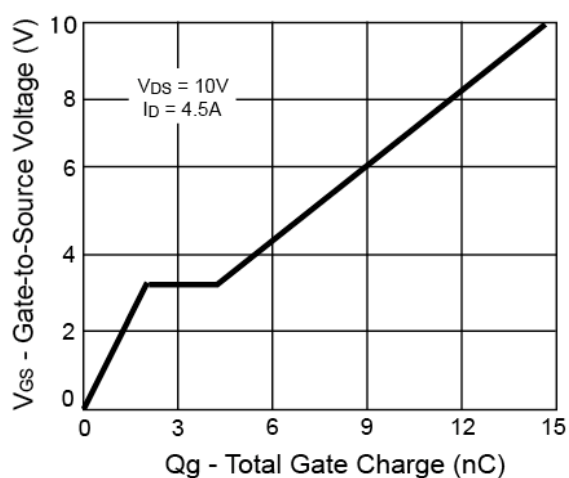
Transfer Characteristics



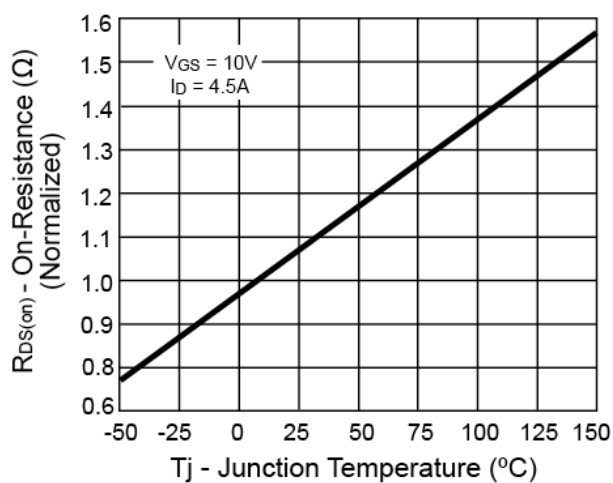
On-Resistance vs. Drain Current



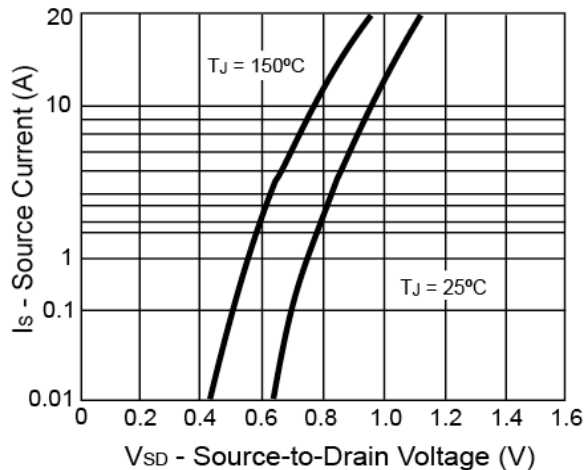
Gate Charge



On-Resistance vs. Junction Temperature

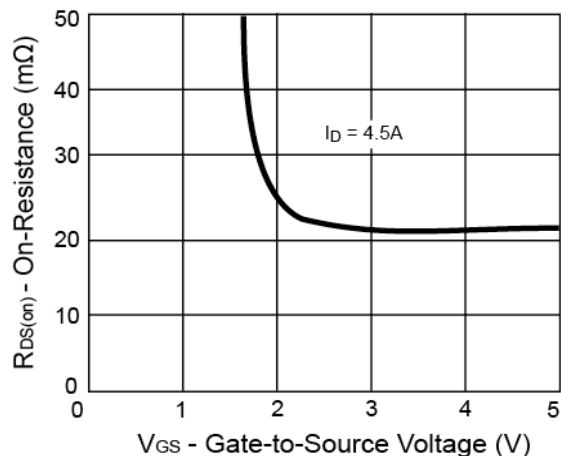


Source-Drain Diode Forward Voltage

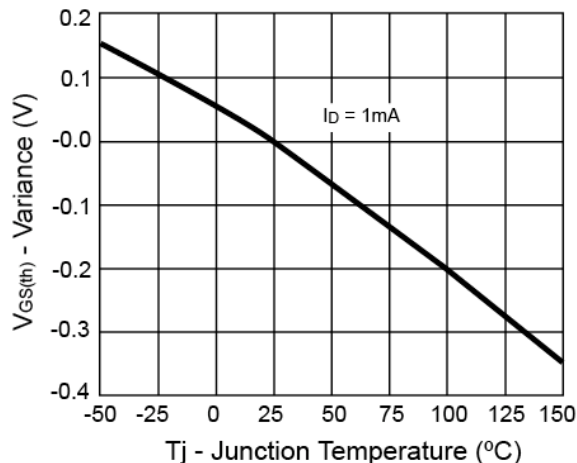


Electrical Characteristics Curve ($T_a = 25^\circ\text{C}$, unless otherwise noted)

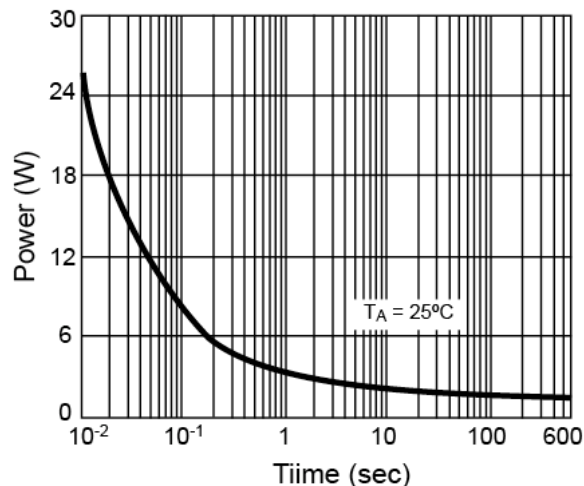
On-Resistance vs. Gate-Source Voltage



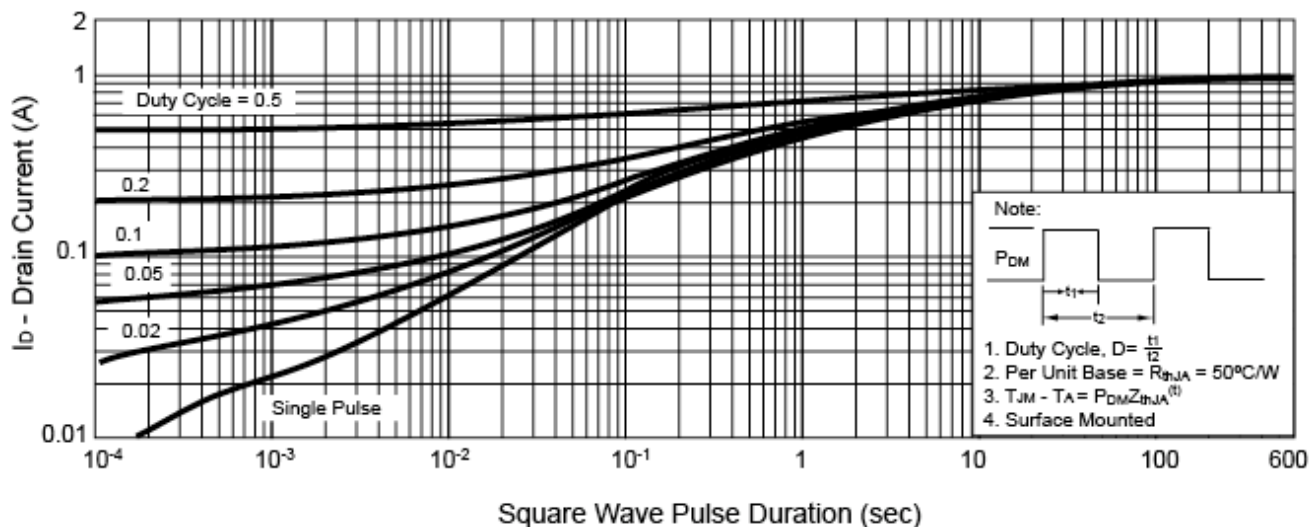
Threshold Voltage



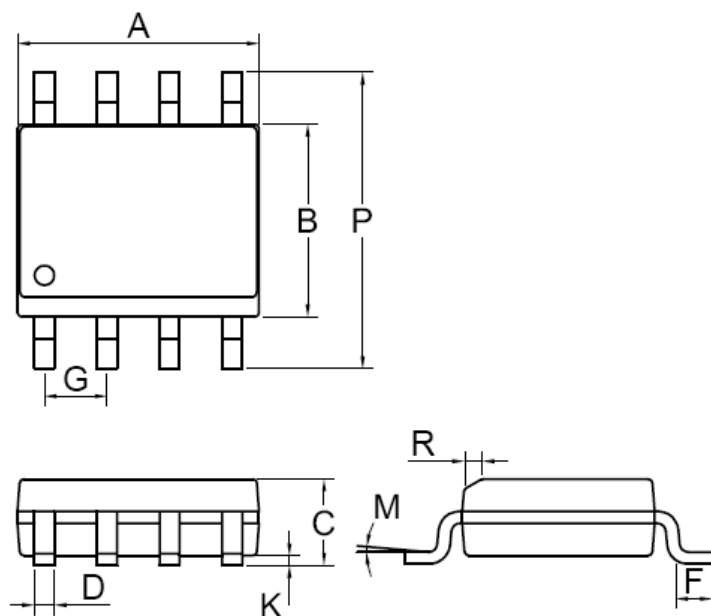
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

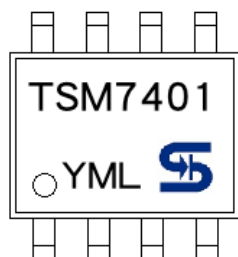


SOP-8 Mechanical Drawing



SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27BSC		0.05BSC	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Marking Diagram



- Y** = Year Code
- M** = Month Code
(A=Jan, B=Feb, C=Mar, D=Apl, E=May, F=Jun, G=Jul, H=Aug, I=Sep, J=Oct, K=Nov, L=Dec)
- L** = Lot Code

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