Mosway Technologies Ltd.

PN7101

High and Low Side Driver

General Description

The PN7101 is a high voltage, high speed power MOSFET and IGBT driver based on P_SUB P_EPI process. The floating channel driver can be used to drive two N-channel power MOSFET or IGBT independently which operates up to 600 V. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross -conduction. Propagation delays are matched to simplify use in high frequency applications.

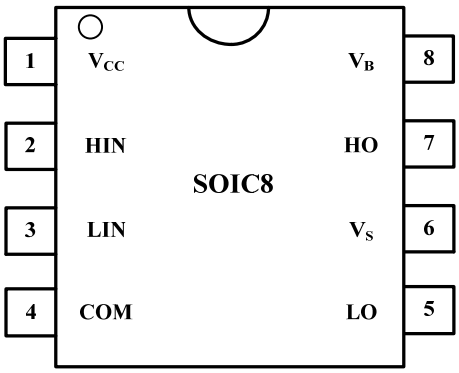
Features

- Fully operational to +600 V
- 3.3 V logic compatible
- dV/dt Immunity ±50 V/nsec
- Floating channel designed for bootstrap operation
- Gate drive supply range from 10 V to 20 V
- UVLO for low side channel
- Output Source / Sink Current Capability 300 mA / 600mA
- Independent Logic Inputs to Accommodate All Topologies
- -5V negative Vs ability
- Matched propagation delay for both channels

Applications

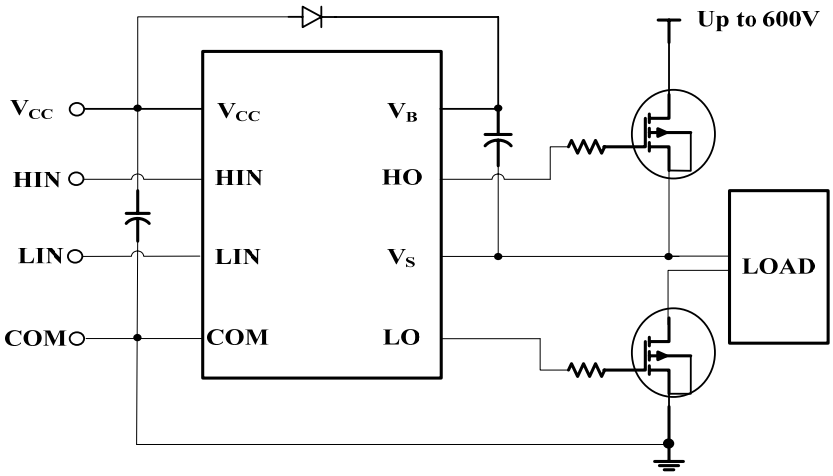
- Small and medium- power motor driver
- Power MOSFET or IGBT driver

Packages/Order information



Part number	Order Code	Package
PN7101	**PN7101SEC-R1**	**SOIC8**

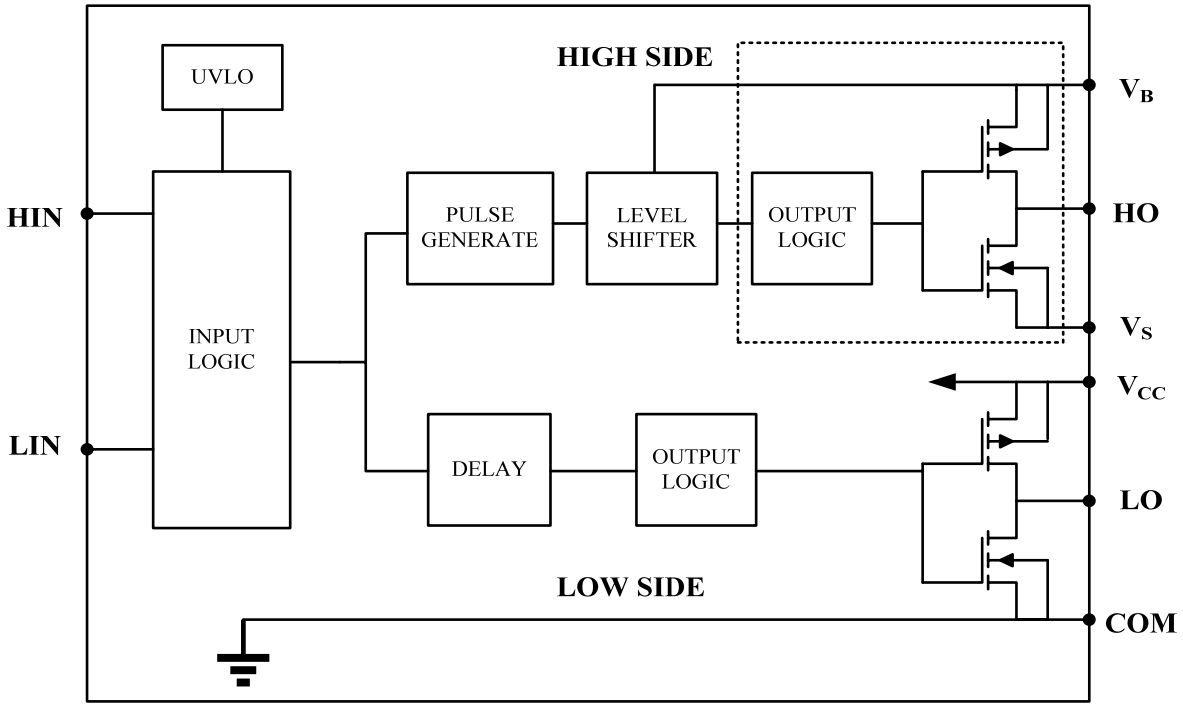
Typical Application Circuit



Pin Description

PIN NO.	PIN NAME	PIN FUNCTION
1	V_{CC}	Low side and main power supply
2	HIN	Logic input for high side gate driver output (HO)
3	LIN	Logic input for low side gate driver output (LO)
4	COM	Ground
5	LO	Low side gate drive output, in phase with LIN
6	V_S	High side floating supply return or bootstrap return
7	HO	High side gate drive output, in phase with HIN
8	V_B	High side floating supply

Functional Block Diagram



Absolute Maximum Ratings [Note1]

Symbol	Definition		MIN.	MAX.	Units
V_B	High side floating supply		-0.3	622	V
V_S	High side floating supply return		V_B - 25	V_B + 0.3	
V_{HO}	High side gate drive output		V_S -0.3	V_B + 0.3	
V_{CC}	Low side and main power supply		-0.3	22	
V_{LO}	Low side gate drive output		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input of HIN & LIN		-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient		--	50	V/ns
ESD	HBM Model		2.5		kV
	Machine Model		200		V
P_D	Package Power Dissipation @ TA ≤25°C	8 Lead SOIC	--	0.625	W
Rth_{JA}	Thermal Resistance Junction to Ambient	8 Lead SOIC	--	200	°C /W
T_J	Junction Temperature		--	150	°C
T_S	Storage Temperature		-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)		--	300	

Note 1: Exceeding these ratings may damage the device.

Recommended Operating Conditions

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	V_S +10	V_S +20	V
V_S	High side floating supply return	-	600	
V_{HO}	High side gate drive output voltage	V_S	V_B	
V_{CC}	Low side supply	10	20	
V_{LO}	Low side gate drive output voltage	0	V_{CC}	
V_{IN}	Logic input voltage(HIN & LIN)	0	V_{CC}	
T_A	Ambient temperature	-40	125	℃

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

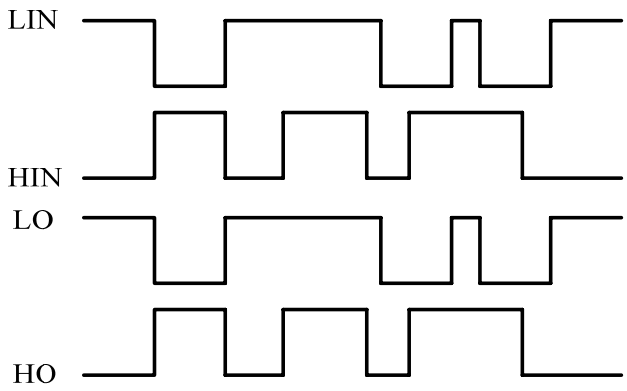
Symbol	Definition	TYP.	MAX.	Units
t_{onH}	High side turn-on propagation delay	160	220	ns
t_{offH}	High side turn-off propagation delay	150	220	
t_{onL}	Low side turn-on propagation delay	160	220	
t_{offL}	Low side turn-off propagation delay	150	220	
MT	Delay matching	20	50	
t_r	Turn-on rise time	60	90	
t_f	Turn-off fall time	40	80	

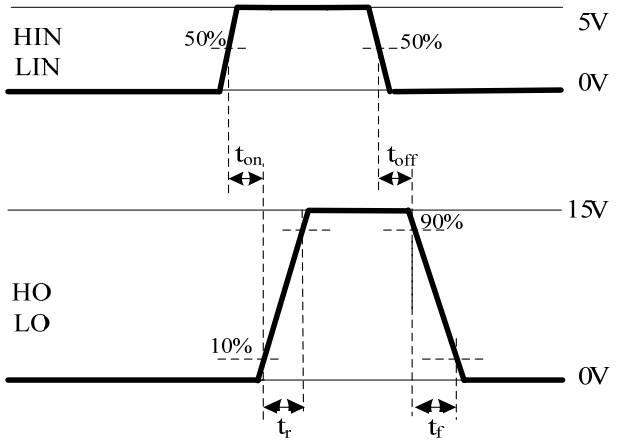
Static Electrical Characteristics

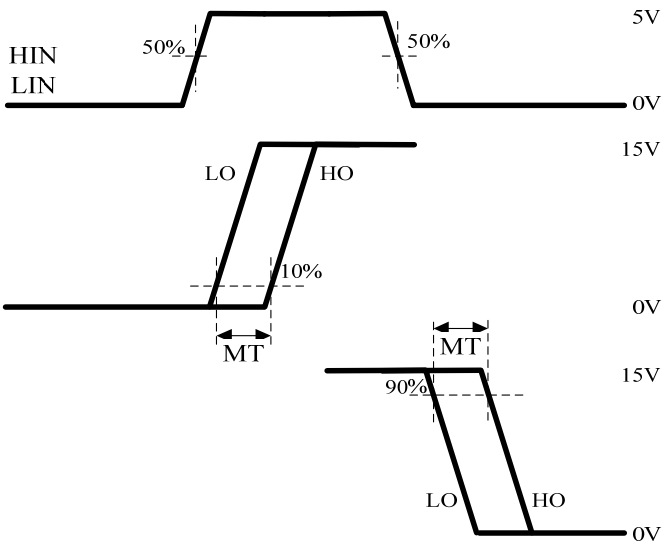
V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units
V_{IH}	Logic "1"(HIN & LIN) input voltage	2.5	-	-	V
V_{IL}	Logic "0" (HIN & LIN) input voltage	-	-	0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	-	-	0.3	
V_{OL}	Low level output voltage, V_O	-	-	0.3	
I_{QCC}	Quiescent V_{CC} supply current	-	170	270	uA
I_{QBS}	Quiescent V_B supply current	-	50	80	
I_{LK}	Leakage current from V_S(600V) to GND		-	10	
I_{IN+}	Logic "1" input bias current	-	6	10	
I_{IN-}	Logic "0" input bias current	-	-	1	
V_{CCU+}	V_{CC} supply UVLO threshold	-	8.7	-	
V_{CCU-}		-	8	-	
I_{O+}	Output high short circuit pulsed current		300		mA
I_{O-}	Output low short circuit pulsed current		600		

Logic Function & Timing Spec





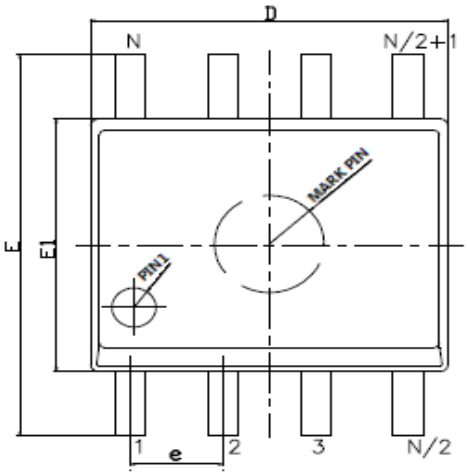


Package Information

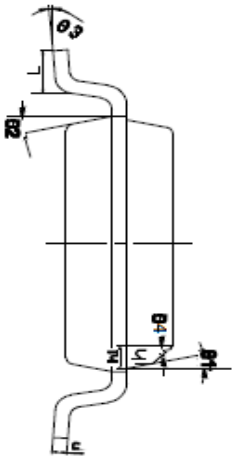
SOIC8 Package Dimensions

Size / Symbol	MIN(mm)	MAX(mm)	Size / Symbol	MIN(mm)	MAX(mm)
A	1.499	1.750	e	1.27TYP	
A1	0.102	0.249	h	-	-
A2	1.397	-	h1	0.254	0.457
b	0.406TYP		L	0.406	0.889
c	0.2TYP		Θ1	12ºTYP	
D	4.852	4.952	Θ2	12ºTYP	
E	5.842	6.198	Θ3	0	8
E1	3.877	3.997	Θ4	45	

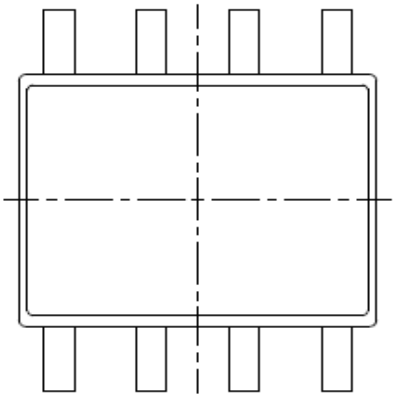
Package outlines



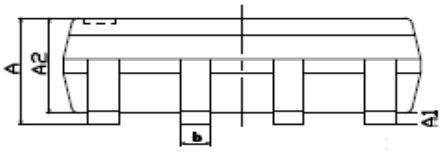
TOP VIEW



SIDE VIEW



BTM VIEW



SIDE VIEW

Mark	Package
PN7101 ABYWX	SOIC8

Note：AB：Product code，Y：Year code； W：Week code； X：Package code

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