

DATA SHEET

BST74A

N-channel vertical D-MOS
transistor

Product specification
File under Discrete Semiconductors, SC13b

April 1995

N-channel vertical D-MOS transistor

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DESCRIPTION	QUICK REFERENCE DATA			
N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.	Drain-source voltage	V_{DS}	max.	200 V
	Gate-source voltage (open drain)	V_{GSO}	max.	20 V
	Drain current (DC)	I_D	max.	250 mA
	Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	1 W
	Drain-source ON-resistance $I_D = 250\text{ mA}; V_{GS} = 10\text{ V}$	$R_{DS(on)}$	typ. max.	6 Ω 12 Ω
FEATURES	Transfer admittance			
	$I_D = 250\text{ mA}; V_{DS} = 15\text{ V}$	$ Y_{fs} $	typ.	250 mS
PINNING - TO-92 VARIANT				
1 = source				
2 = gate				
3 = drain				

PIN CONFIGURATION

MAM146

Note: Various pinout configurations available.

Fig.1 Simplified outline and symbol.

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$ (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		-65 to +150 $^{\circ}\text{C}$
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j-a}$	=	125 K/W
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Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm × 10 mm.

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CHARACTERISTICS $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Drain-source breakdown voltage

 $I_D = 10\text{ }\mu\text{A}; V_{GS} = 0$ $V_{(BR)DS}$ min. 200 V

Drain-source leakage current

 $V_{DS} = 160\text{ V}; V_{GS} = 0$ I_{DSS} max. 10 μA

Gate-source leakage current

 $V_{GS} = 20\text{ V}; V_{DS} = 0$ I_{GSS} max. 100 nA

Gate threshold voltage

 $I_D = 1\text{ mA}; V_{DS} = V_{GS}$ $V_{GS(th)}$ min. 0.8 V
max. 2.8 V

Drain-source ON-resistance (see Fig.4)

 $I_D = 250\text{ mA}; V_{GS} = 10\text{ V}$ $R_{DS(on)}$ typ. 6 Ω
max. 12 Ω

Transfer admittance

 $I_D = 250\text{ mA}; V_{DS} = 15\text{ V}$ $|Y_{fs}|$ typ. 250 mSInput capacitance at $f = 1\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$ C_{iss} typ. 70 pF
max. 90 pFOutput capacitance at $f = 1\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$ C_{oss} typ. 20 pF
max. 30 pFFeedback capacitance at $f = 1\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$ C_{rss} typ. 5 pF
max. 10 pF

Switching times (see Figs 2 and 3)

 $I_D = 250\text{ mA}; V_{DS} = 50\text{ V}; V_{GS} = 0\text{ to }10\text{ V}$ t_{on} typ. 4 ns
max. 10 ns
 t_{off} typ. 15 ns
max. 25 ns

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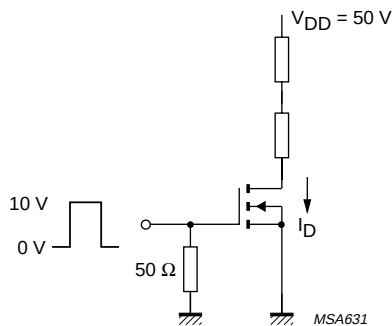


Fig.2 Switching times test circuit.

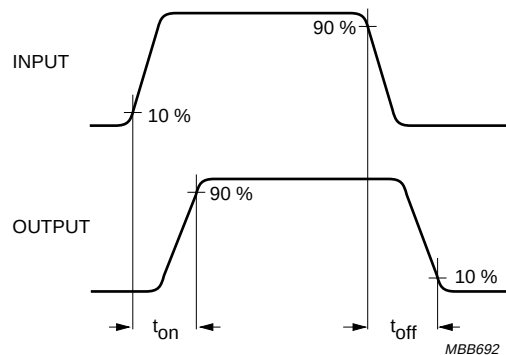


Fig.3 Input and output waveforms.

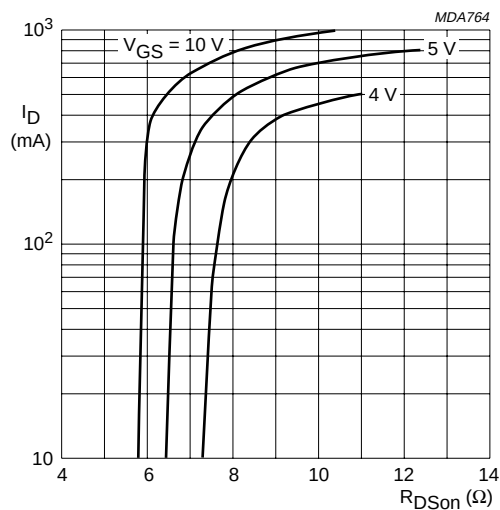


Fig.4 $T_j = 25\text{ }^\circ\text{C}$; typical values.

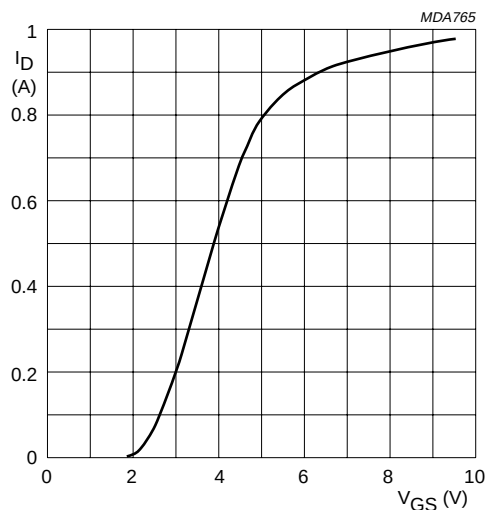
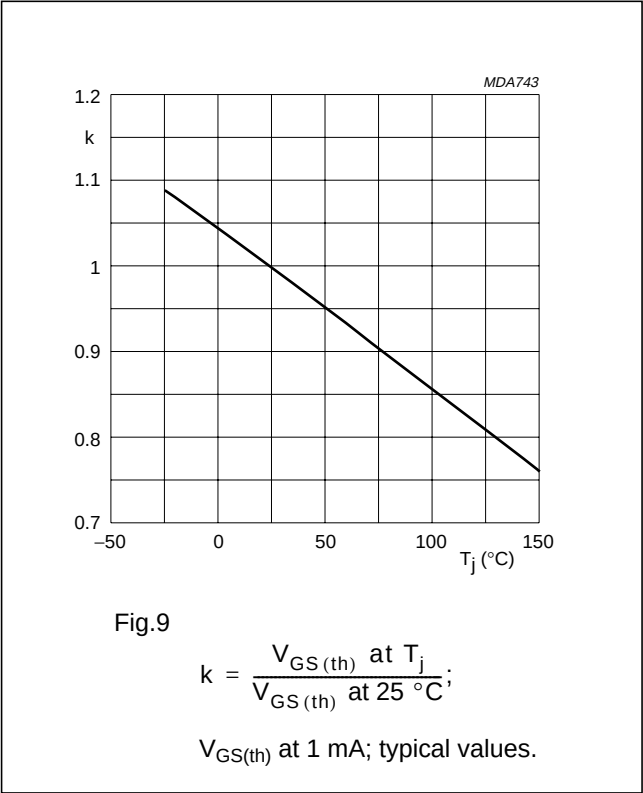
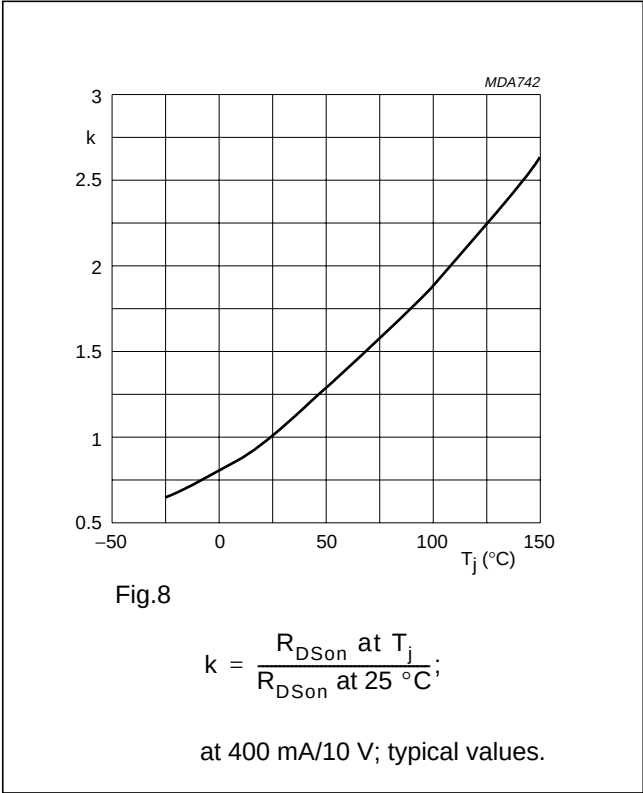
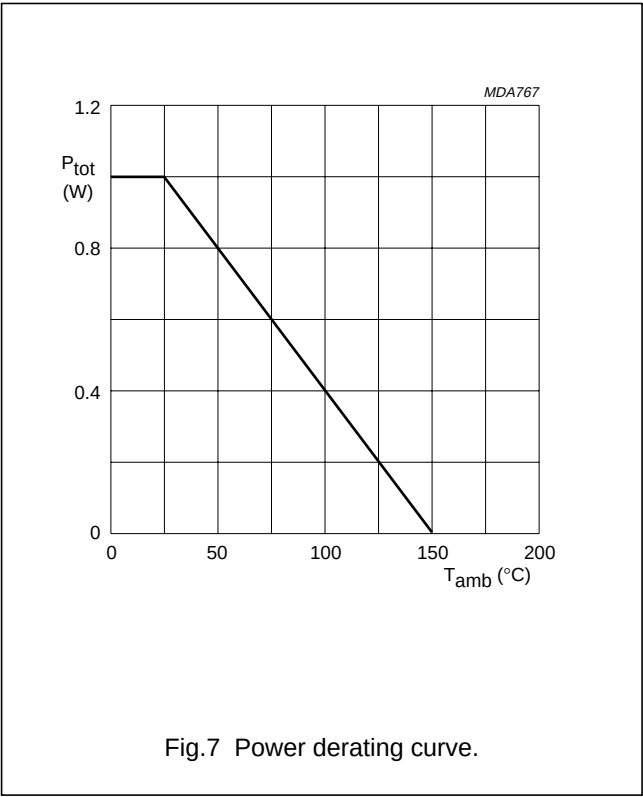
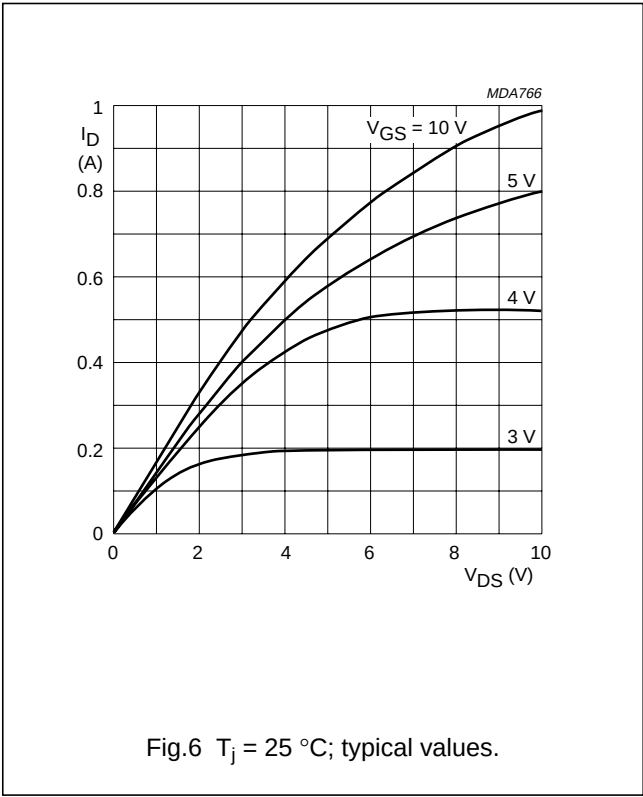


Fig.5 $T_j = 25\text{ }^\circ\text{C}$; $V_{DS} = 10$ V; typical values.

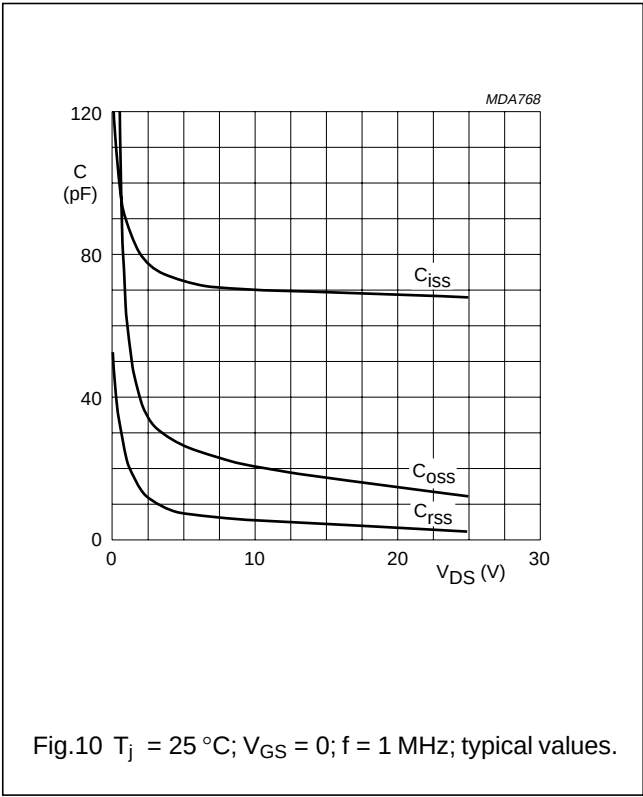
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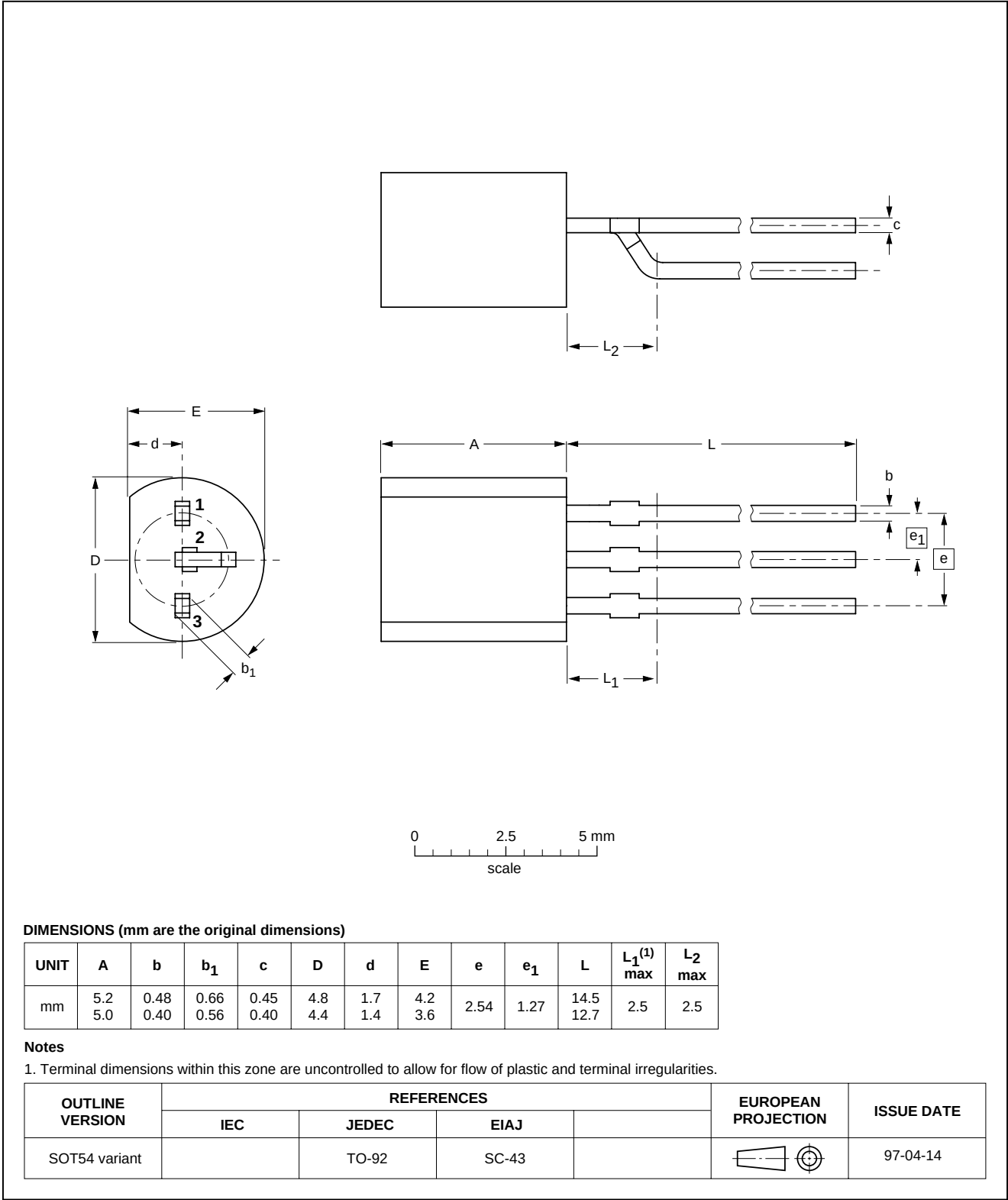
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PACKAGE OUTLINES

Plastic single-ended leaded (through hole) package; 3 leads (on-circle)

SOT54 variant



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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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