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April 1<sup>st</sup>, 2010 Renesas Electronics Corporation

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# MOS FIELD EFFECT TRANSISTOR 2SK3899

# SWITCHING N-CHANNEL POWER MOS FET

# **DESCRIPTION**

The 2SK3899 is N-channel MOS Field Effect Transistor designed for high current switching applications.

# ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3899-ZK	TO-263 (MP-25ZK)

## **FEATURES**

• Super low on-state resistance

 $R_{DS(on)1}$  = 5.3 m $\Omega$  MAX. (Vgs = 10 V, ID = 42 A)

 $R_{DS(on)2} = 6.5 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 4.5 \text{ V, I}_D = 42 \text{ A)}$ 

- Low Ciss: Ciss = 5500 pF TYP.
- Built-in gate protection diode

(TO-263)



# ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C)

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	VDSS	60	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	±84	Α
Drain Current (pulse) Note1	D(pulse)	±336	Α
Total Power Dissipation (Tc = 25°C)	P <sub>T1</sub>	146	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	1.5	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Energy Note2	Eas	245	mJ
Repetitive Avalanche Current Note3	lar	49.5	Α
Repetitive Avalanche Energy Note3	Ear	245	mJ

**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

- **2.** Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = 30 V, R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20  $\rightarrow$  0 V, L = 100  $\mu$ H
- 3. Rg = 25  $\Omega$ , Tch(peak)  $\leq$  150°C

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90%



# **ELECTRICAL CHARACTERISTICS (TA = 25°C)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			10	μΑ
Gate Leakage Current	Igss	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μΑ
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 42 A	35	70		S
Drain to Source On-state Resistance Note	RDS(on)1	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 42 A		4.2	5.3	mΩ
	RDS(on)2	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 42 A		4.9	6.5	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = 10 V		5500		pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V		1050		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		350		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 42 A		19		ns
Rise Time	<b>t</b> r	V <sub>GS</sub> = 10 V		13		ns
Turn-off Delay Time	td(off)	$R_G = 0 \Omega$		91		ns
Fall Time	tf			10		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 48 V		96		nC
Gate to Source Charge	Q <sub>G</sub> s	V <sub>GS</sub> = 10 V		18		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 84 A		23.5		nC
Body Diode Forward Voltage Note	V <sub>F(S-D)</sub>	I <sub>F</sub> = 84 A, V <sub>GS</sub> = 0 V		0.92	1.5	V
Reverse Recovery Time	trr	I <sub>F</sub> = 84 A, V <sub>GS</sub> = 0 V		49		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		70		nC

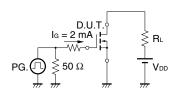
Note Pulsed

# **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

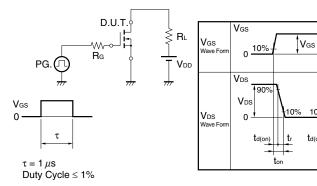
# $V_{GS} = 20 \rightarrow 0 \text{ V}$ $V_{GS} = 20 \rightarrow 0 \text{ V}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{DD}$

# Starting Tch

**TEST CIRCUIT 3 GATE CHARGE** 



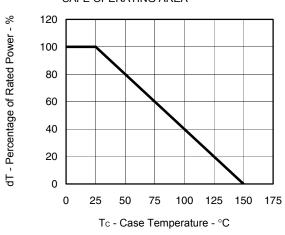
# **TEST CIRCUIT 2 SWITCHING TIME**



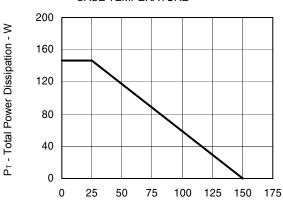


# TYPICAL CHARACTERISTICS (TA = 25°C)

# DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

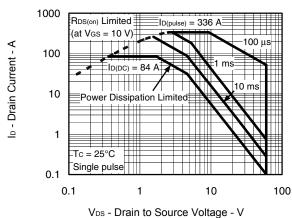


# TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

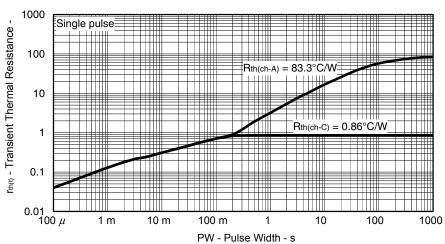


Tc - Case Temperature - °C

# FORWARD BIAS SAFE OPERATING AREA



# TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



0

VGS(off) - Gate Cut-off Voltage - V

0

1

# V<sub>-1</sub> 300 V<sub>GS</sub> = 10 V 4.5 V 4.5 V

DRAIN CURRENT vs.

VDS - Drain to Source Voltage - V

3

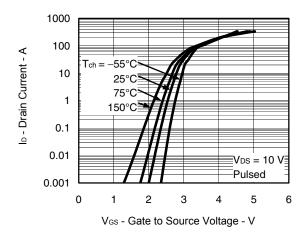
2

Pulsed

5

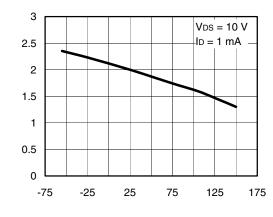
4

# FORWARD TRANSFER CHARACTERISTICS



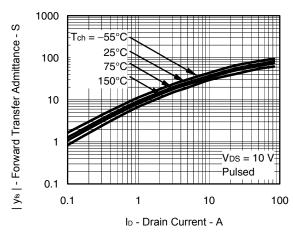
EODWADD TDANSEED A

# GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

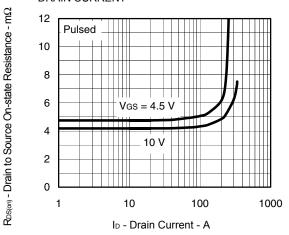


Tch - Channel Temperature - °C

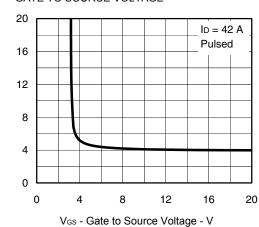
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

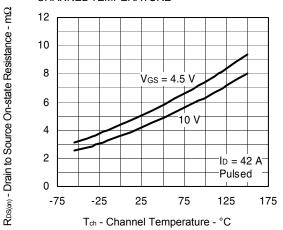


RDS(on) - Drain to Source On-state Resistance - m\Omega

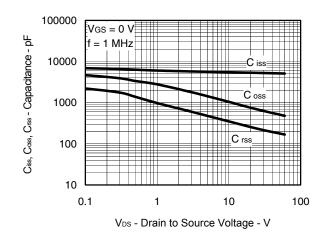
td(on), tr, td(off), tr - Switching Time - ns

IF - Diode Forward Current - A

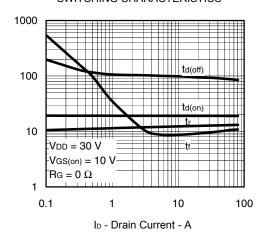
# DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



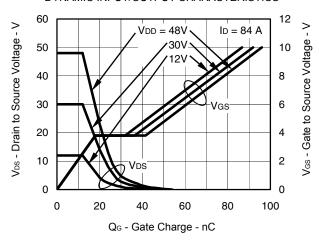
# CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



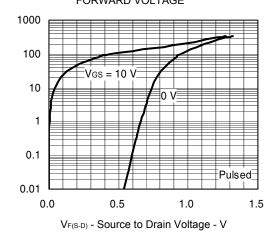
# SWITCHING CHARACTERISTICS



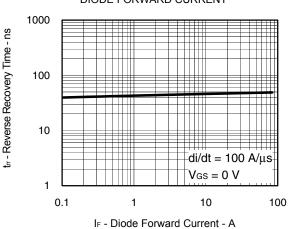
# DYNAMIC INPUT/OUTPUT CHARACTERISTICS

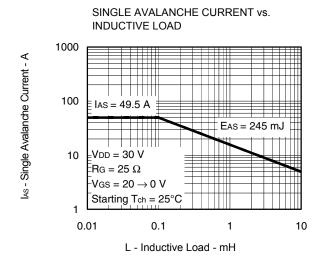


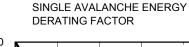
# SOURCE TO DRAIN DIODE FORWARD VOLTAGE

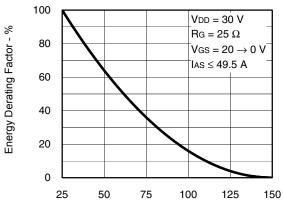


# REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT







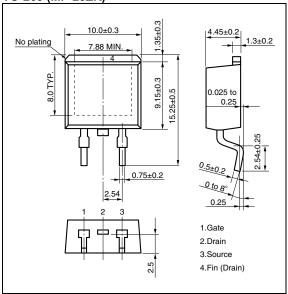


Starting Tch - Starting Channel Temperature - °C

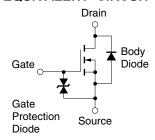


# PACKAGE DRAWING (Unit: mm)

# TO-263 (MP-25ZK)



# **EQUIVALENT CIRCUIT**



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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