

MOS FIELD EFFECT TRANSISTOR μ PA2718GR

SWITCHING P-CHANNEL POWER MOS FET

DESCRIPTION

The μ PA2718GR is P-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and Li-ion battery protection circuit.

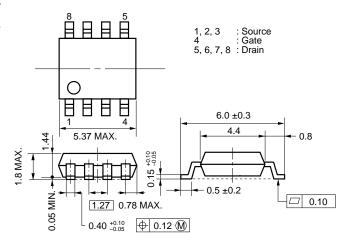
FEATURES

- Low on-state resistance
 - $R_{DS(on)1}$ = 9.0 m Ω MAX. (VGs = -10 V, ID = -6.5 A) $R_{DS(on)2}$ = 14.5 m Ω MAX. (VGs = -4.5 V, ID = -6.5 A)
- Low Ciss: Ciss = 2810 pF TYP.
- Built-in gate protection diode
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2718GR	Power SOP8

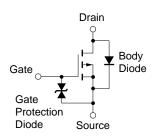
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (Vgs = 0 V)	VDSS	-30	V
Gate to Source Voltage (VDS = 0 V)	Vgss	∓20	V
Drain Current (DC)	ID(DC)	∓13	Α
Drain Current (pulse) Note1	ID(pulse)	∓130	Α
Total Power Dissipation Note2	P _{T1}	2	W
Total Power Dissipation Note3	P _{T2}	2	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note4	las	-13	Α
Single Avalanche Energy Note4	Eas	16.9	mJ

EQUIVALENT CIRCUIT



- **Notes 1.** PW \leq 10 μ s, Duty Cycle \leq 1%
 - 2. Mounted on ceramic substrate of 1200 mm² x 2.2 mm
 - 3. Mounted on glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm, PW = 10 sec
 - **4.** Starting T_{ch} = 25°C, V_{DD} = -15 V, R_G = 25 Ω , L = 100 μ H, V_{GS} = -20 \rightarrow 0 V

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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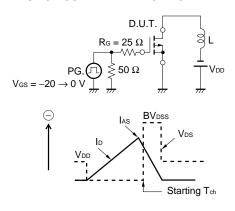


ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

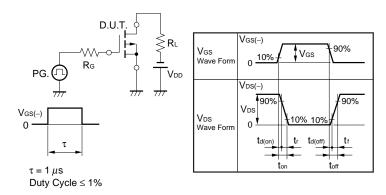
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = -30 V, V _{GS} = 0 V			-1	μΑ
Gate Leakage Current	Igss	V _{GS} = ∓20 V, V _{DS} = 0 V			∓10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = -10 V, I _D = -1 mA	-1.0		-2.5	V
Forward Transfer Admittance Note	y fs	V _{DS} = -10 V, I _D = -6.5 A	9			S
Drain to Source On-state Resistance Note	RDS(on)1	V _{GS} = -10 V, I _D = -6.5 A		7.2	9.0	mΩ
	R _{DS(on)2}	$V_{GS} = -4.5 \text{ V}, I_{D} = -6.5 \text{ A}$		9.9	14.5	mΩ
	RDS(on)3	$V_{GS} = -4.0 \text{ V}, I_D = -6.5 \text{ A}$		11.8	18.2	mΩ
Input Capacitance	Ciss	V _{DS} = -10 V		2810		pF
Output Capacitance	Coss	V _{GS} = 0 V		710		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		460		pF
Turn-on Delay Time	t _{d(on)}	$V_{DD} = -15 \text{ V}, I_D = -6.5 \text{ A}$		13		ns
Rise Time	tr	V _{GS} = -10 V		18		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		510		ns
Fall Time	t f			310		ns
Total Gate Charge	QG	V _{DD} = -24 V		67		nC
Gate to Source Charge	QGS	V _{GS} = -10 V		6.5		nC
Gate to Drain Charge	Q _{GD}	I _D = -13 A		19		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 13 A, V _{GS} = 0 V		0.84		V
Reverse Recovery Time	trr	I _F = 13 A, V _{GS} = 0 V		180		ns
Reverse Recovery Charge	Qrr	di/dt = 50 A/μs		14		nC

Note Pulsed

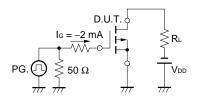
TEST CIRCUIT 1 AVALANCHE CAPABILITY



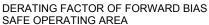
TEST CIRCUIT 2 SWITCHING TIME

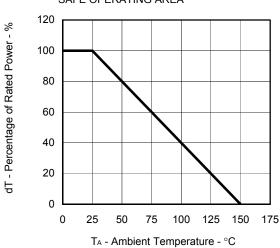


TEST CIRCUIT 3 GATE CHARGE

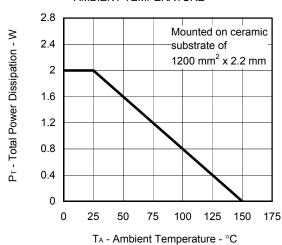


ELECTRICAL CHARACTERISTICS (TA = 25°C)

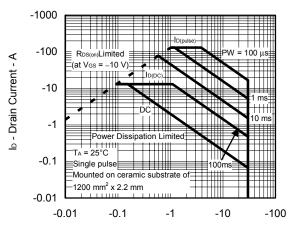




TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

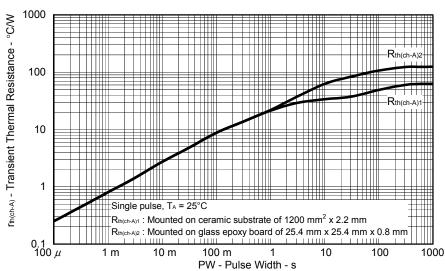


FORWARD BIAS SAFE OPERATING AREA

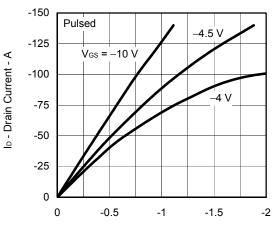


V_{DS} - Drain to Source Voltage - V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

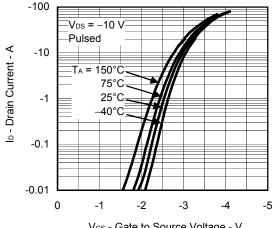


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



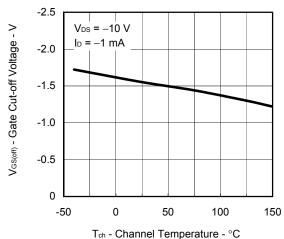
VDS - Drain to Source Voltage - V

FORWARD TRANSFER CHARACTERISTICS

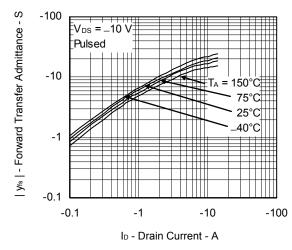


Vgs - Gate to Source Voltage - V

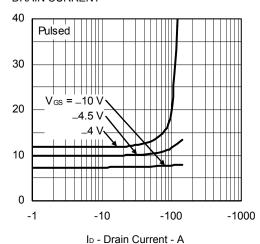
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



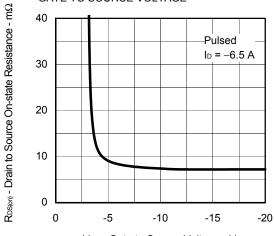
FORWARD TRANSFER ADMITTANCE vs. **DRAIN CURRENT**



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

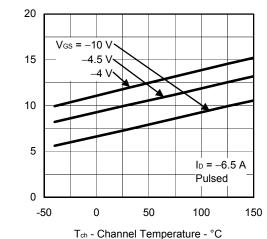


V_{GS} - Gate to Source Voltage - V

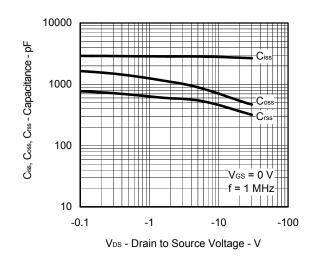
 $\mathsf{Res}_{\text{\tiny{(OI)}}}$ - Drain to Source On-state Resistance - $m\Omega$

R_{DS(on)} - Drain to Source On-state Resistance - mΩ

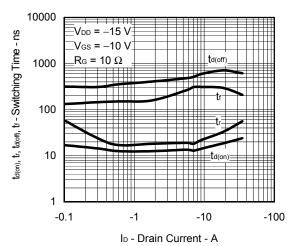
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



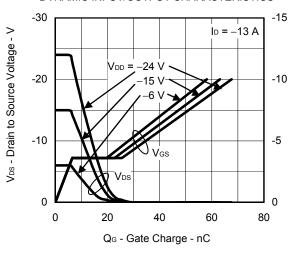
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



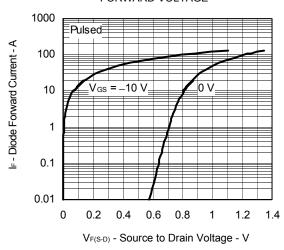
SWITCHING CHARACTERISTICS



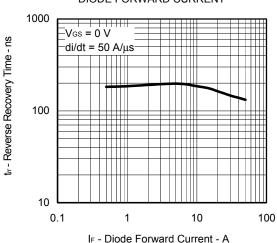
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



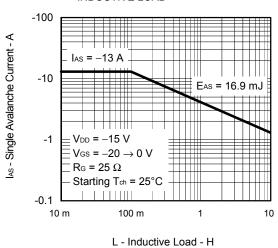
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



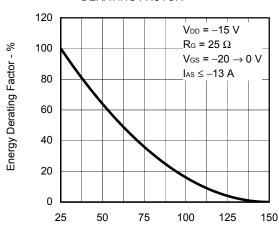
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



Starting Tch - Starting Channel Temperature - °C

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