

SWITCHING
 P-CHANNEL POWER MOS FET

DESCRIPTION

The μ PA2719GR is P-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and Li-ion battery protection circuit.

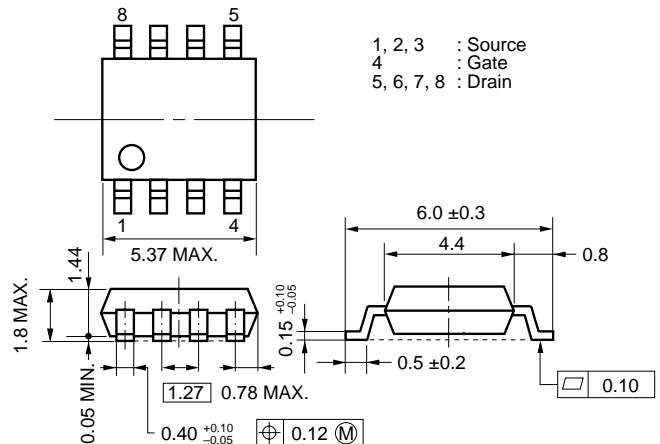
FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 13 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -5.0 \text{ A)}$
 $R_{DS(on)2} = 20.9 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -5.0 \text{ A)}$
- Low C_{iss} : $C_{iss} = 2010 \text{ pF TYP.}$
- Built-in gate protection diode
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA2719GR	Power SOP8

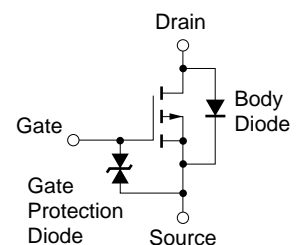
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	-30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±10	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	±100	A
Total Power Dissipation ^{Note2}	P_{T1}	2	W
Total Power Dissipation ^{Note3}	P_{T2}	2	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Single Avalanche Current ^{Note4}	I_{AS}	-10	A
Single Avalanche Energy ^{Note4}	E_{AS}	10	mJ

EQUIVALENT CIRCUIT



- Notes**
1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$
 2. Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 2.2 \text{ mm}$
 3. Mounted on glass epoxy board of $25.4 \text{ mm} \times 25.4 \text{ mm} \times 0.8 \text{ mm}$, $PW = 10 \text{ sec}$
 4. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = -15 \text{ V}$, $R_G = 25 \Omega$, $L = 100 \mu\text{H}$, $V_{GS} = -20 \rightarrow 0 \text{ V}$

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

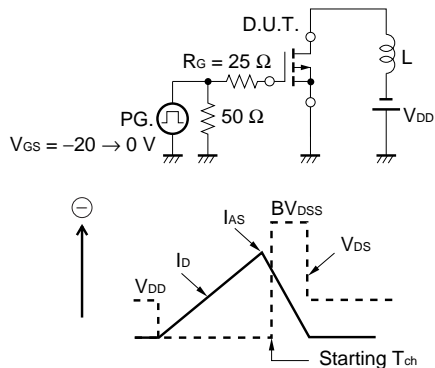
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ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

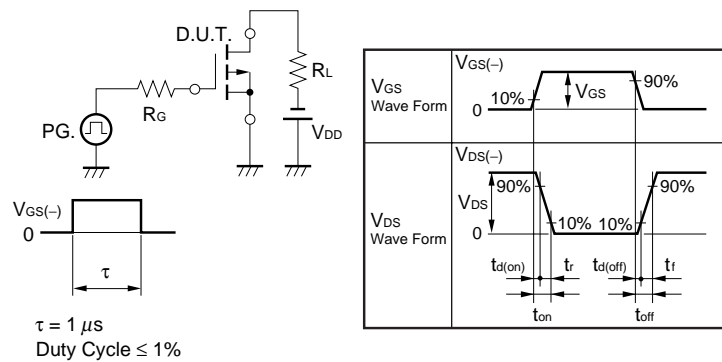
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -30 V, V _{GS} = 0 V			-1	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = -10 V, I _D = -1 mA	-1.0		-2.5	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = -10 V, I _D = -5.0 A	8			S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)1}	V _{GS} = -10 V, I _D = -5.0 A		10.6	13	mΩ
	R _{DS(on)2}	V _{GS} = -4.5 V, I _D = -5.0 A		14.2	20.9	mΩ
	R _{DS(on)3}	V _{GS} = -4.0 V, I _D = -5.0 A		16.6	25.5	mΩ
Input Capacitance	C _{iss}	V _{DS} = -10 V		2010		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		460		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		350		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = -15 V, I _D = -5.0 A		12		ns
Rise Time	t _r	V _{GS} = -10 V		15		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		290		ns
Fall Time	t _f			180		ns
Total Gate Charge	Q _G	V _{DD} = -24 V		43		nC
Gate to Source Charge	Q _{GS}	V _{GS} = -10 V		5.5		nC
Gate to Drain Charge	Q _{GD}	I _D = -10 A		12		nC
Body Diode Forward Voltage ^{Note}	V _{F(S-D)}	I _F = 10 A, V _{GS} = 0 V		0.84		V
Reverse Recovery Time	t _{rr}	I _F = 10 A, V _{GS} = 0 V		105		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 50 A/μs		6.7		nC

Note Pulsed

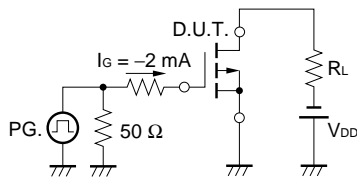
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

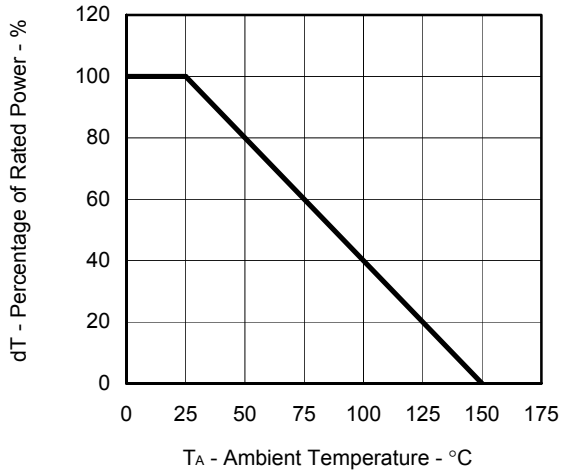


TEST CIRCUIT 3 GATE CHARGE

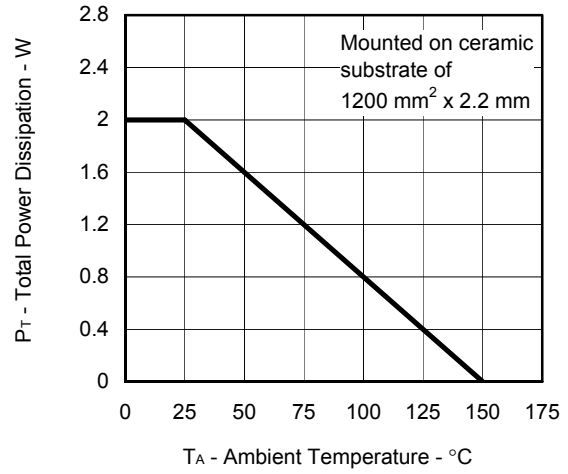


ELECTRICAL CHARACTERISTICS (T_A = 25°C)

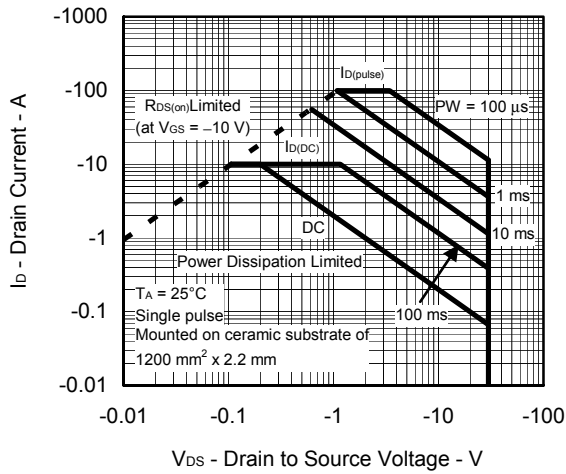
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



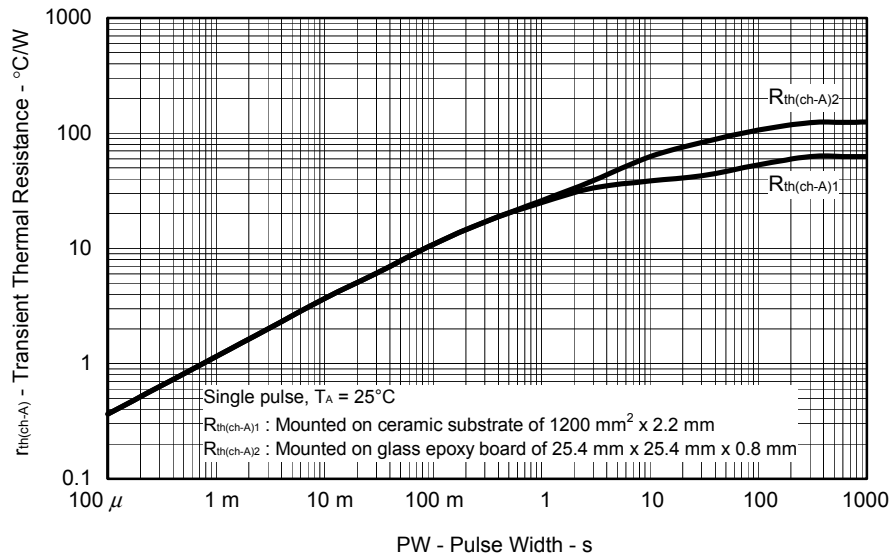
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



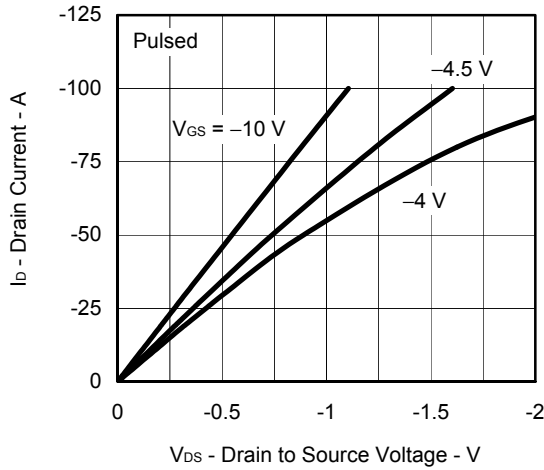
FORWARD BIAS SAFE OPERATING AREA



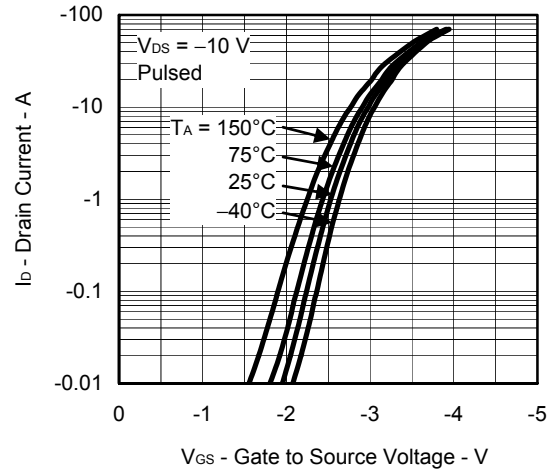
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



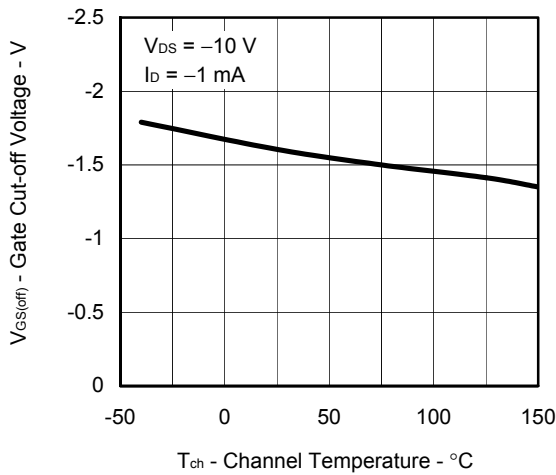
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



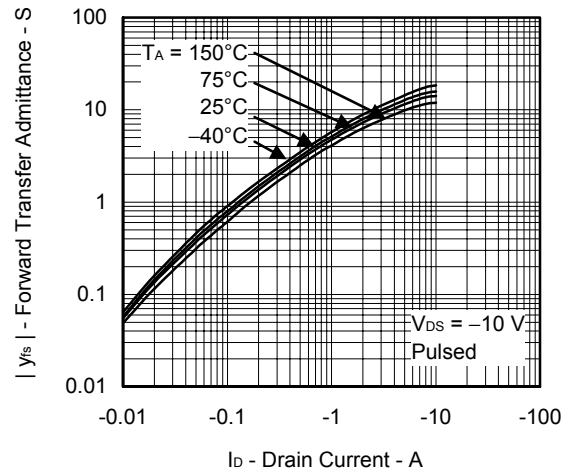
FORWARD TRANSFER CHARACTERISTICS



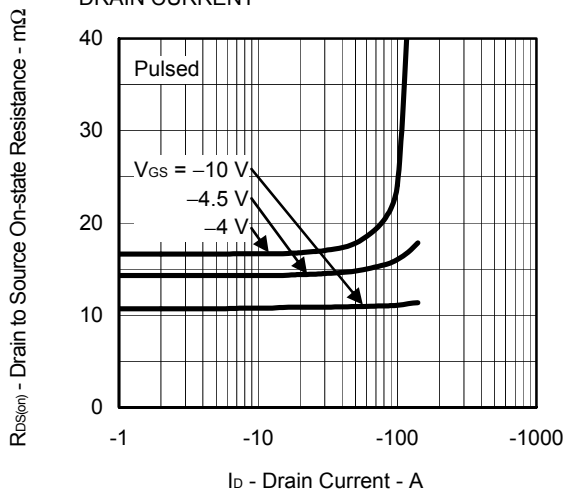
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



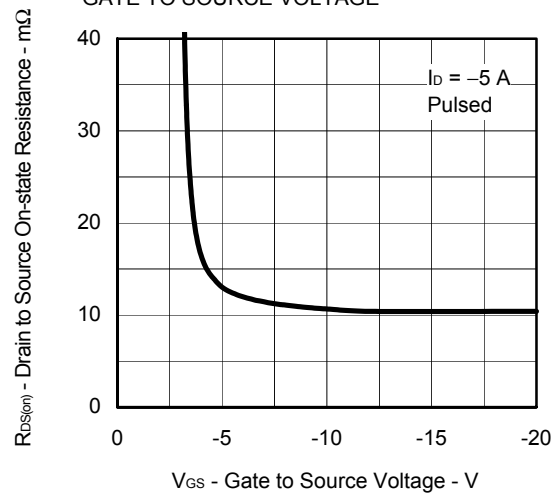
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



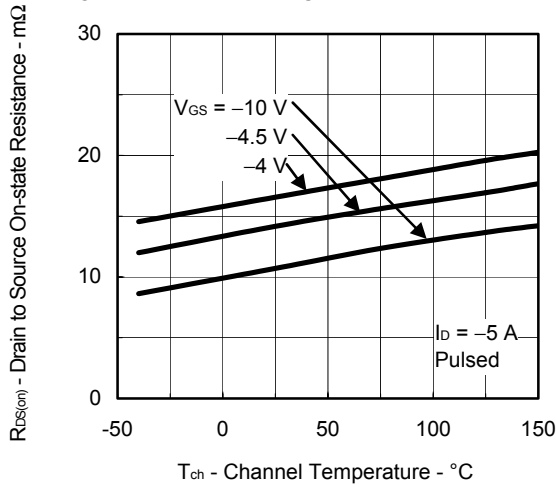
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



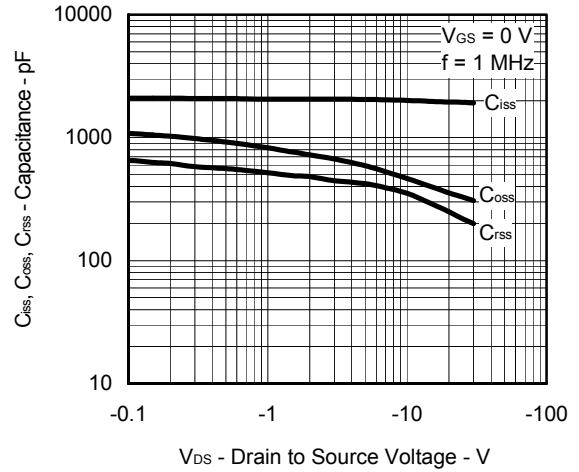
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



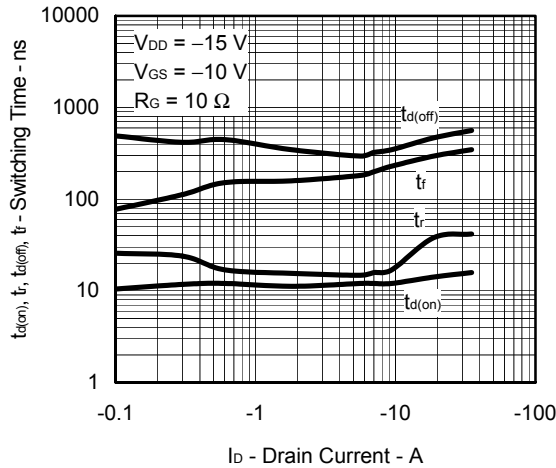
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



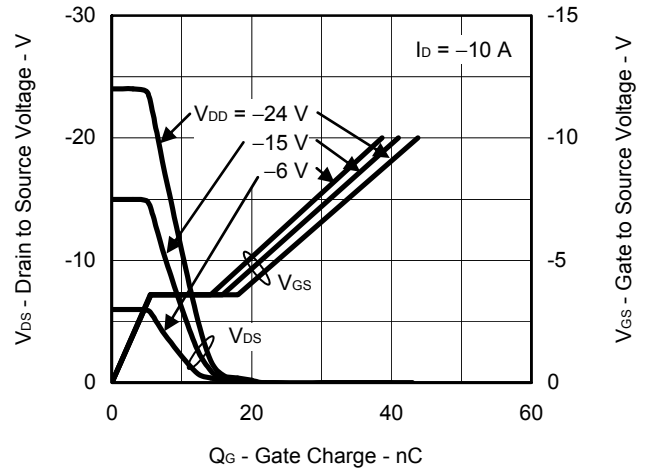
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



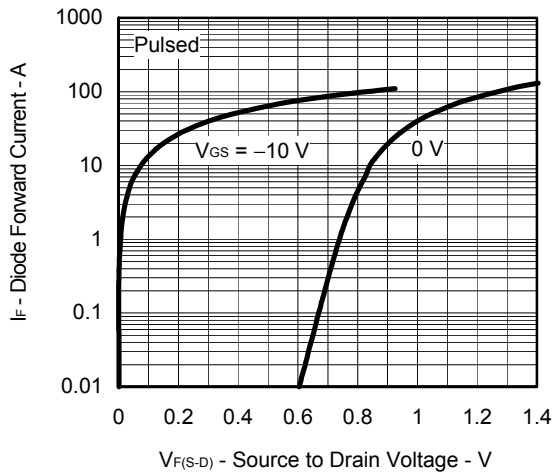
SWITCHING CHARACTERISTICS



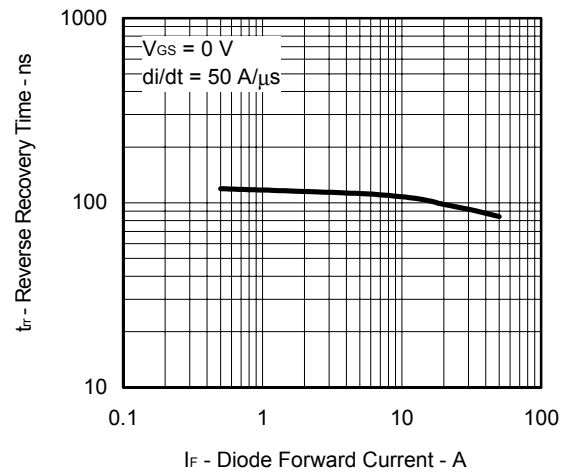
DYNAMIC INPUT/OUTPUT CHARACTERISTICS

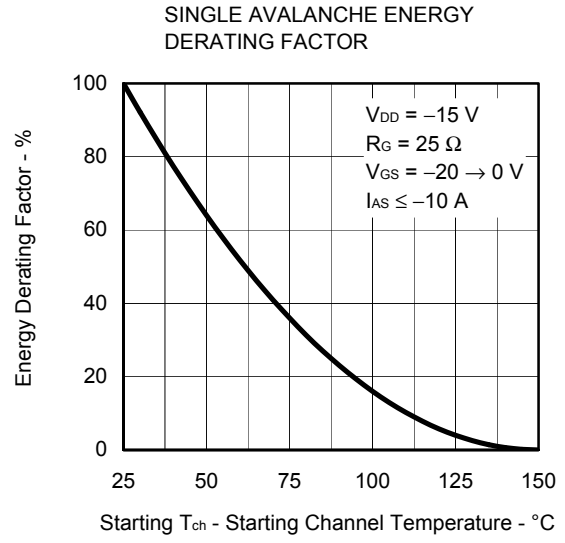
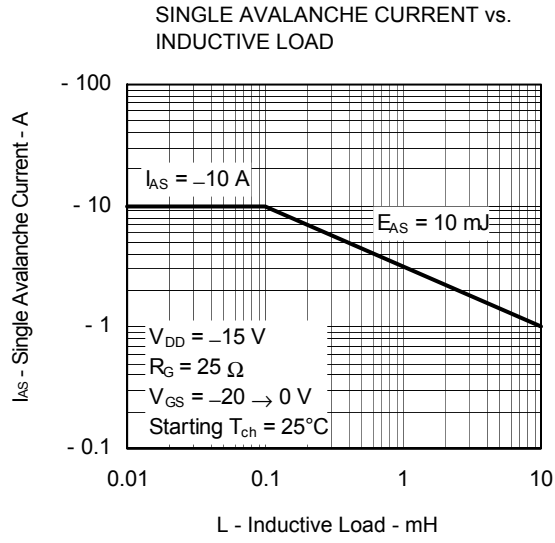


SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT





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