# MPS™

## The Future of Analog IC Technology™

# MP1411
## 2A, 18V, 380KHz
## Step-Down Converter

## DESCRIPTION

The MP1411 is a monolithic step-down switch mode converter with a built in internal power MOSFET. It achieves 2A continuous output current over a wide input supply range with excellent load and line regulation.

Current mode operation provides fast transient response and eases loop stabilization.

Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown. In shutdown mode the regulator draws 23µA of supply current. Programmable soft-start minimizes the inrush supply current and the output overshoot at initial startup.

The MP1411 requires a minimum number of readily available standard external components.
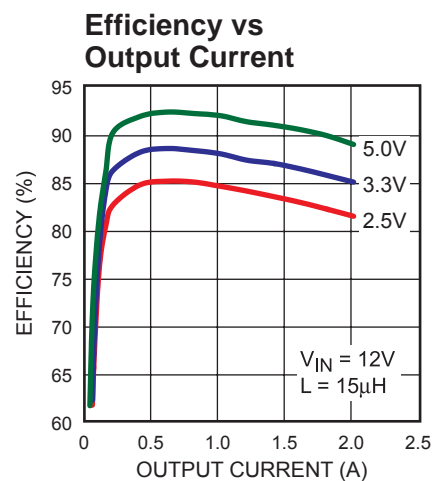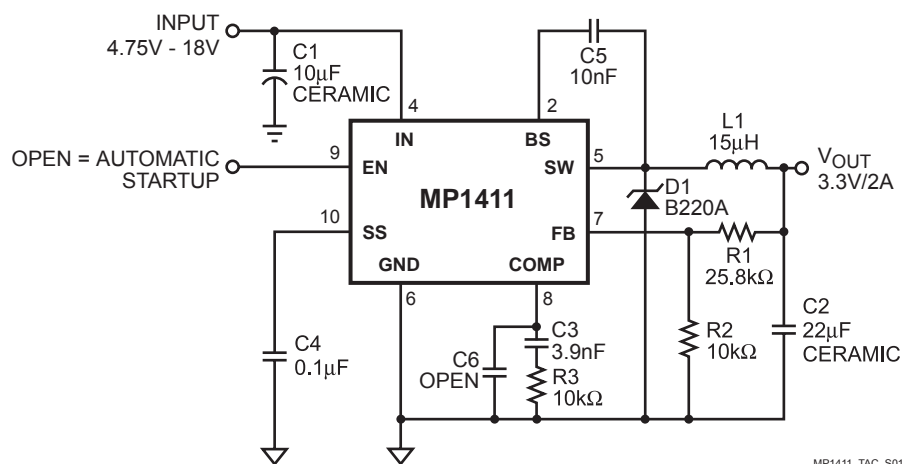
## FEATURES

- 2A Output Current
- 0.2Ω Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- Up to 95% Efficiency
- 23µA Shutdown Mode
- Fixed 380KHz Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Wide 4.75V to 18V Operating Input Range
- Output Adjustable from 0.92V to 16V
- Programmable Under Voltage Lockout
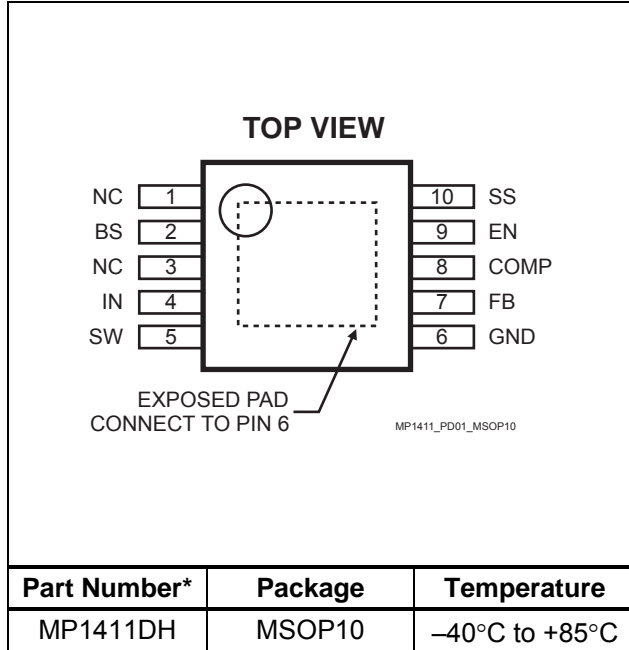- Available in an MSOP10 with Exposed Pad Package

## APPLICATIONS

- Distributed Power Systems
- Battery Charger
- DSL Modems
- Pre-Regulator for Linear Regulators

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## TYPICAL APPLICATION



MP1411_TAC_S01



**Efficiency vs Output Current**

MP1411_EC01

## PACKAGE REFERENCE

**TOP VIEW**

| | | | | |
|---|---|---|---|---|
| NC | 1 | | 10 | SS |
| BS | 2 | | 9 | EN |
| NC | 3 | | 8 | COMP |
| IN | 4 | | 7 | FB |
| SW | 5 | | 6 | GND |

EXPOSED PAD
CONNECT TO PIN 6

MP1411_PD01_MSOP10

| Part Number* | Package | Temperature |
|---|---|---|
| MP1411DH | MSOP10 | –40°C to +85°C |

\* For Tape & Reel, add suffix –Z (eg. MP1411DH–Z)
  For Lead Free, add suffix –LF (eg. MP1411DH–LF–Z)

## ABSOLUTE MAXIMUM RATINGS [1]

Supply Voltage ($V_{IN}$) ..................................... 20V
Switch Node Voltage ($V_{SW}$).......................... 21V
Bootstrap Voltage ($V_{BS}$) ....................... $V_{SW}$ + 6V
Feedback Voltage ($V_{FB}$)................. –0.3V to +6V
Enable/UVLO Voltage ($V_{EN}$)........... –0.3V to +6V
Comp Voltage ($V_{COMP}$) ................... –0.3V to +6V
SS Voltage ($V_{SS}$)........................... –0.3V to +6V
Junction Temperature............................+150°C
Lead Temperature .................................+260°C
Storage Temperature ..............–65°C to +150°C

### *Recommended Operating Conditions* [2]
Supply Voltage ($V_{IN}$) ...................... 4.75V to 18V
Operating Temperature.................–40°C to +85°C

### *Thermal Resistance* [3]   $\theta_{JA}$   $\theta_{JC}$
MSOP10 with Exposed Pad .. 105 ..... 19... °C/W

**Notes:**
1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

## ELECTRICAL CHARACTERISTICS
**$V_{IN}$ = 12V, $T_A$ = +25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Feedback Voltage | $V_{FB}$ | 4.75V $\leq$ $V_{IN}$ $\leq$ 18V | 0.892 | 0.920 | 0.948 | V |
| Upper Switch On Resistance | $R_{DS(ON)1}$ | | | 0.2 | | Ω |
| Lower Switch On Resistance | $R_{DS(ON)2}$ | | | 10 | | Ω |
| Upper Switch Leakage | | $V_{EN}$ = 0V, $V_{SW}$ = 0V | | 0 | 10 | µA |
| Current Limit [4] | | | 2.8 | 3.4 | | A |
| Current Sense Transconductance Output Current to Comp Pin Voltage | $G_{CS}$ | | | 1.95 | | A/V |
| Error Amplifier Voltage Gain | $A_{VEA}$ | | | 400 | | V/V |
| Error Amplifier Transconductance | $G_{EA}$ | $\Delta I_C$ = ±10µA | 550 | 830 | 1150 | µA/V |
| Oscillator Frequency | $f_S$ | | | 380 | | KHz |
| Short Circuit Frequency | | $V_{FB}$ = 0V | | 240 | | KHz |
| Soft-Start Pin Equivalent Output Resistance | | | | 9 | | kΩ |

## ELECTRICAL CHARACTERISTICS *(continued)*

$V_{IN}$ = 12V, $T_A$ = +25°C, unless otherwise noted.

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Maximum Duty Cycle | $D_{MAX}$ | $V_{FB}$ = 0.8V | | 90 | | % |
| Minimum On Time | $t_{ON}$ | | | 100 | | ns |
| EN Shutdown Threshold | | $I_{CC}$ > 100µA | 0.7 | 1.0 | 1.3 | V |
| Enable Pull Up Current | | $V_{EN}$ = 0V | | 1.0 | | µA |
| EN UVLO Threshold Rising | | $V_{EN}$ Rising | 2.37 | 2.50 | 2.62 | V |
| EN UVLO Threshold Hysteresis | | | | 210 | | mV |
| Supply Current (Shutdown) | | $V_{EN} \leq 0.4V$ | | 23 | 36 | µA |
| Supply Current (Quiescent) | | $V_{EN} \geq 3V$ | | 1.1 | 1.3 | mA |
| Thermal Shutdown | | | | 160 | | °C |

**Note:**
4) Slope compensation changes current limit above 40% duty cycle.

## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | NC | No Connect. |
| 2 | BS | Bootstrap. This capacitor (C5) is needed to drive the power switch's gate above the supply voltage. It is connected between the SW and BS pins to form a floating supply across the power switch driver. The voltage across C5 is about 5V and is supplied by the internal +5V supply when the SW pin voltage is low. |
| 3 | NC | No Connect. |
| 4 | IN | Supply Voltage. The MP1411 operates from a +4.75V to +18V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input. |
| 5 | SW | Switch. This connects the inductor to either IN through M1 or to GND through M2. |
| 6 | GND | Ground. This pin is the voltage reference for the regulated output voltage. For this reason care must be taken in its layout. This node should be placed outside of the D1 to C1 ground path to prevent switching current spikes from inducing voltage noise into the part. |
| 7 | FB | Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. To prevent current limit runaway during a short circuit fault condition the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 400mV. |
| 8 | COMP | Compensation. This node is the output of the transconductance error amplifier and the input to the current comparator. Frequency compensation is done at this node by connecting a series R-C to ground. See the compensation section for exact details. |
| 9 | EN | Enable/UVLO. A voltage greater than 2.62V enables operation. Leave EN unconnected for automatic startup. An Under Voltage Lockout (UVLO) function can be implemented by the addition of a resistor divider from $V_{IN}$ to GND. For complete low current shutdown the EN pin voltage needs to be less than 700mV. |
| 10 | SS | Soft-Start. Connect SS to an external capacitor to program the soft-start. If unused, leave it open. |

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# OPERATION

The MP1411 is a current mode regulator. That is, the COMP pin voltage is proportional to the peak inductor current. At the beginning of a cycle: the upper transistor M1 is off; the lower transistor M2 is on (see Figure 1); the COMP pin voltage is higher than the current sense amplifier output; and the current comparator's output is low. The rising edge of the 380KHz CLK signal sets the RS Flip-Flop. Its output turns off M2 and turns on M1 thus connecting the SW pin and inductor to the input supply. The increasing inductor current is sensed and amplified by the Current Sense Amplifier. Ramp compensation is summed to Current Sense Amplifier output and compared to the Error Amplifier output by the Current Comparator. When the Current Sense Amplifier plus Slope Compensation signal exceeds the COMP pin voltage, the RS Flip-Flop is reset and the

MP1411 reverts to its initial M1 off, M2 on state. If the Current Sense Amplifier plus Slope Compensation signal does not exceed the COMP voltage, then the falling edge of the CLK resets the Flip-Flop.

The output of the Error Amplifier integrates the voltage difference between the feedback and the 0.92V bandgap reference. The polarity is such that an FB pin voltage lower than 0.92V increases the COMP pin voltage. Since the COMP pin voltage is proportional to the peak inductor current an increase in its voltage increases current delivered to the output. The lower 10Ω switch ensures that the bootstrap capacitor voltage is charged during light load conditions. External Schottky Diode D1 carries the inductor current when M1 is off.
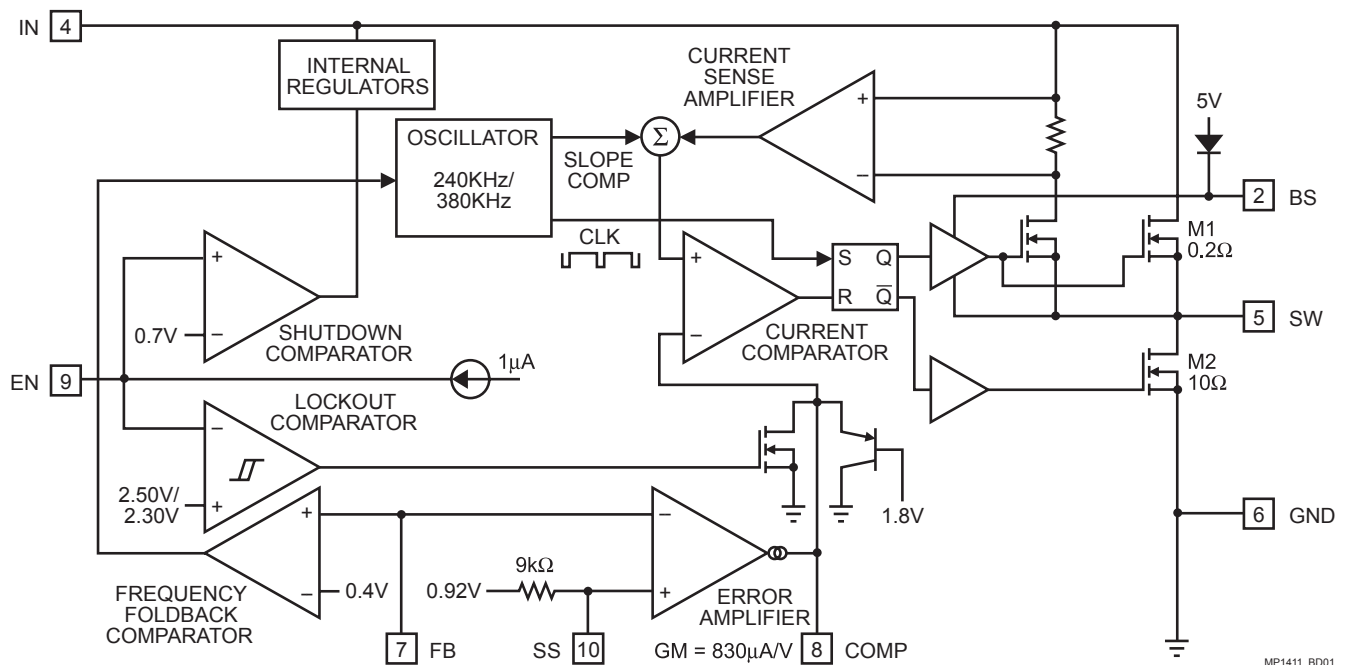


**Figure 1—Functional Block Diagram**

MP1411 Rev. 1.2
12/5/2005

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# APPLICATION INFORMATION

## COMPONENT SELECTION

### Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB pin. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \frac{R2}{R1+R2}$$

Where $V_{FB}$ is the feedback voltage and $V_{OUT}$ is the output voltage.

Thus the output voltage is:

$$V_{OUT} = 0.92 \times \frac{R1+R2}{R2}$$

A typical value for R2 can be as high as 100kΩ, but a typical value is 10kΩ. Using that value, R1 is determined by:

$$R1 = 10.87 \times (V_{OUT} - 0.92)$$

For example, for a 3.3V output voltage, R2 is 10kΩ, and R1 is 25.8kΩ.

### Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where $f_S$ is the switching frequency, $\Delta I_L$ is the peak-to-peak inductor ripple current and $V_{IN}$ is the input voltage.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where $I_{LOAD}$ is the load current.

### Output Rectifier Diode

The output rectifier diode supplies the current to the inductor when the high-side switch is off. To reduce losses due to the diode forward voltage and recovery times, use a Schottky diode.

Choose a diode whose maximum reverse voltage rating is greater than the maximum input voltage, and whose current rating is greater than the maximum load current.

### Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice.

Since the input capacitor absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1µF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where $C_{IN}$ is the input capacitance value.

### Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C_O}\right)$$

Where L is the inductor value, $R_{ESR}$ is the equivalent series resistance (ESR) value of the output capacitor and $C_O$ is the output capacitance value.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C_O} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP1411 can be optimized for a wide range of capacitance and ESR values.

### Compensation Components

The MP1411 employs current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP pin is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the characteristics of the control system.

The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{VEA} \times \frac{V_{FB}}{V_{OUT}}$$

Where $R_{LOAD}$ is the load resistor value, $G_{CS}$ is the current sense transconductance and $A_{VEA}$ is the error amplifier voltage gain.

The system has two poles of importance. One is due to the compensation capacitor (C3) and the output resistor of error amplifier, and the other is due to the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}}$$

$$f_{P2} = \frac{1}{2\pi \times C_O \times R_{LOAD}}$$

Where $G_{EA}$ is the error amplifier transconductance.

The system has one zero of importance, due to the compensation capacitor (C3) and the compensation resistor (R3). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$f_{ESR} = \frac{1}{2\pi \times C_O \times R_{ESR}}$$

In this case, a third pole set by the compensation capacitor (C6) and the compensation resistor (R3) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$f_{P3} = \frac{1}{2\pi \times C6 \times R3}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important.

Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause the system to become unstable. A good rule of thumb is to set the crossover frequency to below one-tenth of the switching frequency. To optimize the compensation components, the following procedure can be used:

1. Choose the compensation resistor (R3) to set the desired crossover frequency. Determine the R3 value by the following equation:

$$R3 = \frac{2\pi \times C_O \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

Where $f_C$ is the desired crossover frequency, which is typically less than one tenth of the switching frequency.

2. Choose the compensation capacitor (C3) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero, $f_{Z1}$, to below one forth of the crossover frequency provides sufficient phase margin. Determine the C3 value by the following equation:

$$C3 > \frac{2}{\pi \times R3 \times f_C}$$

Where R3 is the compensation resistor value.

3. Determine if the second compensation capacitor (C6) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency, or the following relationship is valid:

$$\frac{1}{2\pi \times C_O \times R_{ESR}} < \frac{f_S}{2}$$

If this is the case, then add the second compensation capacitor (C6) to set the pole $f_{P3}$ at the location of the ESR zero. Determine the C6 value by the equation:

$$C6 = \frac{C_O \times R_{ESR}}{R3}$$

**External Bootstrap Diode**

For applications with large duty cycles, it is recommended that an external boost diode be connected to a fixed 5V. This helps improve the efficiency of the MP1411 regulator and also avoids the problems caused by the decrease of BS voltage with large duty cycles. The fixed 5V can be pulled from the input of the system the output generated by the power supply. The boost diode can be a low cost one such as IN4148 or BAT54.
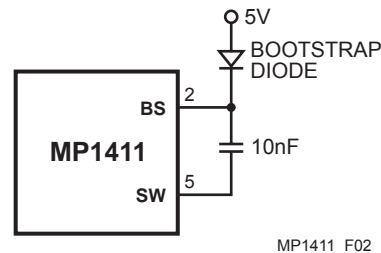


**Figure 2—External Bootstrap Diode**

**Power Dissipation and Temperature Rise**

The power dissipation of the MP1411 is mostly from the conduction loss of the internal main switch. This power loss is estimated to be:

$$P_{LOSS} \cong \frac{V_{OUT}}{V_{IN}} \times I_{OUT}^2 \times 0.18\Omega \times 1.3$$

Where 1.3 is a temperature coefficient factor that reflects the increase in the $R_{DS(ON)}$ resistance at elevated temperatures.

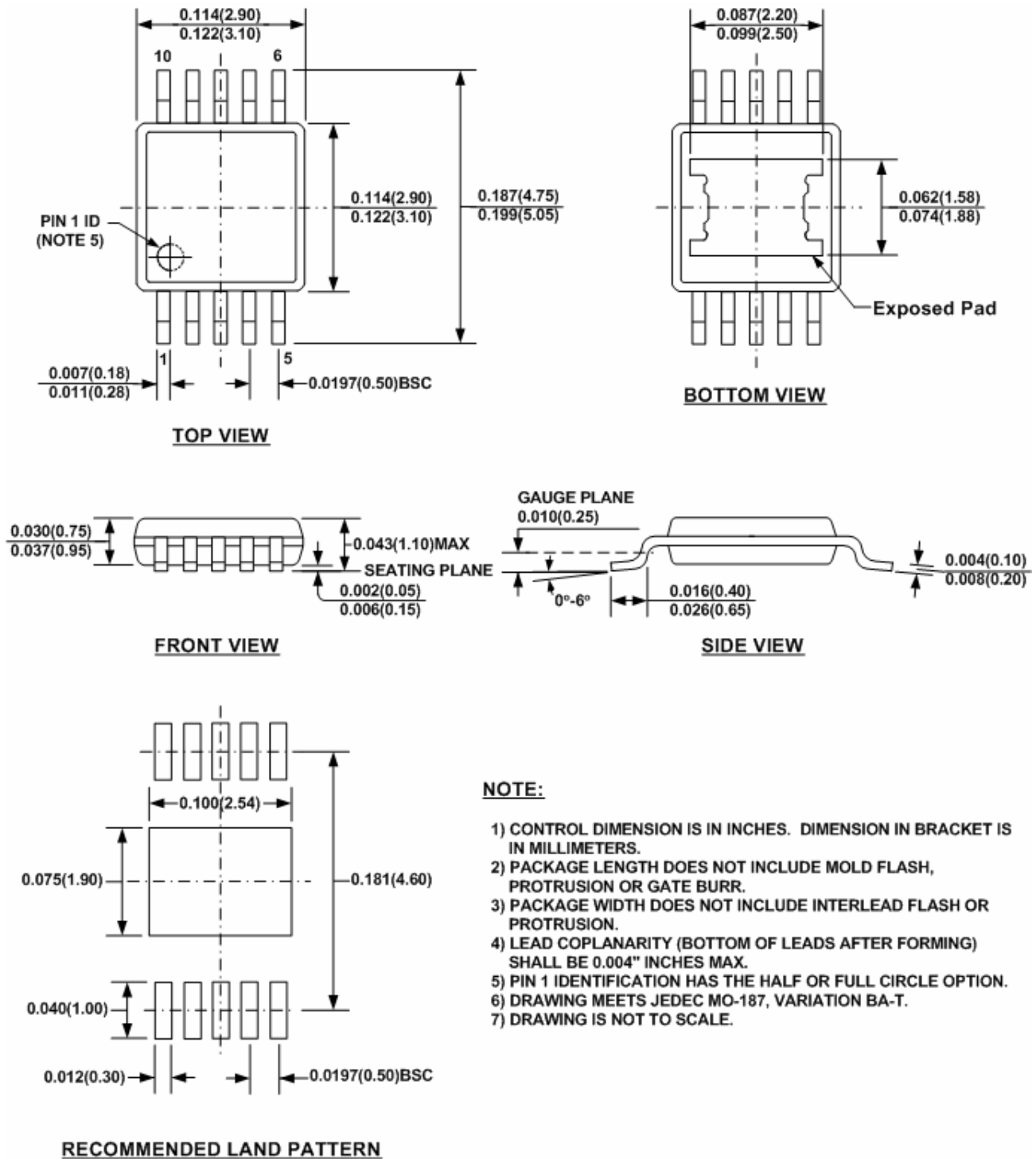For example: for $V_{IN}$ = 12V, $V_{OUT}$ = 3.3V and $I_{OUT}$ = 2A:

$$P_{LOSS} \cong \frac{3.3V}{12V} \times (2A)^2 \times 0.18\Omega \times 1.3 = 0.26W$$

Because the thermal resistance $\theta_{JA}$ is 105°C/W, the resulting rise in temperature between junction and ambient is approximately 27°C. Therefore, caution must be exercised when using the MP1411 in applications with high duty cycles.

# PACKAGE INFORMATION

## MSOP10 (WITH EXPOSED PAD)



0.114(2.90)
0.122(3.10)

10    6

0.114(2.90)
0.122(3.10)

0.187(4.75)
0.199(5.05)

PIN 1 ID
(NOTE 5)

0.007(0.18)
0.011(0.28)    1

5

0.0197(0.50)BSC

**TOP VIEW**

0.087(2.20)
0.099(2.50)

0.062(1.58)
0.074(1.88)

Exposed Pad

**BOTTOM VIEW**

0.030(0.75)
0.037(0.95)

0.043(1.10)MAX

SEATING PLANE

0.002(0.05)
0.006(0.15)

**FRONT VIEW**

GAUGE PLANE
0.010(0.25)

0°-6°

0.016(0.40)
0.026(0.65)

0.004(0.10)
0.008(0.20)

**SIDE VIEW**

0.100(2.54)

0.075(1.90)

0.181(4.60)

0.040(1.00)

0.012(0.30)

0.0197(0.50)BSC

**RECOMMENDED LAND PATTERN**

**NOTE:**

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS THE HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-187, VARIATION BA-T.
7) DRAWING IS NOT TO SCALE.

MP1411 Rev. 1.2
12/5/2005

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