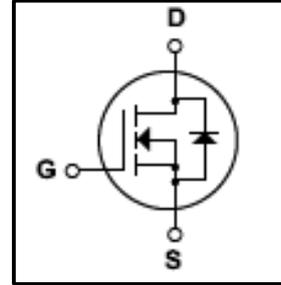


Silicon N-Channel MOSFET

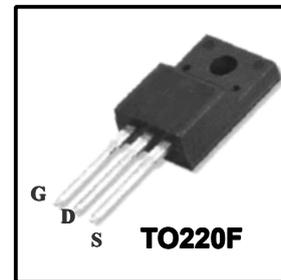
Features

- 8A,500V, $R_{DS(on)}$ (Max 0.8 Ω)@ $V_{GS}=10V$
- Ultra-low Gate Charge(Typical 48nC)
- Fast Switching Capability
- 100%Avalanche Tested
- Isolation Voltage ($V_{ISO} = 4000V$ AC)
- Maximum Junction Temperature Range(150°C)



General Description

This Power MOSFET is produced using Winsemi's advanced planarstripe, VDMOS technology. This latest technology has been especially designed to minimize on-state resistance, have a high rugged avalanche characteristics. This devices is specially well suited for high efficiency switch model power supplies, power factor correction bridge and full bridge resonant topology line a and half electronic lamp ballast.



Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DSS}	Drain Source Voltage	500	V
I_D	Continuous Drain Current(@ $T_c=25^\circ C$)	8*	A
	Continuous Drain Current(@ $T_c=100^\circ C$)	5.1*	A
I_{DM}	Drain Current Pulsed (Note1)	32*	A
V_{GS}	Gate to Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	320	mJ
E_{AR}	Repetitive Avalanche Energy (Note 1)	13.4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	3.5	V/ns
P_D	Total Power Dissipation(@ $T_c=25^\circ C$)	44	W
	Derating Factor above 25°C	0.35	W/°C
T_J, T_{stg}	Junction and Storage Temperature	-55~150	°C
T_L	Maximum lead Temperature for soldering purposes	300	°C

*Drain current limited by junction temperature

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
R_{QJC}	Thermal Resistance, Junction-to-Case	-	-	2.84	°C/W
R_{QCS}	Thermal Resistance, Case to Sink	-	0.5	-	°C/W
R_{QA}	Thermal Resistance, Junction-to-Ambient	-	-	62	°C/W

Electrical Characteristics (Tc = 25°C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit	
Gate leakage current	I_{GSS}	VGS = ± 30 V, VDS = 0 V	-	-	± 100	nA	
Gate-source breakdown voltage	$V_{(BR)GSS}$	IG = ± 10 μ A, VDS = 0 V	± 30	-	-	V	
Drain cut-off current	I_{DSS}	VDS = 400 V, VGS = 0 V	-	-	10	μ A	
Drain-source breakdown voltage	$V_{(BR)DSS}$	ID = 250 μ A, VGS = 0 V	500	-	-	V	
Break Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	$I_D=250\mu A$, Referenced to 25°C	-	0.5	-	V/°C	
Gate threshold voltage	$V_{GS(th)}$	VDS = 10 V, ID = 250 μ A	2	-	4	V	
Drain-source ON resistance	$R_{DS(ON)}$	VGS = 10 V, ID = 4.0A	-	0.65	0.80	Ω	
Forward Transconductance	gfs	VDS = 40 V, ID = 4.0A	-	7.3	-	S	
Input capacitance	C_{iss}	VDS = 25 V,	-	1400	1800	pF	
Reverse transfer capacitance	C_{riss}	VGS = 0 V,	-	34	44		
Output capacitance	C_{oss}	f = 1 MHz	-	145	190		
Switching time	Rise time	tr	VDD = 250 V,	-	22	55	ns
	Turn-on time	ton	ID = 8 A	-	65	140	
	Fall time	tf	RG = 9.1 Ω	-	125	260	
	Turn-off time	toff	RD = 31 Ω (Note4,5)	-	75	160	
Total gate charge (gate-source plus gate-drain)	Qg	VDD = 400 V,	-	59	70	nC	
Gate-source charge	Qgs	VGS = 10 V,	-	7	9		
Gate-drain ("miller") Charge	Qgd	ID = 8 A (Note4,5)	-	28	32		

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit
Continuous drain reverse current	I_{DR}	-	-	-	8	A
Pulse drain reverse current	I_{DRP}	-	-	-	32	A
Forward voltage (diode)	V_{DSF}	IDR = 8 A, VGS = 0 V	-	-	1.4	V
Reverse recovery time	trr	IDR = 8A, VGS = 0 V,	-	390	-	ns
Reverse recovery charge	Qrr	dIDR / dt = 100 A / μ s	-	4.2	-	μ C

Note 1.Repeativity rating :pulse width limited by junction temperature

2.L=9mH, $I_{AS}=8A$, $V_{DD}=50V$, $R_G=25\Omega$,Starting $T_J=25^\circ C$

3. $I_{SD}\leq 8A$, $di/dt\leq 300A/\mu s$, $V_{DD}<BV_{DSS}$,STARTING $T_J=25^\circ C$

4.Pulse Test: Pulse Width $\leq 300\mu s$,Duty Cycle $\leq 2\%$

5.Essentially independent of operating temperature.

This transistor is an electrostatic sensitive device

Please handle with caution

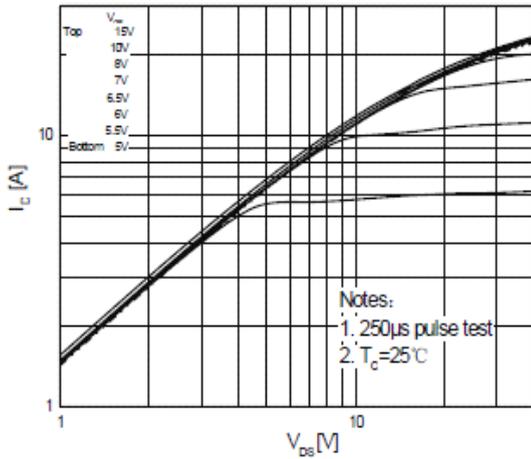


Fig. 1 On-State Characteristics

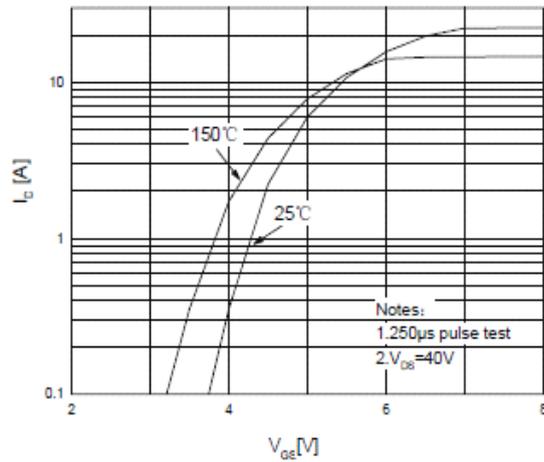


Fig.2 Transfer Characteristics

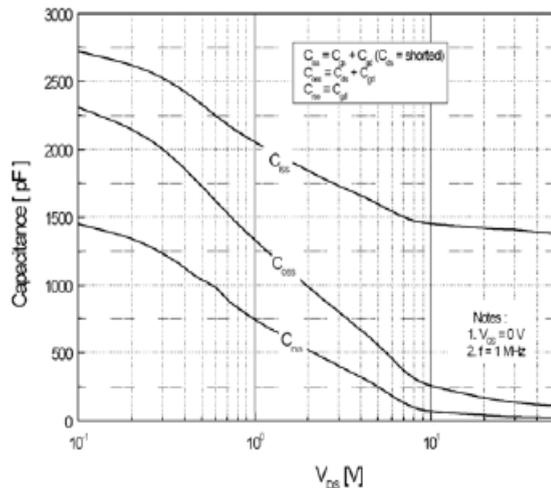


Fig.3 Capacitance Variation vs Drain Voltage

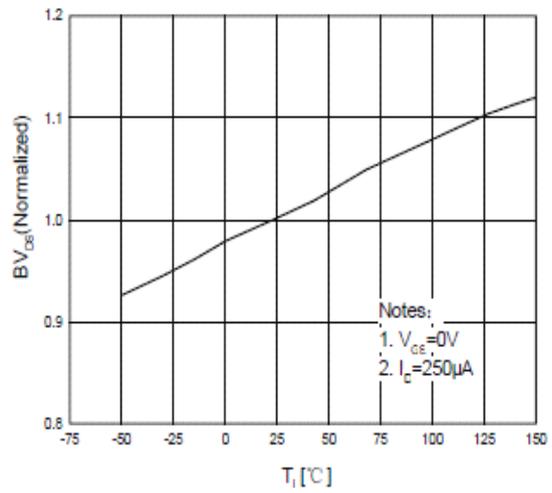


Fig.4 Maximum Avalanche Energy vs On-State Current

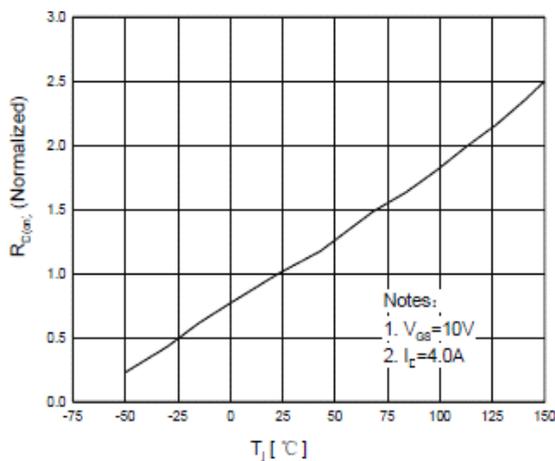


Fig.5 On-Resistance Variation vs Junction Temperature

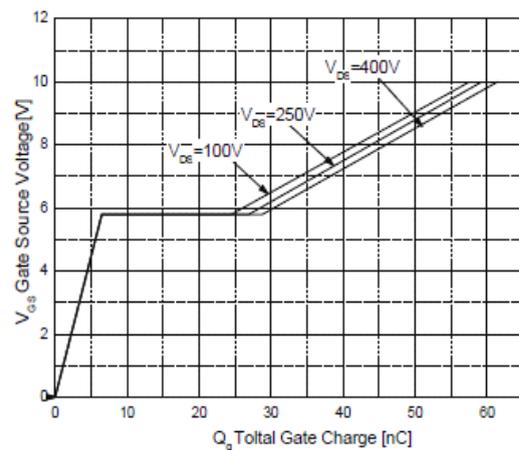


Fig.6 Gate Charge Characteristics

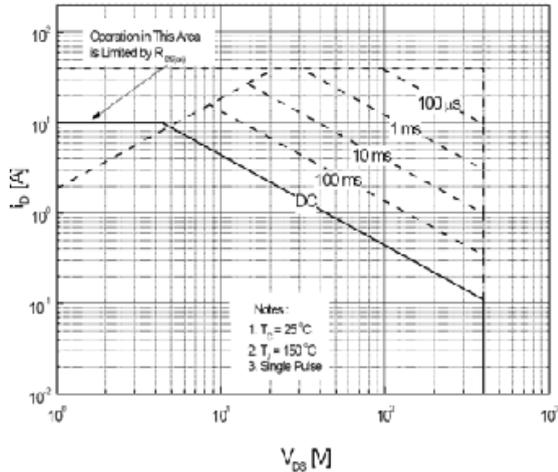


Fig.7 Maximum Safe Operation Area

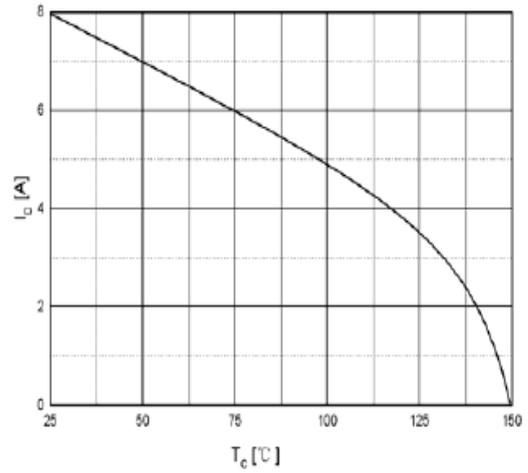


Fig.8 Maximum Drain Current vs Case Temperature

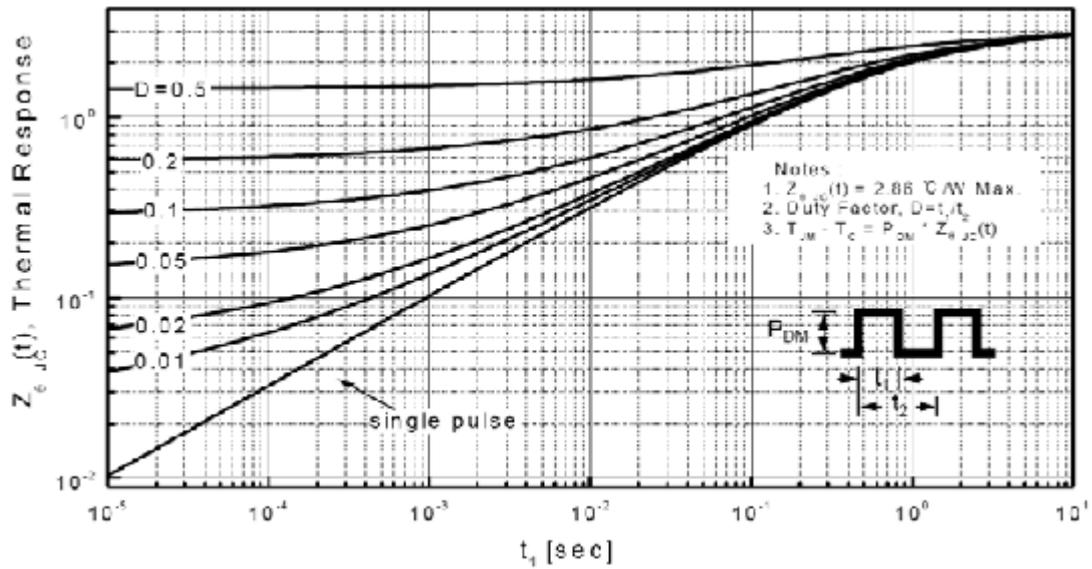


Fig.9 Transient Thermal Response Curve

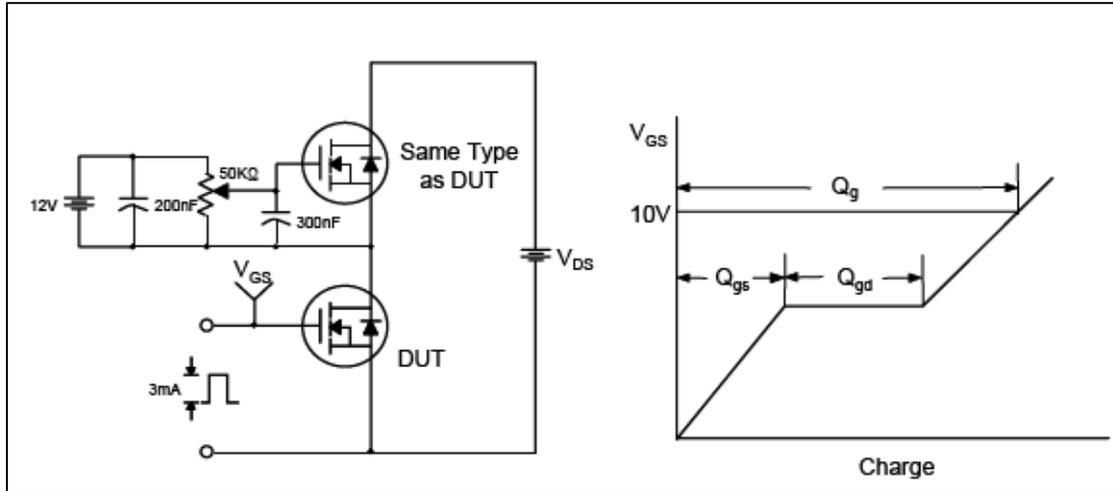


Fig.10 Gate Test Circuit & Waveform

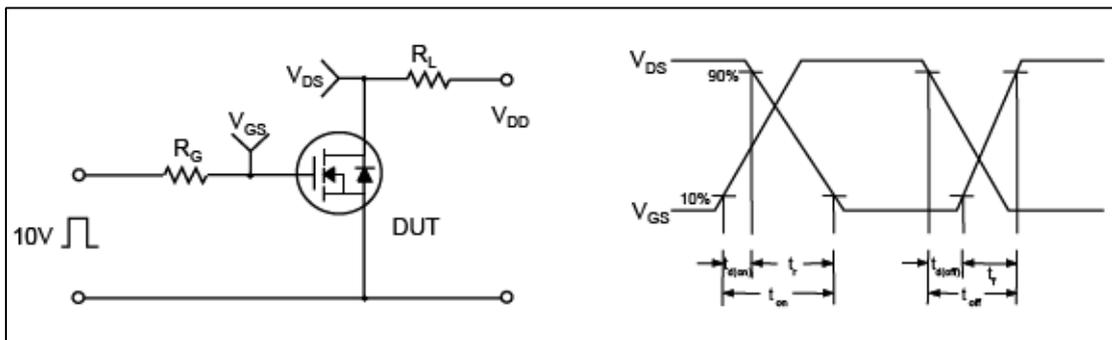


Fig.11 Resistive Switching Test Circuit & Waveform

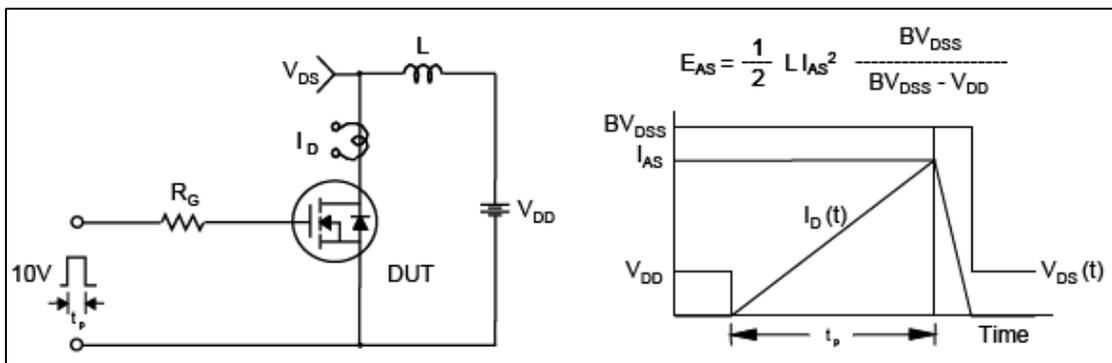


Fig.12 Unclamped Inductive Switching Test Circuit & Waveform

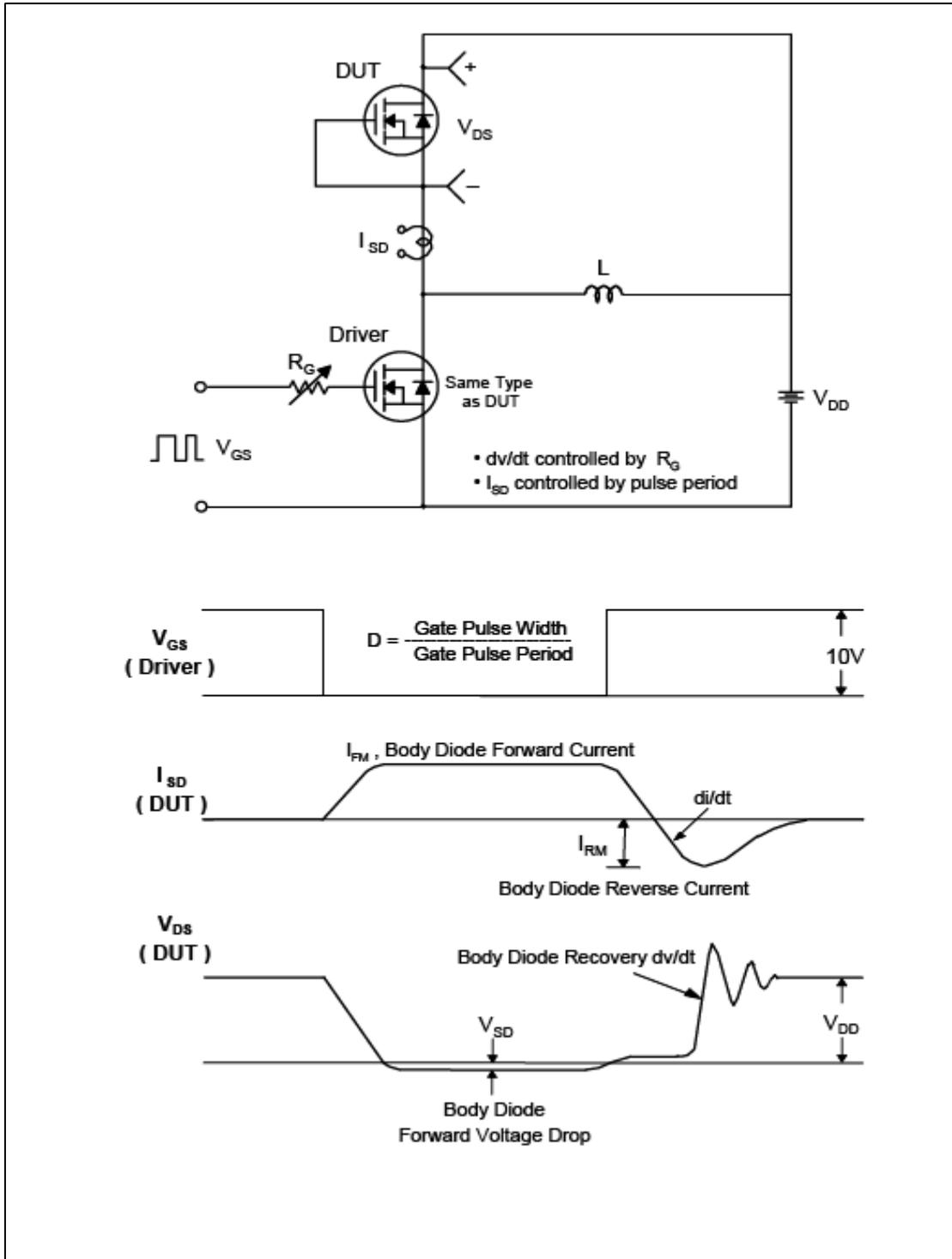


Fig.13 Peak Diode Recovery dv/dt Test Circuit & Waveform

TO-220F Package Dimension

