500V / 600V High Voltage 3-phase Motor Driver ICs

SIM6800M Series

Data Sheet

Description

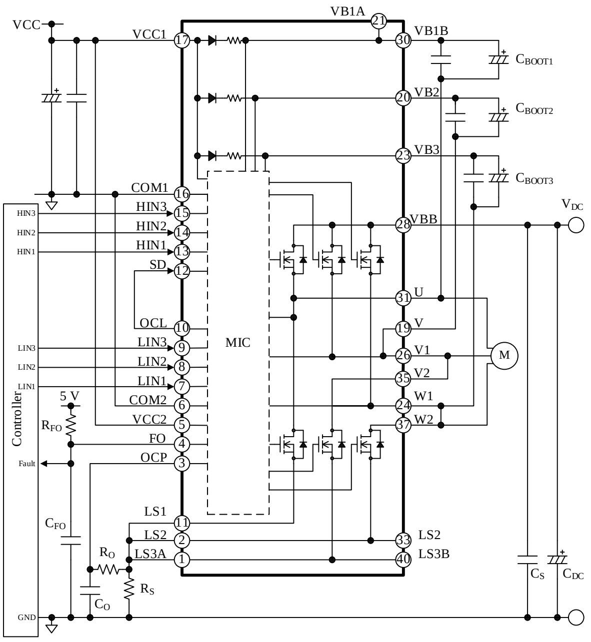
The SIM6800M series are high voltage 3-phase motor driver ICs in which transistors, a pre-driver IC (MIC), and bootstrap circuits (diodes and resistors) are highly integrated.

These products can run on a 3-shunt current detection system and optimally control the inverter systems of small- to medium-capacity motors that require universal input standards.

Features

- Built-in Bootstrap Diodes with Current Limiting Resistors (60 Ω)
- CMOS-compatible Input (3.3 V or 5 V)
- Bare Lead Frame: Pb-free (RoHS compliant)
- Isolation Voltage: 1500 V (for 1 min)
  UL-recognized Component (File No.: E118037)
  (SIM6880M UL Recognition Pending)
- Fault Signal Output at Protection Activation (FO Pin)
- High-side Shutdown Signal Input (SD Pin)
- Protections Include:
  Overcurrent Limit (OCL): Auto-restart
  Overcurrent Protection (OCP): Auto-restart
  Undervoltage Lockout for Power Supply
    High-side (UVLO_VB): Auto-restart
    Low-side (UVLO_VCC): Auto-restart
  Thermal Shutdown (TSD): Auto-restart

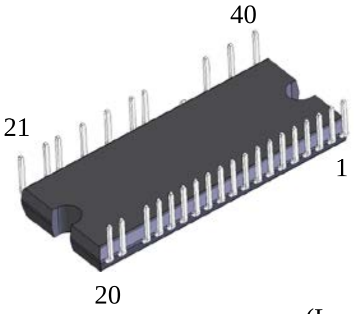
Typical Application (SIM681xM)



Package

DIP40

(Mold Dimensions: 36.0 mm × 14.8 mm × 4.0 mm)



(Leadform 1890)

Not to scale

Selection Guide

Maximum Main Supply Voltage	Output DC Current	Feature	Part Number
500 V	2.0 A	Power MOSFET	SIM6811M
	2.5 A		SIM6812M
	3.0 A		SIM6813M
600 V	2.5 A	IGBT with FRD, low switching dissipation	SIM6880M
	5.0 A		SIM6822M
			SIM6827M

Applications

For motor drives such as:

- Refrigerator Compressor Motor
- Fan Motor and Pump Motor for Washer and Dryer
- Fan Motor for Air Conditioner, Air Purifier, and Electric Fan

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1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, COM1 = COM2 = COM.

Parameter	Symbol	Conditions	Rating	Unit	Remarks
Main Supply Voltage (DC)	V_{DC}	VBB–LS1, VBB–LS2, VBB–LS3	400	V	SIM681xM
			450		SIM682xM SIM6880M
Main Power Voltage (Surge)	$V_{DC(SURGE)}$	VBB–LS1, VBB–LS2, VBB–LS3	450	V	SIM681xM
			500		SIM682xM SIM6880M
IGBT / Power MOSFET Breakdown Voltage	V_{DSS}	V_{CC} = 15 V, I_D = 1 μA, V_{IN} = 0 V	500	V	SIM681xM
	V_{CES}	V_{CC} = 15 V, I_C = 1 mA, V_{IN} = 0 V	600		SIM682xM SIM6880M
Logic Supply Voltage	V_{CC}	VCC1–COM, VCC2–COM	20	V	
	V_{BS}	VB1B–U, VB2–V, VB3–W1	20		
Output Current (1)	I_O	T_C = 25 °C, T_j < 150 °C	2	A	SIM6811M
			2.5		SIM6812M SIM6880M
			3		SIM6813M
			5		SIM6822M SIM6827M
Output Current (Pulse)	I_{OP}	T_C = 25 °C, V_{CC} = 15 V, $P_W \leq$ 1 ms, single pulse	3	A	SIM6811M
			3.75		SIM6812M SIM6880M
			4.5		SIM6813M
			7.5		SIM6822M SIM6827M
Input Voltage	V_{IN}	HIN1–COM, HIN2–COM, HIN3–COM, LIN1–COM, LIN2–COM, LIN3–COM	− 0.5 to 7	V	
FO Pin Voltage	V_{FO}	FO–COM	−0.5 to 7	V	
OCP Pin Voltage	V_{OCP}	OCP–COM	−10 to 5	V	
SD Pin Voltage	V_{SD}	SD–COM	−0.5 to 7	V	
Operating Case Temperature(2)	$T_{C(OP)}$		−30 to 100	°C	
Junction Temperature(3)	T_j		150	°C	
Storage Temperature	T_{stg}		−40 to 150	°C	
Isolation Voltage(4)	$V_{ISO(RMS)}$	Between surface of the case and each pin; AC, 60 Hz, 1 min	1500	V	

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(1) Should be derated depending on an actual case temperature. See Section 15.4.

(2) Refers to a case temperature measured during IC operation.

(3) Refers to the junction temperature of each chip built in the IC, including the controller IC (MIC), transistors, and fast recovery diodes.

(4) Refers to voltage conditions to be applied between the case and all pins. All pins have to be shorted.

2. Recommended Operating Conditions

Unless specifically noted, COM1 = COM2 = COM.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Main Supply Voltage	V_{DC}	VBB–COM	—	300	400	V	
Logic Supply Voltage	V_{CC}	VCC1–COM, VCC2–COM	13.5	15.0	16.5	V	
	V_{BS}	VB1B–U, VB2–V, VB3–W1	13.5	—	16.5	V	
Input Voltage (HINx, LINx, OCP, SD, FO)	V_{IN}		0	—	5.5	V	
Minimum Input Pulse Width	$t_{IN(MIN)ON}$		0.5	—	—	μs	
	$t_{IN(MIN)OFF}$		0.5	—	—	μs	
Dead Time of Input Signal	t_{DEAD}		1.5	—	—	μs	
FO Pin Pull-up Resistor	R_{FO}		3.3	—	10	kΩ	
FO Pin Pull-up Voltage	V_{FO}		3.0	—	5.5	V	
FO Pin Noise Filter Capacitor	C_{FO}		0.001	—	0.01	μF	
Bootstrap Capacitor	C_{BOOT}		1	—	220	μF	
Shunt Resistor	R_S	$I_P \leq 3$ A	390	—	—	mΩ	SIM6811M
		$I_P \leq 3.75$ A	270	—	—		SIM6812M
		$I_P \leq 4.5$ A	270	—	—		SIM6813M
		$I_P \leq 7.5$ A	150	—	—		SIM6822M SIM6827M
RC Filter Resistor	R_O		—	—	100	Ω	
RC Filter Capacitor	C_O		1000	—	2200	pF	SIM6822M SIM6827M
			1000	—	10000		SIM6811M SIM6812M SIM6813M
PWM Carrier Frequency	f_c		—	—	20	kHz	
Operating Case Temperature	$T_{C(OP)}$		—	—	100	°C	

3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, V_{CC} = 15 V, COM1 = COM2 = COM.

3.1 Characteristics of Control Parts

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Power Supply Operation							
Logic Operation Start Voltage	$V_{CC(ON)}$	VCC1–COM, VCC2–COM	10.5	11.5	12.5	V	
	$V_{BS(ON)}$	VB1B–U, VB2–V, VB3–W1	9.5	10.5	11.5	V	
Logic Operation Stop Voltage	$V_{CC(OFF)}$	VCC1–COM, VCC2–COM	10.0	11.0	12.0	V	
	$V_{BS(OFF)}$	VB1B–U, VB2–V, VB3–W1	9.0	10.0	11.0	V	
Logic Supply Current	I_{CC}	VCC1 = VCC2, VCC pin current in 3-phase operation	—	3.2	4.5	mA	
	I_{BS}	VB1B–U, or VB2–V, or VB3–W1; HINx = 5 V; VBx pin current in 1-phase operation	—	140	400	μA	
Input Signal							
High Level Input Threshold Voltage (HINx, LINx, SD, FO)	V_{IH}		—	2.0	2.5	V	
Low Level Input Threshold Voltage (HINx, LINx, SD, FO)	V_{IL}		1.0	1.5	—	V	
High Level Input Current (HINx, LINx)	I_{IH}	V_{IN} = 5 V	—	230	500	μA	
Low Level Input Current (HINx, LINx)	I_{IL}	V_{IN} = 0 V	—	—	2	μA	
Fault Signal Output							
FO Pin Voltage at Fault Signal Output	V_{FOL}	V_{FO} = 5 V, R_{FO} = 10 kΩ	0	—	0.5	V	
FO Pin Voltage in Normal Operation	V_{FOH}	V_{FO} = 5 V, R_{FO} = 10 kΩ	4.8	—	—	V	
Protection							
OCL Pin Output Voltage (L)	$V_{OCL(L)}$		0	—	0.5	V	
OCL Pin Output Voltage (H)	$V_{OCL(H)}$		4.5	—	5.5	V	
Current Limit Reference Voltage	V_{LIM}		0.6175	0.6500	0.6825	V	
Overcurrent Protection Threshold Voltage	V_{TRIP}		0.9	1.0	1.1	V	
Overcurrent Protection Hold Time	t_P		20	25	—	μs	

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Overcurrent Protection Blanking Time	$t_{BK(OCP)}$		—	2	—	µs	
Current Limit Blanking Time	$t_{BK(OCL)}$		—	2	—	µs	
Thermal Shutdown Operating Temperature	T_{DH}		135	150	—	°C	
Thermal Shutdown Releasing Temperature	T_{DL}		105	120	—	°C	

3.2 Bootstrap Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Bootstrap Diode Leakage Current	I_{LBD}	V_R = 500 V	—	—	10	µA	
Bootstrap Diode Forward Voltage	V_{FB}	I_{FB} = 0.15 A	—	1.0	1.3	V	
Bootstrap Diode Series Resistor	R_{BOOT}		45	60	75	Ω	

3.3 Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Junction-to-Case Thermal Resistance(1)	R_{j-C}	All power MOSFETs operating	—	—	3.6	°C/W	SIM681xM
	$R_{(j-C)Q}$(2)	All IGBTs operating	—	—	3.6	°C/W	SIM682xM SIM6880M
	$R_{(j-C)F}$(3)	All freewheeling diodes operating	—	—	4.2	°C/W	SIM682xM SIM6880M
Junction-to-Ambient Thermal Resistance	R_{j-A}	All power MOSFETs operating	—	—	25	°C/W	SIM681xM
	$R_{(j-A)Q}$	All IGBTs operating	—	—	25	°C/W	SIM682xM SIM6880M
	$R_{(j-A)F}$	All freewheeling diodes operating	—	—	29	°C/W	SIM682xM SIM6880M

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(1) Refers to a case temperature at the measurement point described in Figure 3-1, below.

(2) Refers to steady-state thermal resistance between the junction of the built-in transistors and the case. For transient thermal characteristics, see Section 15.1.

(3) Refers to steady-state thermal resistance between the junction of the built-in freewheeling diodes and the case.

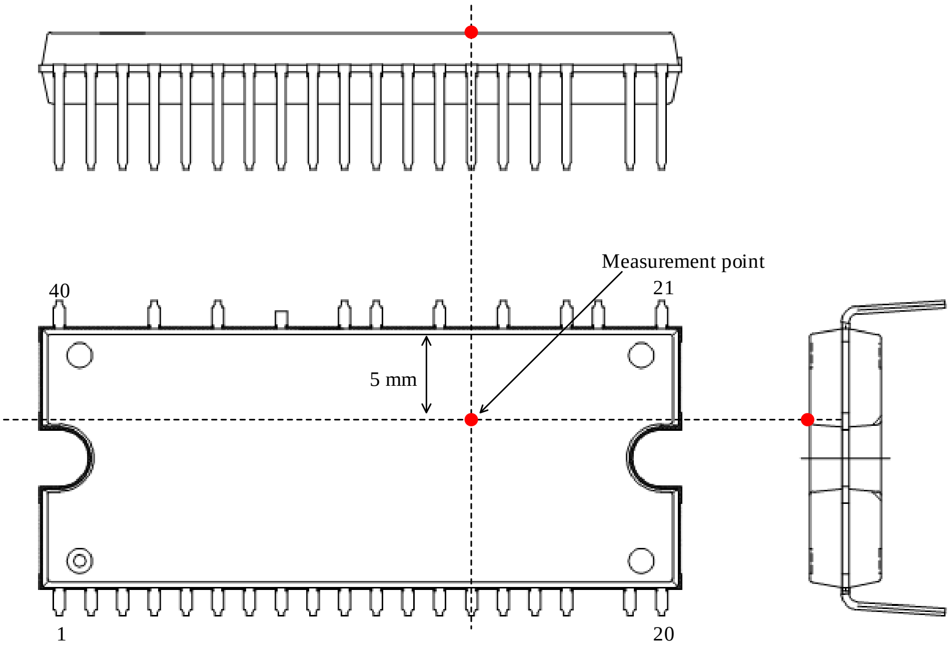


Figure 3-1. Case Temperature Measurement Point

3.4 Transistor Characteristics

Figure 3-2 provides the definitions of switching characteristics described in this and the following sections.

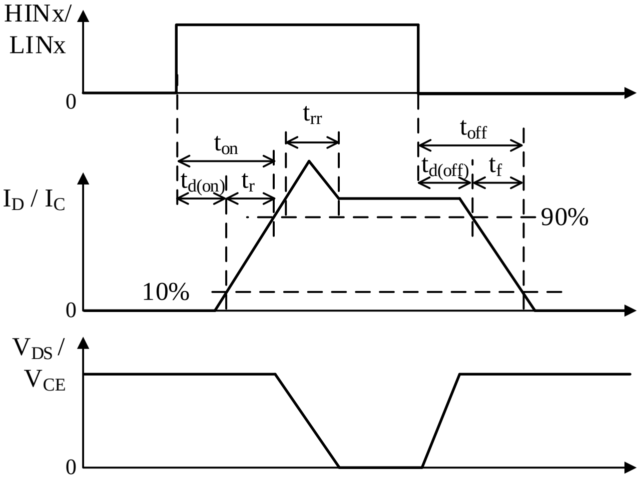


Figure 3-2. Switching Characteristics Definitions

3.4.1 SIM6811M

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 500 V, V_{IN} = 0 V	—	—	100	µA
Drain-to-Source On Resistance	$R_{DS(ON)}$	I_D = 1.0 A, V_{IN} = 5 V	—	3.2	4.0	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} =1.0 A, V_{IN} = 0 V	—	1.0	1.5	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 1.0 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	150	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	770	—	ns
Rise Time	t_r		—	70	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	690	—	ns
Fall Time	t_f		—	30	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 1.0 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	150	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	690	—	ns
Rise Time	t_r		—	90	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	650	—	ns
Fall Time	t_f		—	50	—	ns

3.4.2 SIM6812M

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{CES}	V_{DS} = 500 V, V_{IN} = 0 V	—	—	100	µA
Drain-to-Source On Resistance	$V_{CE(SAT)}$	I_D = 1.25 A, V_{IN} = 5 V	—	2.0	2.4	Ω
Source-to-Drain Diode Forward Voltage	V_F	I_{SD} =1.25 A, V_{IN} = 0 V	—	1.0	1.5	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 1.25 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	140	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	910	—	ns
Rise Time	t_r		—	100	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	700	—	ns
Fall Time	t_f		—	40	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 1.25 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	155	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	875	—	ns
Rise Time	t_r		—	110	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	775	—	ns
Fall Time	t_f		—	35	—	ns

3.4.3 SIM6813M

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 500 V, V_{IN} = 0 V	—	—	100	µA
Drain-to-Source On Resistance	$R_{DS(ON)}$	I_D = 1.5 A, V_{IN} = 5 V	—	1.4	1.7	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} =1.5 A, V_{IN} = 0 V	—	1.0	1.5	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 1.5 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	170	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	820	—	ns
Rise Time	t_r		—	100	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	810	—	ns
Fall Time	t_f		—	50	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 1.5 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	180	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	760	—	ns
Rise Time	t_r		—	130	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	750	—	ns
Fall Time	t_f		—	50	—	ns

3.4.4 SIM6880M

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 300 V, V_{IN} = 0 V	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 2.5 A, V_{IN} = 5 V	—	1.85	2.35	V
Diode Forward Voltage	V_F	I_F = 2.5 A, V_{IN} = 0 V	—	2.0	2.4	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 2.5 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	100	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	880	—	ns
Rise Time	t_r		—	120	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	740	—	ns
Fall Time	t_f		—	210	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 2.5 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	100	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	820	—	ns
Rise Time	t_r		—	140	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	660	—	ns
Fall Time	t_f		—	200	—	ns

3.4.5 SIM6822M

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 5 A, V_{IN} = 5 V	—	1.75	2.2	V
Diode Forward Voltage	V_F	I_F = 5 A, V_{IN} = 0 V	—	2.0	2.4	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 5 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	80	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	740	—	ns
Rise Time	t_r		—	70	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	570	—	ns
Fall Time	t_f		—	100	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 5 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	80	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	690	—	ns
Rise Time	t_r		—	100	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	540	—	ns
Fall Time	t_f		—	100	—	ns

3.4.6 SIM6827M

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 5 A, V_{IN} = 5 V	—	1.75	2.2	V
Diode Forward Voltage	V_F	I_F = 5 A, V_{IN} = 0 V	—	2.0	2.4	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 5 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	100	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	1030	—	ns
Rise Time	t_r		—	180	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	590	—	ns
Fall Time	t_f		—	150	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 5 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25 °C	—	100	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	1030	—	ns
Rise Time	t_r		—	240	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	540	—	ns
Fall Time	t_f		—	150	—	ns

4. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Heatsink Mounting Screw Torque	*	0.294	—	0.441	N·m	
Flatness of Heatsink Attachment Area	See Figure 4-1.	0	—	60	µm	
Package Weight		—	5.2	—	g	

* When mounting a heatsink, it is recommended to use a metric screw of M2.5 and a plain washer of 6.0 mm (φ) together at each end of it. For more details about screw tightening, see Section 13.2.

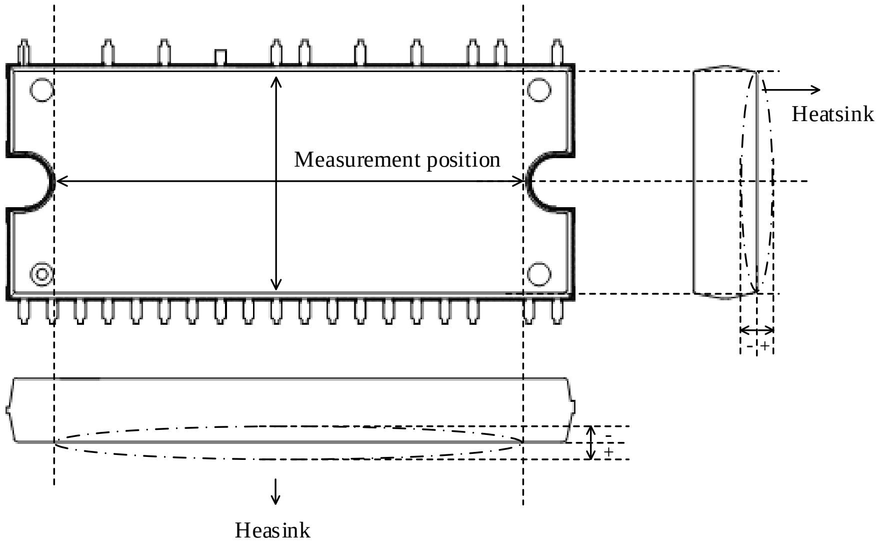


Figure 4-1. Flatness Measurement Position

5. Insulation Distance

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Clearance	Between heatsink* and leads. See Figure 5-1.	1.5	—	2.1	mm	
Creepage		1.7	—	—	mm	

* Refers to when a heatsink to be mounted is flat. If your application requires a clearance exceeding the maximum distance given above, use an alternative (e.g., a convex heatsink) that will meet the target requirement.

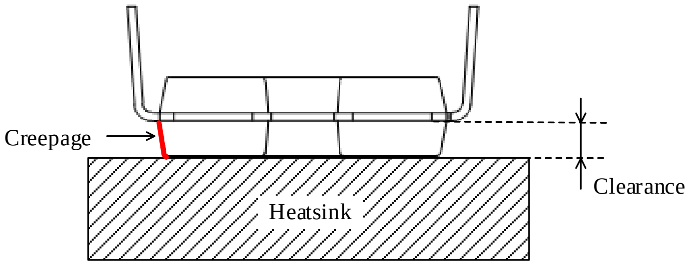


Figure 5-1. Insulation Distance Definitions

6. Truth Table

Table 6-1 is a truth table that provides the logic level definitions of operation modes.

In the case where HINx and LINx signals in each phase are high at the same time, both the high- and low-side transistors become on (simultaneous on-state).

After the IC recovers from a UVLO_VCC condition, the low-side transistors resume switching in accordance with the input logic levels of the LINx signals (level-triggered) whereas the high-side transistors resume switching at the next rising edge of an HINx signal (edge-triggered).

After the IC recovers from a UVLO_VB condition, the high-side transistors resume switching at the next rising edge of an HINx signal (edge-triggered).

Table 6-1. Truth Table for Operation Modes

Mode	HINx	LINx	High-side Transistor	Low-side Transistor
Normal Operation	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	ON
	H	H	ON	ON
External Shutdown Signal Input FO = Low Level	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF
Undervoltage Lockout for High-side Power Supply (UVLO_VB)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	ON
	H	H	OFF	ON
Undervoltage Lockout for Low-side Power Supply (UVLO_VCC)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	OFF
	H	H	OFF	OFF
Overcurrent Protection (OCP)	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF
Overcurrent Limit (OCL) (OCL = SD)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	ON
	H	H	OFF	ON
Thermal Shutdown (TSD)	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF

7. Block Diagrams

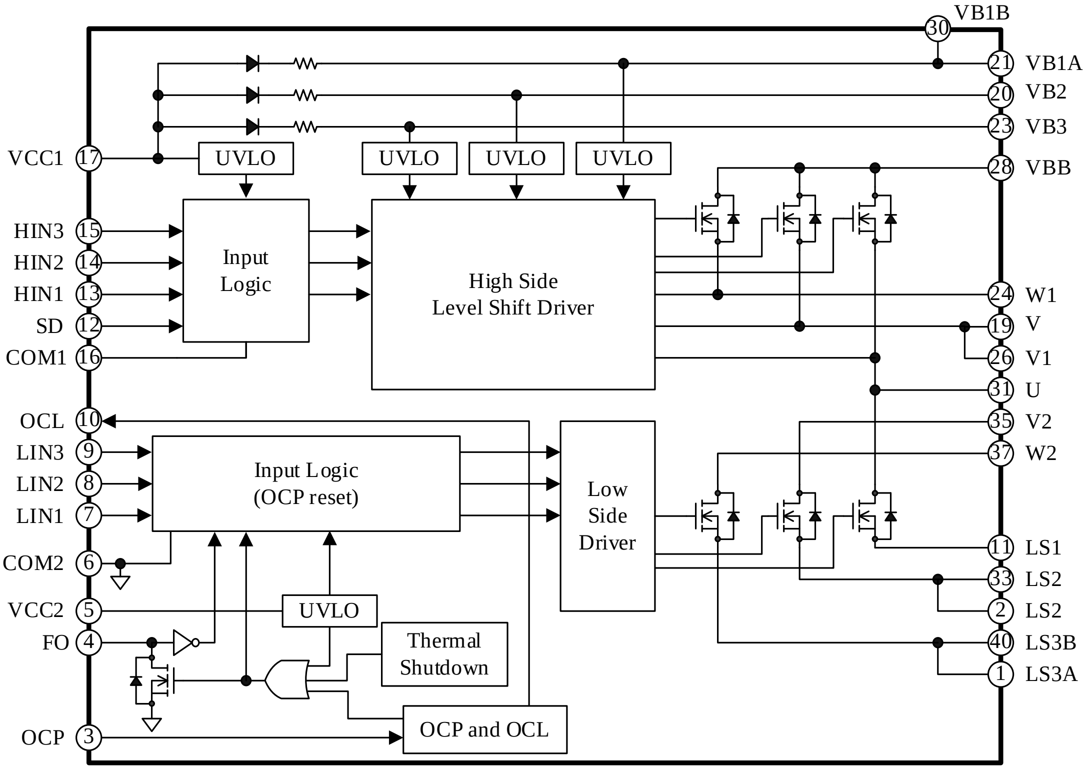


Figure 7-1. SIM681xM

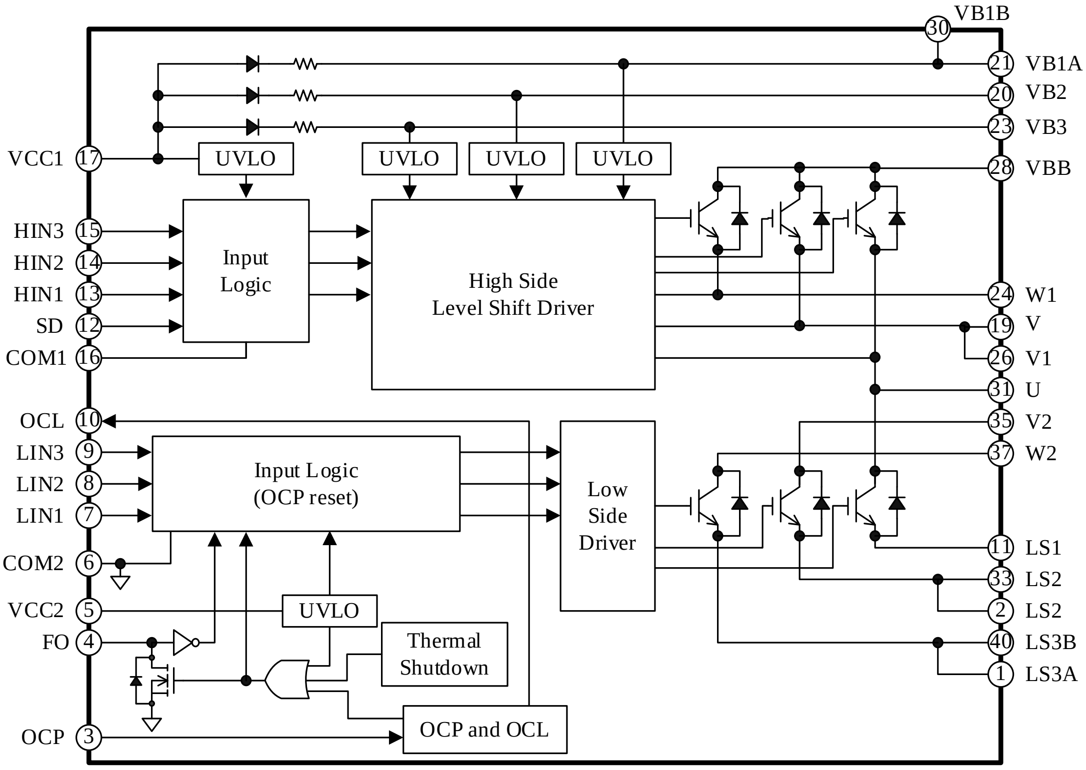
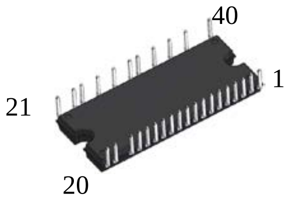
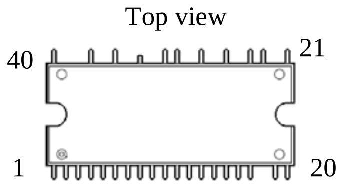


Figure 7-2. SIM682xM or SIM688xM

8. Pin Configuration Definitions





Pin Number	Pin Name	Function
1	LS3A	W-phase IGBT emitter, or power MOSFET source
2	LS2	V-phase IGBT emitter, or power MOSFET source
3	OCP	Overcurrent protection signal input
4	FO	Fault output and shutdown signal input
5	VCC2	Low-side logic supply voltage input
6	COM2	Low-side logic ground
7	LIN1	Logic input for U-phase low-side gate driver
8	LIN2	Logic input for V-phase low-side gate driver
9	LIN3	Logic input for W-phase low-side gate driver
10	OCL	Overcurrent limit signal input
11	LS1	U-phase IGBT emitter, or power MOSFET source
12	SD	High-side shutdown signal input
13	HIN1	Logic input for U-phase high-side gate driver
14	HIN2	Logic input for V-phase high-side gate driver
15	HIN3	Logic input for W-phase high-side gate driver
16	COM1	High-side logic ground
17	VCC1	High-side logic supply voltage input
18	—	(Pin removed)
19	V	V-phase high-side floating supply voltage input, bootstrap capacitor connection for V-phase
20	VB2	V-phase high-side floating supply voltage input
21	VB1A	U-phase high-side floating supply voltage input
22	—	(Pin removed)
23	VB3	W-phase high-side floating supply voltage input
24	W1	W-phase output (connected to W2 externally)
25	NC	(No connection)
26	V1	V-phase output (connected to V2 externally)
27	—	(Pin removed)
28	VBB	Positive DC bus supply voltage
29	NC	(No connection)
30	VB1B	V-phase high-side floating supply voltage input
31	U	U-phase output
32	—	(Pin removed)
33	LS2	(Pin trimmed) V-phase IGBT emitter, or power MOSFET source
34	—	(Pin removed)
35	V2	V-phase output (connected to V1 externally)
36	NC	(No connection)
37	W2	W-phase output (connected to W1 externally)
38	—	(Pin removed)
39	—	(Pin removed)
40	LS3B	W-phase IGBT emitter, or power MOSFET source

9. Typical Applications

CR filters and Zener diodes should be added to your application as needed. This is to protect each pin against surge voltages causing malfunctions, and to avoid the IC being used under the conditions exceeding the absolute maximum ratings where critical damage is inevitable. Then, check all the pins thoroughly under actual operating conditions to ensure that your application works flawlessly.

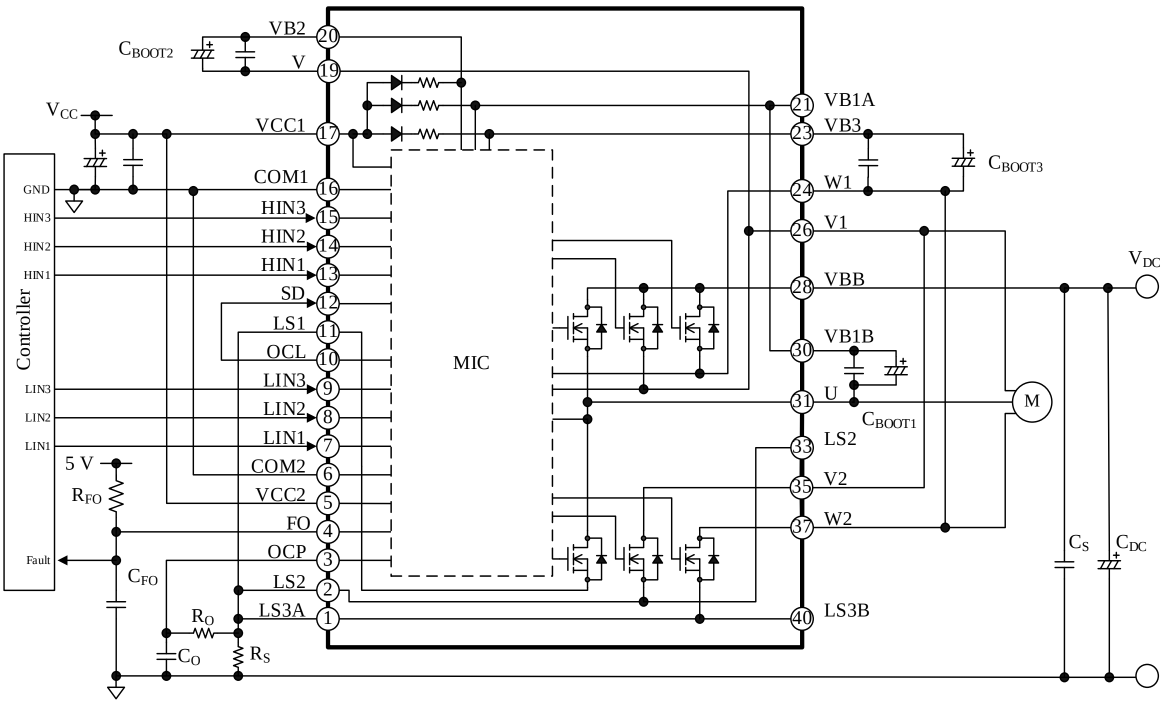


Figure 9-1. SIM681xM Typical Application using a Single Shunt Resistor

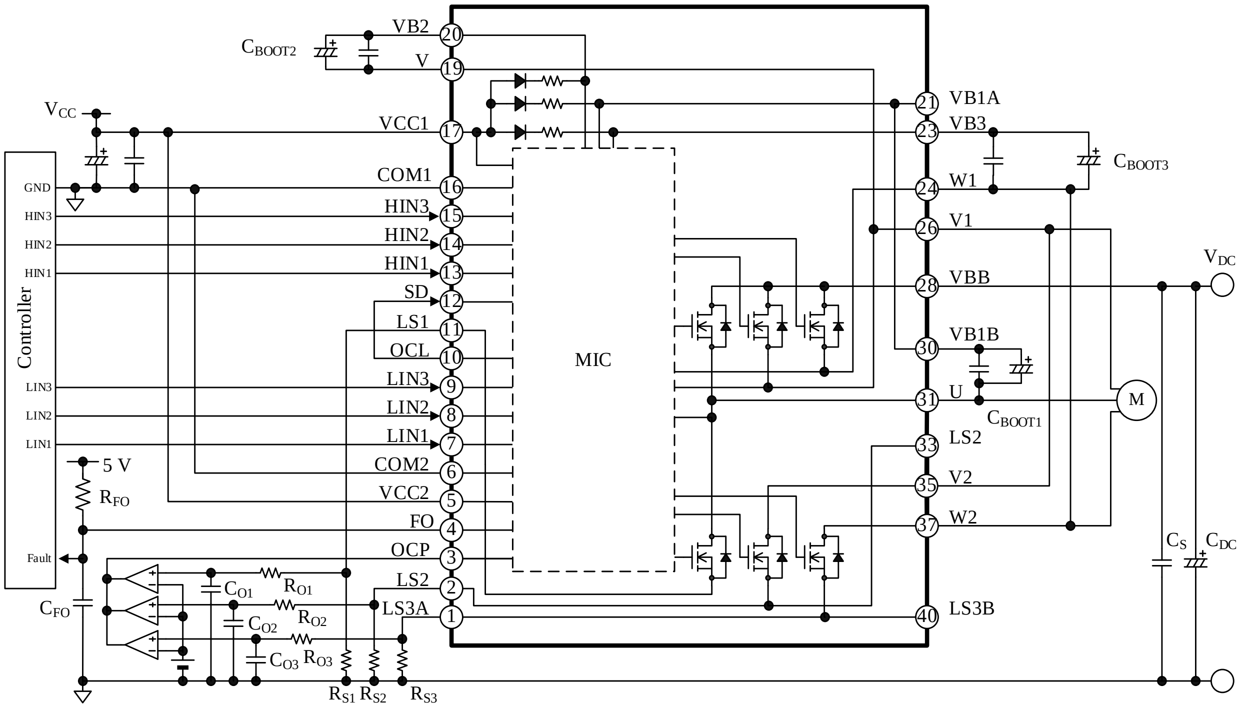
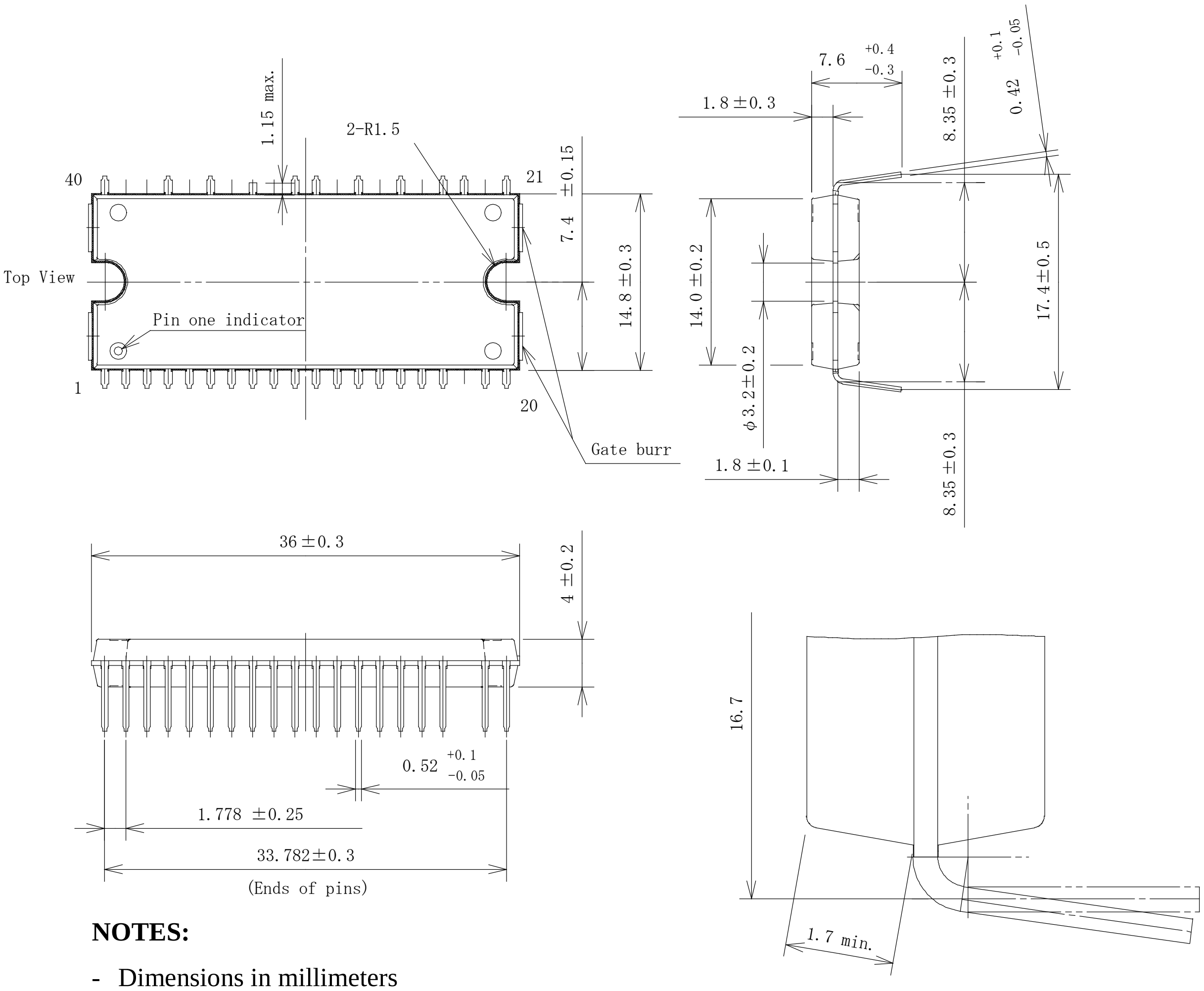


Figure 9-2. SIM681xM Typical Application using Three Shunt Resistors

10. Physical Dimensions

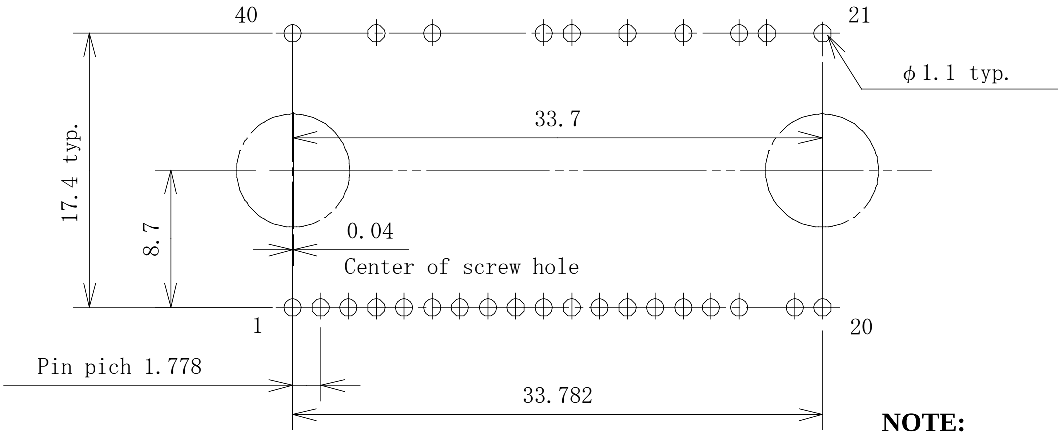
● DIP40 Package



NOTES:

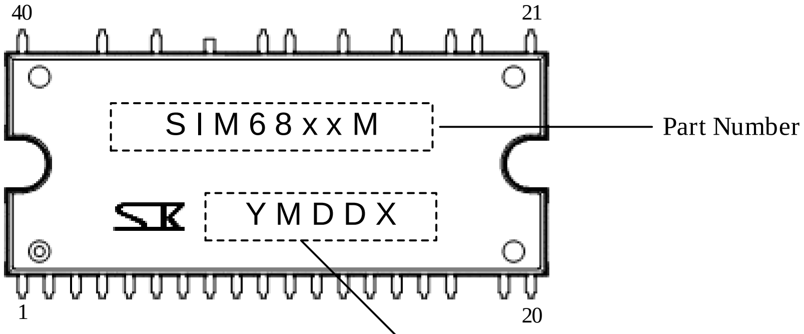
- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)
- The leads illustrated above are for reference only, and may not be actual states of being bent.
- Maximum gate burr height is 0.3 mm.

● Reference Through Hole Size and Layout



NOTE:
Dimensions in millimeters

11. Marking Diagram



Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
DD is the day of the month (01 to 31)
X is the control number

12. Functional Descriptions

Unless specifically noted, this section uses the following definitions:

- All the characteristic values given in this section are typical values.
- All the circuit diagrams listed in this section represent the type of IC including power MOSFETs. All the functional descriptions in this section are also applicable to the type of IC including IGBTs.
- For pin and peripheral component descriptions, this section employs a notation system that denotes a pin name with the arbitrary letter "x", depending on context. Thus, "the VCCx pin" is used when referring to either of the VCC1 or VCC2 pin.
- The COM1 pin is always connected to the COM2 pin.

12.1 Turning On and Off the IC

The procedures listed below provide recommended startup and shutdown sequences. To turn on the IC properly, do not apply any voltage on the VBB, HINx, and LINx pins until the VCCx pin voltage has reached a stable state ($V_{CC(ON)} \geq 12.5$ V).

It is required to charge bootstrap capacitors, C_{BOOTx}, up to full capacity at startup (see Section 12.2.2).

To turn off the IC, set the HINx and LINx pins to logic low (or "L"), and then decrease the VCCx pin voltage.

12.2 Pin Descriptions

12.2.1 U, V, V1, V2, W1, and W2

These pins are the outputs of the three phases, and serve as connection terminals to the 3-phase motor. The V1 and W1 pins must be connected to the V2 and W2 pins on a PCB, respectively.

The U, V (V1) and W1 pins are the grounds for the VB1A (VB1B), VB2, and VB3 pins.

The U, V and W1 pins are connected to the negative nodes of the bootstrap capacitors, C_{BOOTx}. The V pin is internally connected to the V1 pin.

Since high voltages are applied to these output pins (U, V, V1, V2, W1, and W2), it is required to take measures for insulating as to keep enough distance between the traces of follows:

- Keep enough distance between the output pins and low-voltage traces.
- Coat the output pins with insulating resin.

12.2.2 VB1A, VB1B, VB2, and VB3

These pins are connected to bootstrap capacitors for the high-side floating supply.

In actual applications, use either of the VB1A or VB1B pin because they are internally connected. Voltages across the VBx and these output pins should be maintained within the recommended range (i.e., the Logic Supply Voltage, V_{BS}) given in Section 2.

A bootstrap capacitor, C_{BOOTx}, should be connected in each of the traces between the VB1A (VB1B) and U pins, the VB2 and V pins, the VB3 and W1 (W2) pins.

For proper startup, turn on the low-side transistor first, then charge the bootstrap capacitor, C_{BOOTx}, up to its maximum capacity.

For capacitance of the bootstrap capacitors, C_{BOOTx}, choose the values that satisfy Equations (1) and (2). Note that capacitance tolerance and DC bias characteristics must be taken into account when choosing the appropriate values for C_{BOOTx}.

$$C_{BOOTx}\ (\mu F) > 800 \times t_{L(OFF)} \qquad (1)$$

$$1\ \mu F \leq C_{BOOTx} \leq 220\ \mu F \qquad (2)$$

In Equation (1), let $t_{L(OFF)}$ be the maximum off-time of the low-side transistor (i.e., the non-charging time of C_{BOOTx}), measured in seconds.

Even during the high-side transistor is not on, voltage across the bootstrap capacitor keeps decreasing due to power dissipation in the IC. When the VBx pin voltage decreases to $V_{BS(OFF)}$ or less, the high-side undervoltage lockout (UVLO_VB) starts operating (see Section 12.3.3.1). Therefore, actual board checking should be done thoroughly to validate that voltage across the VBx pin maintains over 11.0 V ($V_{BS} > V_{BS(OFF)}$) during a low-frequency operation such as a startup period.

As Figure 12-1 shows, in each trace between the VCC1 and VBx pins, a bootstrap diode, D_{BOOTx}, and a current-limiting resistor, R_{BOOTx}, are placed in series.

Time constant for the charging time of C_{BOOTx}, τ, can be computed by Equation (3):

$$\tau = C_{BOOTx} \times R_{BOOTx}\ , \qquad (3)$$

where C_{BOOTx} is the optimized capacitance of the bootstrap capacitor, and R_{BOOTx} is the resistance of the current-limiting resistor (60 Ω ± 25%).

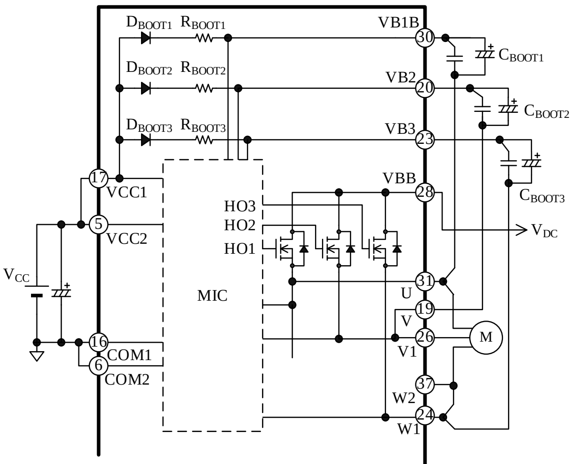


Figure 12-1. Bootstrap Circuit

Figure 12-2 shows an internal level-shifting circuit that produces high-side output signals, HOx.

A high-side output signal, HOx, is generated according to an input signal on the HINx pin. When an input signal on the HINx pin transits from low to high (rising edge), a “Set” signal is generated. When the HINx input signal transits from high to low (falling edge), a “Reset” signal is generated. These two signals are then transmitted to the high-side by the level-shifting circuit and are input to the SR flip-flop circuit. Finally, the SR flip-flop circuit feeds an output signal, Q (i.e., HOx).

Figure 12-3 is a timing diagram describing how noise or other detrimental effects will improperly influence the level-shifting process. When a noise-induced rapid voltage drop between the VBx and output pins (U, V or W1; hereafter “VBx–HSx”) occurs after the Set signal generation, the next Reset signal cannot be sent to the SR flip-flop circuit. And the state of the high-side output, HOx, stays logic high (or “H”) because the SR flip-flop does not respond. With the HOx state being held high, the next LINx signal turns on the low-side transistor and causes a simultaneously-on condition which may result in critical damage to the IC. To protect the VBx pin against such noise effect, add a bootstrap capacitor, C_{BOOTx}, in each phase. C_{BOOTx} must be placed near the IC and connected between the VBx and HSx pins with a minimal length of traces. To use an electrolytic capacitor, add a 0.01 µF to 0.1 µF bypass capacitor, C_P, in parallel near these pins used for the same phase.

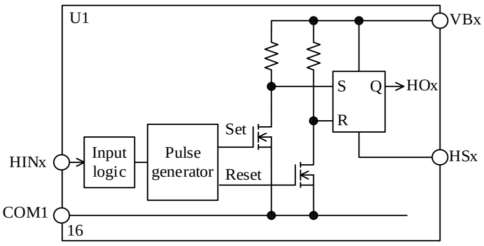


Figure 12-2. Internal Level-shifting Circuit

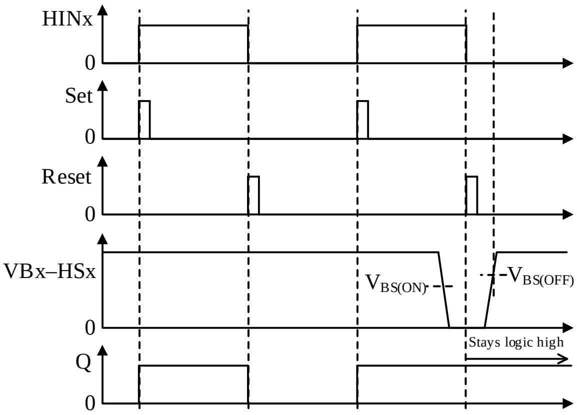


Figure 12-3. Waveforms at VBx–HSx Voltage Drop

12.2.3 VCC1 and VCC2

These are the power supply pins for the built-in control IC. The VCC1 and VCC2 pins must be externally connected on a PCB because they are not internally connected. To prevent malfunction induced by supply ripples or other factors, put a 0.01 µF to 0.1 µF ceramic capacitor, C_{VCC}, near these pins. To prevent damage caused by surge voltages, put a 18 V to 20 V Zener diode, DZ, between the VCCx and COMx pins.

Voltage to be applied between the VCCx and COMx pins should be regulated within the recommended operational range of V_{CC}, given in Section 2.

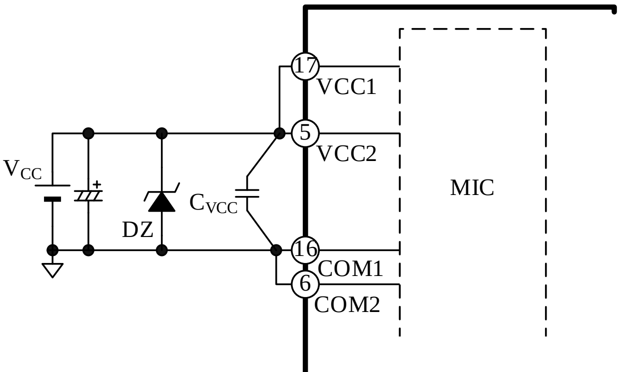


Figure 12-4. The VCCx Pin Peripheral Circuit

12.2.4 COM1 and COM2

These are the logic ground pins for the built-in control IC. The COM1 and COM2 pins should be connected externally on a PCB because they are not internally connected.

Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect these pins as close and short as possible to shunt resistors, R_{Sx}, at a single-point ground (or star ground) which is separated from the power ground (see Figure 12-5).

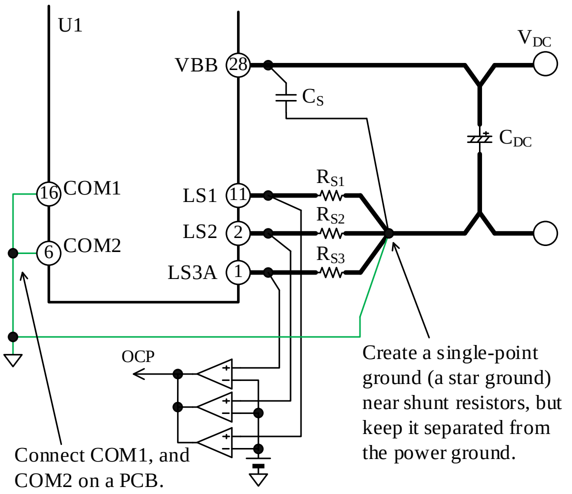


Figure 12-5. Connections to Logic Ground

12.2.5 HIN1, HIN2, HIN3, LIN1, LIN2, and LIN3

These are the input pins of the internal motor drivers for each phase. The HINx pin acts as a high-side controller whereas the LINx pin acts as a low-side controller.

Figure 12-6 shows an internal circuit diagram of the HINx or LINx pin. This is a CMOS Schmitt trigger circuit with 20 kΩ pull-down resistor, and its input logic is active high.

Input signals across the HINx–COMx and the LINx–COMx pins in each phase should be set within the ranges provided in Table 12-1, below. Note that dead time setting must be done for HINx and LINx signals because the IC does not have a dead time generator.

The higher PWM carrier frequency rises, the more switching loss increases. Hence, the PWM carrier frequency must be set so that operational case temperatures and junction temperatures can have sufficient margins in the absolute maximum ranges specified in Section 1.

If the signals from the microcontroller become unstable, the IC may result in malfunctions. To avoid this event, the outputs from the microcontroller output line should not be high impedance.

Also, if the traces from the microcontroller to the HINx or LINx pins (or both) are too long, the traces may be interfered by noise. Therefore, it is recommended to add an additional filter or a pull-down resistor near the the HINx or LINx pin as needed (see Figure 12-7).

Here are filter circuit constants for reference:

- R_{IN1x}: 33 Ω to 100 Ω
- R_{INx}: 1 kΩ to 10 kΩ
- C_{INx}: 100 pF to 1000 pF

Extra attention should be paid when adding R_{IN1x} and R_{IN2x} to the traces. When they are connected each other, the input voltage of the HINx and LINx pins becomes slightly lower than the output voltage of the microcontroller.

Table 12-1. Input Signals for HINx and LINx Pins

Parameter	High Level Signal	Low Level Signal
Input Voltage	$3\text{ V} < V_{IN} < 5.5\text{ V}$	$0\text{ V} < V_{IN} < 0.5\text{ V}$
Input Pulse Width	≥0.5 μs	≥0.5 μs
PWM Carrier Frequency	≤20 kHz	
Dead Time	≥1.5 μs	

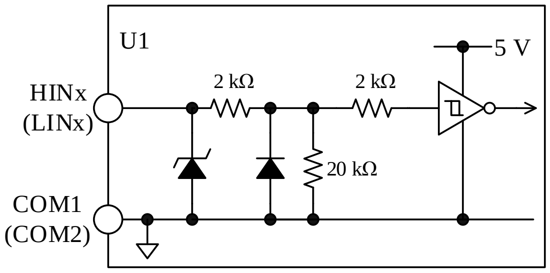


Figure 12-6. Internal Circuit Diagram of HINx or LINx Pin

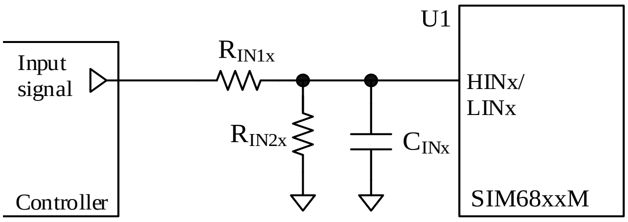


Figure 12-7. Filter Circuit for HINx or LINx Pin

12.2.6 VBB

This is the input pin for the main supply voltage, i.e., the positive DC bus. All of the IGBT collectors (power MOSFET drains) of the high-side are connected to this pin. Voltages between the VBB and COMx pins should be set within the recommended range of the main supply voltage, V_{DC}, given in Section 2.

To suppress surge voltages, put a 0.01 μF to 0.1 μF bypass capacitor, C_S, near the VBB pin and an electrolytic capacitor, C_{DC}, with a minimal length of PCB traces to the VBB pin.

12.2.7 LS1, LS2, LS3A, and LS3B

These are the emitter (source) pins of the low-side IGBTs (power MOSFETs). For current detection, the LS1, LS2, and LS3 (LS3B) pins should be connected externally on a PCB via shunt resistors, R_{Sx}, to the COMx pin. In actual applications, use either of the LS3A or LS3B pin because they are internally connected.

When connecting a shunt resistor, place it as near as possible to the IC with a minimum length of traces to the LSx and COMx pins. Otherwise, malfunction may occur because a longer circuit trace increases its inductance and thus increases its susceptibility to improper operations. In applications where long PCB traces are required, add a fast recovery diode, D_{RSx}, between the LSx and COMx pins in order to prevent the IC from malfunctioning.

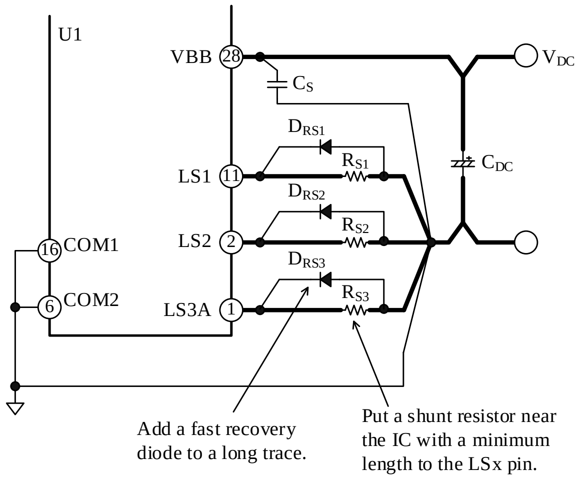


Figure 12-8. Connections to LSx Pin

12.2.8 OCP and OCL

The OCP pin serves as the input for the overcurrent protections which monitor the currents going through output transistors.

In normal operation, the OCL pin logic level is low. In case one or more of the protections listed below are activated by an OCP input signal, the OCL pin logic level becomes high. When the OCL pin is connected to the SD pin so that the SD pin responds to the OCL input signal, the high-side transistors turn off during the protections (OCP and OCL) are activated.

- **Overcurrent Limit (OCL)**

When the OCP pin voltage exceeds the reference voltage, V_{LIM}, the OCL pin logic level becomes high. During the OCL is in working, the output transistors operate according to an input signal (HINx or LINx). If the OCL pin is connected to the SD pin, the high-side transistors can be turned off. For a more detailed OCL description, see Section 12.3.4.

- **Overcurrent Pprotection (OCP)**

This function detects inrush currents larger than those detected by the OCL. When the OCP pin voltage exceeds the threshold voltage, V_{TRIP}, the IC operates as follows: the OCL pin = logic high, the low-side transistors = off, the FO pin = logic low.

In addition, if the OCL pin is connected to the SD pin, the high-side transistors can be turned off. For a more detailed OCP description, see Section 12.3.5.

12.2.9 SD

When a 5 V or 3.3 V signal is input to the SD pin, the high-side transistors turn off independently of any HINx signals. This is because the SD pin does not respond to a pulse shorter than the internal filter of 3.3 μs (typ.).

The SD-OCL pin connection, therefore, allows the IC to turn off the high-side transistors at OCL or OCP activation. In addition, by connecting the FO and SD pins, all the high- and low-side transistors turn off due to an inverting signal from the FO pin, even if the IC falls into an abnormal condition in which some or all of the protections (TSD, OCP, and UVLO) are activated.

12.2.10 FO

This pin operates as a fault output and a low-side shutdown input. Sections 12.3.1 and 12.3.2 explain these two functions in detail, respectively. Figure 12-9 illustrates a schematic diagram of the FO pin and its peripheral circuit.

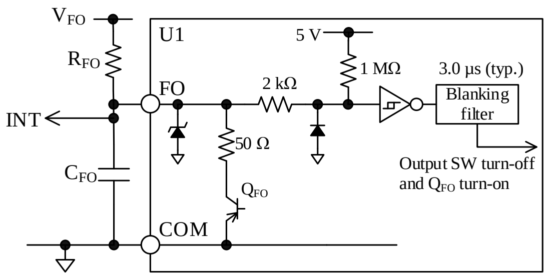


Figure 12-9. Internal Circuit Diagram of FO Pin and Its Peripheral Circuit

Because of its open-collector nature, the FO pin should be tied by a pull-up resistor, R_{FO}, to the external power supply. The external power supply voltage, V_{FO}, should range from 3.0 V to 5.5 V. When the pull-up resistor, R_{FO}, has a too small resistance, the FO pin voltage at fault output becomes high due to the saturation voltage drop of a built-in transistor, Q_{FO}. Therefore, it is recommended to use a 3.3 kΩ to 10 kΩ pull-up resistor. To suppress noise, add a filter capacitor, C_{FO}, near the IC with minimizing a trace length between the FO and COMx pins.

To avoid the repetition of the Overcurrent Protection

(OCP) activations, the external microcontroller must shut off any input signals to the IC within an OCP hold time, t_P, which occurs after the internal transistor (Q_{FO}) turn-on. t_P is 15 μs where minimum values of thermal characteristics are taken into account. (For more details, see Section 12.3.5.) Our recommendation is to use a 0.001 μF to 0.01 μF filter capacitor.

12.3 Protection Functions

This section describes the various protection circuits provided in the SIM6800M series. The protection circuits include: the Undervoltage Lockout for power supplies (UVLO), the Overcurrent Protection (OCP), and the Thermal Shutdown (TSD). In case one or more of these protection circuits are activated, the FO pin outputs a fault signal; as a result, the external microcontroller can stop all operations of the three phases by receiving the fault signal. The external microcontroller can also shut down the IC operations by inputting a fault signal to the FO pin.

In the following functional descriptions, “HOx” denotes a gate input signal on the high-side transistor whereas “LOx” denotes a gate input signal on the low-side transistor. “VBx–HSx” refers to the voltages between the VBx pin and output pins (U, V, and W1).

12.3.1 Fault Signal Output

In case one or more of the following protections are actuated, an internal transistor, Q_{FO}, turns on; then the FO pin logic level becomes low (≤0.5 V).

1) Low-side Undervoltage Lockout (UVLO_VCC)
2) Overcurrent Protection (OCP)
3) Thermal Shutdown (TSD)

During the time when the FO pin holds the logic low state, all the low-side transistors turn off. In normal operation, the FO pin holds a high state and outputs a 5 V signal. The fault signal output time of the FO pin at OCP activation is the OCP hold time (t_P) of 25 μs (typ.), fixed by a built-in feature of the IC itself (see Section 12.3.5). The fault signals are then sent to an interrupt pin (INT) of the external microcontroller, and should be processed as an interrupt task to be done within the predetermined OCP hold time, t_P.

12.3.2 Shutdown Signal Input

The FO pin is the input pin of shutdown signals. When the FO pin logic level becomes low, all the low-side transistors turn off.

The voltages and pulse widths of the shutdown signals to be applied between the FO and COMx pins are listed in Table 12-2.

Table 12-2. Shutdown Signals

Parameter	High Level Signal	Low Level Signal
Input Voltage	3 V < V_{IN} < 5.5 V	0 V < V_{IN} < 0.5 V
Input Pulse Width	—	≥6 μs

12.3.3 Undervoltage Lockout for Power Supply (UVLO)

In case the gate-driving voltage of output transistors decreases, the steady-state power dissipation of the transistors increases. This overheating condition may cause permanent damage to the IC in the worst case. To prevent this event, the SIM6800M series has the Undervoltage Lockout (UVLO) circuits for both of the high- and low-side power supplies in the controller IC (MIC).

12.3.3.1. Undervoltage Lockout for High-side Power Supply (UVLO_VB)

Figure 12-10 shows operational waveforms of the undervoltage lockout operation for high-side power supply (i.e., UVLO_VB).

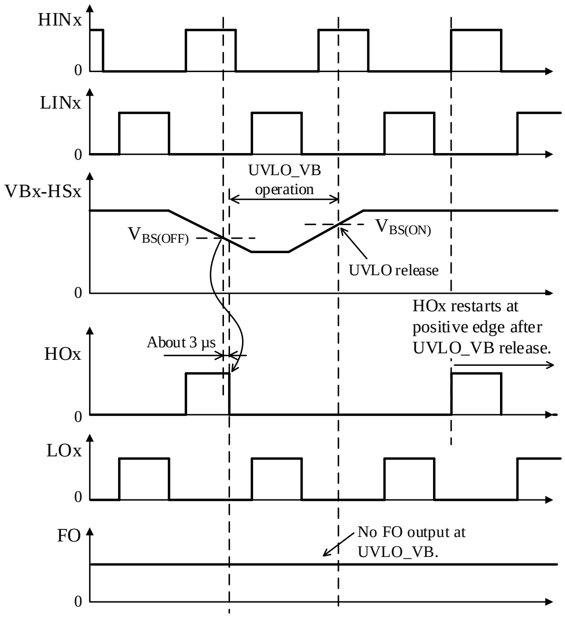


Figure 12-10. Operational Waveforms of UVLO_VB

When the voltage between the VBx and output pins (VBx–HSx) decreases to the Logic Operation Stop Voltage ($V_{BS(OFF)}$, 10.0 V) or less, the UVLO_VB circuit in the corresponding phase activates and sets only HOx signals to logic low. When the voltage between the VBx and HSx pins increases to the Logic Operation Start Voltage ($V_{BS(ON)}$, 10.5 V) or more, the IC releases the UVLO_VB condition. Then, the HOx logic level becomes high at the rising edge of the first input command after the UVLO_VB release. The FO pin does not transmit any fault signals during the UVLO_VB is in operation. In addition, the VBx pin has an internal UVLO_VB filter of about 3 µs, in order to prevent noise-induced malfunctions.

12.3.3.2. Undervoltage Lockout for Low-side Power Supply (UVLO_VCC)

Figure 12-11 shows operational waveforms of the undervoltage lockout operation for low-side power supply (i.e., UVLO_VCC).

When the VCC2 pin voltage decreases to the Logic Operation Stop Voltage ($V_{CC(OFF)}$, 11.0 V) or less, the UVLO_VCC circuit in the corresponding phase activates and sets both of HOx and LOx logic levels to low.

When the VCC pin voltage increases to the Logic Operation Start Voltage ($V_{CC(ON)}$, 11.5 V) or more, the IC releases the UVLO_VCC condition. Then, the IC resumes the transmissions of: LOx signals according to the LINx pin input commands; HOx signals according to the rising edges of the first HINx pin input commands after the UVLO_VCC release.

During the UVLO_VCC operation, the FO pin logic becomes low and sends fault signals.

In addition, the VCC2 pin has an internal UVLO_VCC filter of about 3 µs, in order to prevent noise-induced malfunctions.

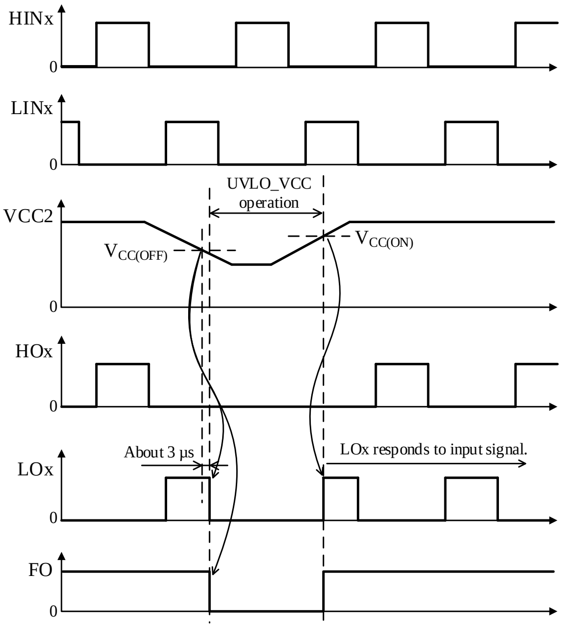


Figure 12-11. Operational Waveforms of UVLO_VCC

12.3.4 Overcurrent Limit (OCL)

The Overcurrent Limit (OCL) is a protection against relatively low overcurrent conditions. Figure 12-12 shows the internal circuit of the OCP and OCL pins; Figure 12-13 shows OCL operational waveforms.

When the OCP pin voltage increases to the Current Limit Reference Voltage (V_{LIM}, 0.6500 V) or more, and remains in this condition for a period of the Current Limit Blanking Time ($t_{BK(OCP)}$, 2 µs), the OCL operation starts. Then the OCL pin goes logic high.

During the OCL operation, the gate logic levels of the low-side transistors respond to the input commands on the LINx pins. By connecting the OCL and SD pins on a PCB, the high-side transistors turn off even during the OCL operation. The SD pin has an internal filter of about 3.3 µs (typ.).

When the OCP pin voltage falls below V_{LIM} (0.6500 V), the OCL pin logic level becomes low. After the OCL pin logic has become low, the high-side transistors remain turned off until the first low-to-high transition on an HINx input signal occurs (i.e., rising edge triggering).

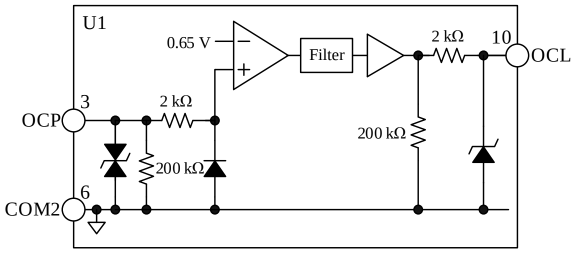


Figure 12-12. Internal Circuit of OCP and OCL Pins

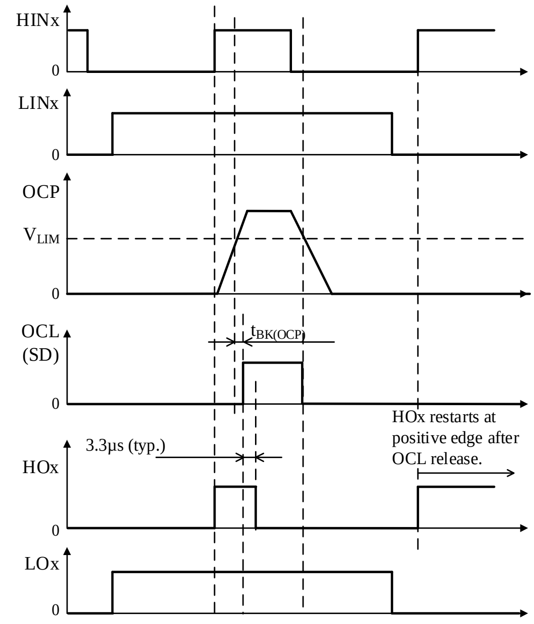


Figure 12-13. OCL Operational Waveforms (OCL = SD)

12.3.5 Overcurrent Protection (OCP)

The Overcurrent Protection (OCP) is a protection against large inrush currents (i.e., high di/dt). Figure 12-14 is an internal circuit diagram describing the OCP pin and its peripheral circuit.

The OCP pin detects overcurrents with input voltage across external shunt resistors, R_{Sx}. Because the OCP pin is internally pulled down, the OCP pin voltage increases proportionally to a rise in the currents running through the shunt resistors, R_{Sx}.

Figure 12-15 is a timing chart that represents operation waveforms during OCP operation. When the OCP pin voltage increases to the Overcurrent Protection Threshold Voltage (V_{TRIP}, 1.0 V) or more, and remains in this condition for a period of the Overcurrent Protection Blanking Time (t_{BK}, 2 µs) or longer, the OCP operation starts. The enabled OCP circuit then shuts off the low-side transistors and puts the FO pin logic level into low. And output current decreases after the output transistors turn off. Even if the OCP pin voltage falls below V_{TRIP}, the IC keeps the FO pin logic level in low for a fixed OCP hold time (t_P) of 25 µs. Then, the output transistors operate according to input signals.

The OCP is used for detecting abnormal conditions, such as an output transistor shorted. In case short-circuit conditions occur repeatedly, the output transistors can be destroyed. To prevent such event, motor operation must be controlled by the external microcontroller so that it can immediately stop the motor when fault signals are detected.

For proper shunt resistor setting, your application must meet the following:

- Use the shunt resistor that has a recommended resistance, R_{Sx} (see Section 2).
- Set the OCP pin input voltage to vary within the rated OCP pin voltages, V_{OCP} (see Section 1).
- Keep the current through the output transistors below the rated output current (pulse), I_{OP} (see Section 1).

It is required to use a resistor with low internal inductance because high-frequency switching current will flow through the shunt resistors, R_{Sx}. In addition, choose a resistor with allowable power dissipation according to your application.

When you connect a CR filter (i.e., a pair of a filter resistor, R_O and a filter capacitor, C_O) to the OCP pin, care should be taken in setting the time constants of R_O and C_O. The larger the time constant, the longer the time that the OCP pin voltage rises to V_{TRIP}. And this may cause permanent damage to the transistors. Consequently, a propagation delay of the IC must be taken into account when you determine the time constants. For R_O and C_O, their time constants should be set to the values listed in Table 12-3. And place C_O as close as possible to the IC with minimizing a trace length between the OCP and COMx pins.

Note that overcurrents are undetectable when one or more of the U, V/V1/V2, and W1/W2 pins or these traces are shorted to ground (ground fault). In case either of these pins falls into a state of ground fault, the output transistors may be destroyed.

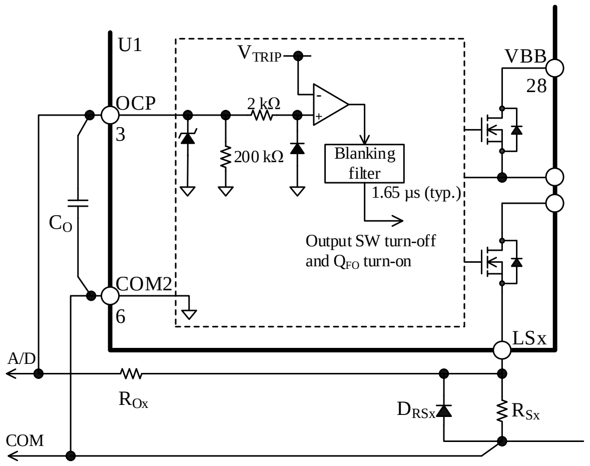


Figure 12-14. Internal Circuit Diagram of OCP Pin and Its Peripheral Circuit

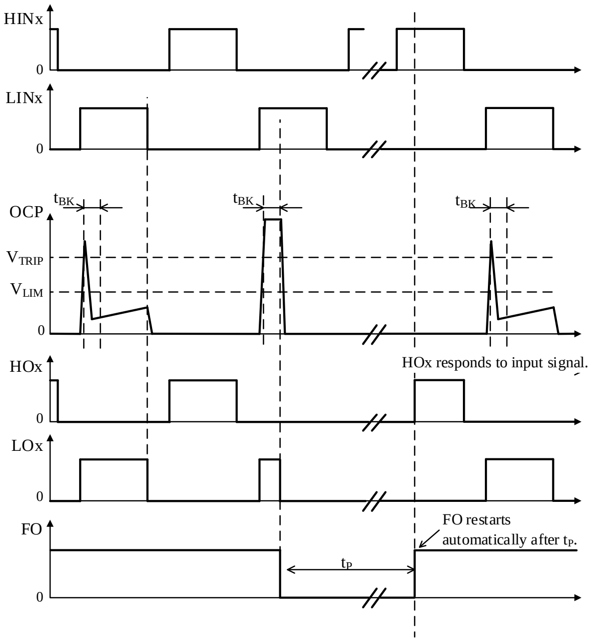


Figure 12-15. OCP Operational Waveforms

Table 12-3. Reference Time Constants for CR Filter

Part Number	Time Constant
SIM681x	≤2 µs
SIM682x SIM688x	≤0.2 µs

12.3.6 Thermal Shutdown (TSD)

The SIM6800M series incorporates the Thermal Shutdown (TSD) circuit in each phase. Figure 12-16 shows TSD operational waveforms. In case of overheating (e.g., increased power dissipation due to overload, a rise in ambient temperature at the device, etc.), the IC shuts down the low-side output transistors.

The TSD circuit in the monolithic IC (MIC) monitors temperatures (see Section 7). When the temperature of the monolithic IC (MIC) exceeds the Thermal Shutdown Operating Temperature, T_{DH}, of 150 °C, the corresponding TSD circuit is activated.

When the temperature decreases to the Thermal Shutdown Releasing Temperature, T_{DL}, of 120 °C or less, the shut-down condition is released. And then the output transistors resume operating according to input signals.

During the TSD operation, the FO pin becomes logic low and transmits fault signals.

Note that junction temperatures of the output transistors themselves are not monitored; therefore, do not use the TSD function as an overtemperature prevention for the output transistors.

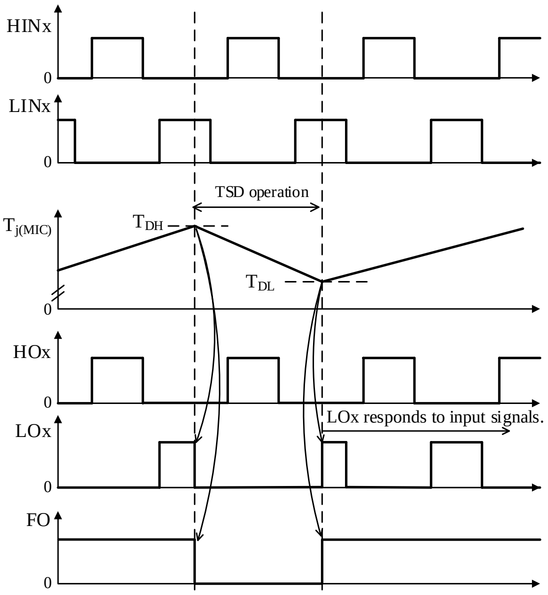


Figure 12-16. TSD Operational Waveforms

13. Design Notes

13.1 PCB Pattern Layout

Figure 13-1 shows a schematic diagram of a motor driver circuit. The motor driver circuit consists of current paths carrying high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing.

Current loops, which carry high frequencies and high voltages, should be as small and wide as possible, in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

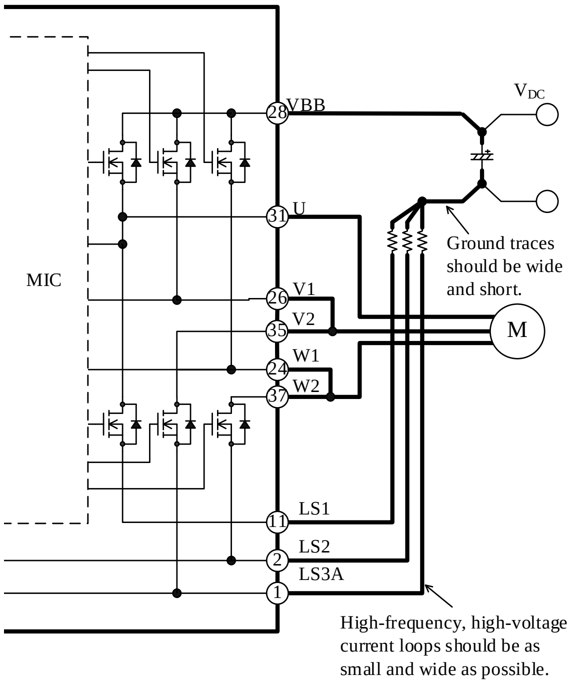


Figure 13-1. High-frequency, High-voltage Current Paths

13.2 Considerations in Heatsink Mounting

The following are the key considerations and the guidelines for mounting a heatsink:

- It is recommended to use a pair of a metric screw of M2.5 and a plain washer of 6.0 mm (φ). To tighten the screws, use a torque screwdriver. Tighten the two screws firstly up to about 30% of the maximum screw torque, then finally up to 100% of the prescribed maximum screw torque. Perform appropriate tightening within the range of screw torque defined in Section 4.

- When mounting a heatsink, it is recommended to use silicone greases. If a thermally-conductive sheet or an electrically insulating sheet is used, package cracks may be occured due to creases at screw tightening. Therefore, thorough evaluations should be conducted before using these materials.
- When applying a silicone grease, make sure that there must be no foreign substances between the IC and a heatsink. Extreme care should be taken not to apply a silicone grease onto any device pins as much as possible.

13.3 Considerations in IC Characteristics Measurement

When measuring the breakdown voltage or leakage current of the transistors incorporated in the IC, note that the gate and emitter (source) of each transistor should have the same potential. Moreover, care should be taken because each transistor is connected as follows:

- All the high-side collectors (drains) are internally connected to the VBB pin.
- In the U phase, the high-side emitter (source) and the low-side collector (drain) are internally connected, and are also connected to the U pin.
  (In the V and W phases, the high- and low-side transistors are unconnected inside the IC.)

The gates of the high-side transistors are pulled down to the corresponding output (U, V/V1, and W1) pins; similarly, the gates of the low-side transistors are pulled down to the COM2 pin.

When measuring the breakdown voltage or leakage current of the transistors, note that all of the output (U, V/V1, and W1), LSx, and COMx pins must be appropriately connected. Otherwise the switching transistors may result in permanent damage.

The following are circuit diagrams representing typical measurement circuits for breakdown voltage: Figure 13-2 shows the high-side transistor (Q_{1H}) in the U phase whereas Figure 13-3 shows the low-side transistor (Q_{1L}) in the U phase. And all the pins that are not represented in these figures are open.

When measuring the high-side transistors, leave all the pins not be measured open. When measuring the low-side transistors, connect the LSx pin to be measured to the COMx pin, then leave other unused pins open.

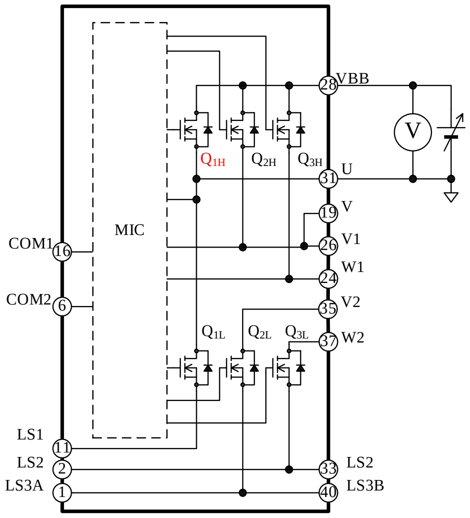


Figure 13-2. Typical Measurement Circuit for High-side Transistor (Q_{1H}) in U Phase

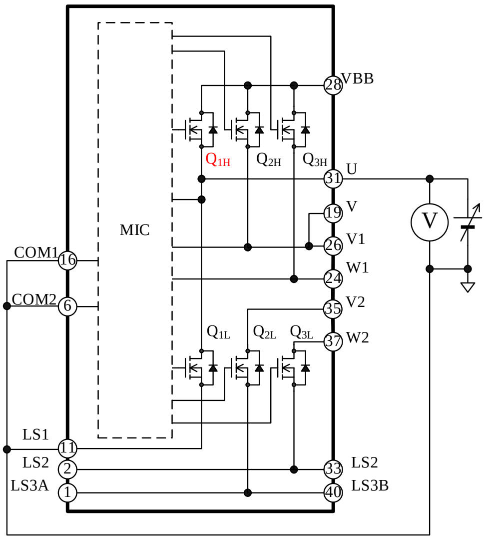


Figure 13-3. Typical Measurement Circuit for Low-side Transistor (Q_{1L}) in U Phase

14. Calculating Power Losses and Estimating Junction Temperatures

This section describes the procedures to calculate power losses in switching transistors, and to estimate junction temperatures. Note that the descriptions listed here are applicable to the SIM6800M series, which is controlled by a 3-phase sine-wave PWM driving strategy.

For quick and easy references, we offer calculation support tools online. Please visit our website to find out more.

- DT0026: SIM682xM Calculation Tool
  http://www.semicon.sanken-ele.co.jp/en/calc-tool/sim682xm_caltool_en.html
- DT0027: SIM681xM Calculation Tool
  http://www.semicon.sanken-ele.co.jp/en/calc-tool/sim681xm_caltool_en.html
- DT0030: SIM688xM Calculation Tool
  http://www.semicon.sanken-ele.co.jp/en/calc-tool/sim688xm_caltool_en.html

14.1 IGBT

Total power loss in an IGBT can be obtained by taking the sum of steady-state loss, P_{ON}, and switching loss, P_{SW}. The following subsections contain the mathematical procedures to calculate these losses (P_{ON} and P_{SW}) and the junction temperature under all-IGBT operation.

14.1.1 IGBT Steady-state Loss, P_{ON}

Steady-state loss in an IGBT can be computed by using the $V_{CE(SAT)}$ vs. I_C curves, listed in Section 15.3.1. As expressed by the curves in Figure 14-1, linear approximations at a range the I_C is actually used are obtained by: $V_{CE(SAT)} = \alpha \times I_C + \beta$. The values gained by the above calculation are then applied as parameters in Equation (4), below. Hence, the equation to obtain the IGBT steady-state loss, P_{ON}, is:

$$P_{ON} = \frac{1}{2\pi}\int_0^{\pi} V_{CE(SAT)}\,(\varphi) \times I_C(\varphi) \times DT \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2}+\frac{4}{3\pi}M \times \cos\theta\right){I_M}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2}+\frac{\pi}{8}M \times \cos\theta\right)I_M\,. \qquad (4)$$

Where:

$V_{CE(SAT)}$ is the collector-to-emitter saturation voltage of the IGBT in V,

I_C is the collector current of the IGBT in A,

DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2}\qquad ,$$

M is the modulation index (0 to 1),

cosθ is the motor power factor (0 to 1),

I_M is the effective motor current in A,

α is the slope of the linear approximation in the $V_{CE(SAT)}$ vs. I_C curve, and

β is the intercept of the linear approximation in the $V_{CE(SAT)}$ vs. I_C curve.

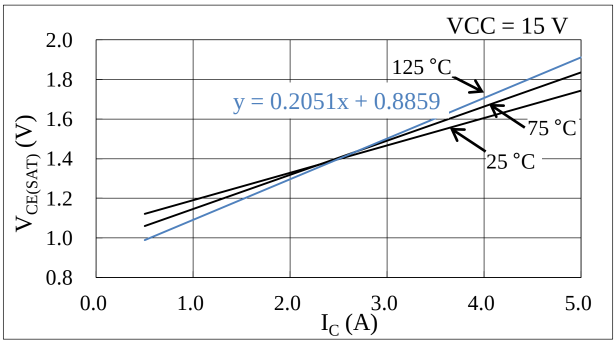


Figure 14-1. Linear Approximate Equation of $V_{CE(SAT)}$ vs. I_C Curve

14.1.2 IGBT Switching Loss, P_{SW}

Switching loss in an IGBT can be calculated by Equation (5), letting I_M be the effective current value of the motor:

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{300}\,. \qquad (5)$$

Where:

f_C is the PWM carrier frequency in Hz,

V_{DC} is the main power supply voltage in V (i.e., the VBB pin input voltage), and

α_E is the slope of the switching loss curve (see Section 15.3.2).

14.1.3 Estimating Junction Temperature of IGBT

The junction temperature under all-IGBT operation, T_j, can be estimated with Equation (6):

$$T_j = R_{(j-C)Q} \times \{(P_{ON} + P_{SW}) \times 6\} + T_C\,. \qquad (6)$$

Where:

$R_{(j-C)Q}$ is the junction-to-case thermal resistance in °C/W under all-IGBT operation, and

T_C is the case temperature in °C, measured at the point defined in Figure 3-1.

14.2 Power MOSFET

Total power loss in a power MOSFET can be obtained by taking the sum of losses including: steady-state loss, P_{RON}; switching loss, P_{SW}; steady-state loss of the body diode, P_{SD}. In the calculation procedure we offer, recovery loss of a body diode, P_{RR}, is considered negligibly small compared with the ratios of other losses.

The following subsections contain the mathematical procedures to calculate these losses (P_{RON}, P_{SW}, and P_{SD}) and the junction temperature under all-IGBT operation.

14.2.1 Power MOSFET Steady-state Loss, P_{RON}

Steady-state loss in a power MOSFET can be computed by using the $R_{DS(ON)}$ vs. I_D curves, listed in Section 15.3.1. As expressed by the curves in Figure 14-2, linear approximations at a range the I_D is actually used are obtained by: $R_{DS(ON)} = \alpha \times I_D + \beta$. The values gained by the above calculation are then applied as parameters in Equation (7), below. Hence, the equation to obtain the power MOSFET steady-state loss, P_{RON}, is:

$$P_{RON} = \frac{1}{2\pi}\int_0^{\pi} I_D(\varphi)^2 \times R_{DS(ON)}(\varphi) \times DT \times d\varphi$$

$$= 2\sqrt{2}\alpha\left(\frac{1}{3\pi}+\frac{3}{32}M\times\cos\theta\right)I_M{}^3 + 2\beta\left(\frac{1}{8}+\frac{1}{3\pi}M\times\cos\theta\right)I_M{}^2 . \tag{7}$$

Where:

I_D is the drain current of the power MOSFET in A,

$R_{DS(ON)}$ is the drain-to-source on-resistance of the power MOSFET in Ω,

DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2} ,$$

M is the modulation index (0 to 1),

cosθ is the motor power factor (0 to 1),

I_M is the effective motor current in A,

α is the slope of the linear approximation in the $R_{DS(ON)}$ vs. I_D curve, and

β is the intercept of the linear approximation in the $R_{DS(ON)}$ vs. I_D curve.

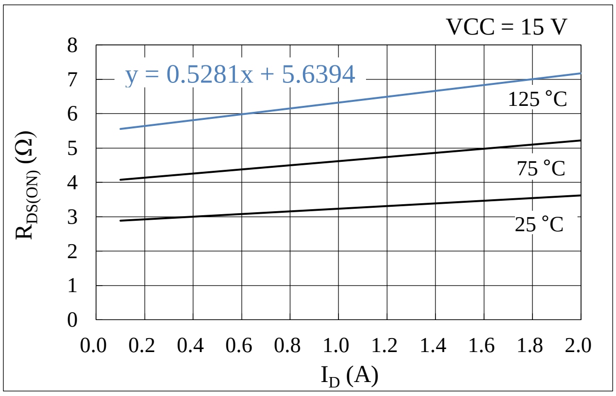


Figure 14-2. Linear Approximate Equation of $R_{DS(ON)}$ vs. I_D Curve

14.2.2 Power MOSFET Switching Loss, P_{SW}

Switching loss in a power MOSFET can be calculated by Equation (8), letting I_M be the effective current value of the motor:

$$P_{SW} = \sqrt{2} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{300} . \tag{8}$$

Where:

f_C is the PWM carrier frequency in Hz,

V_{DC} is the main power supply voltage in V (i.e., the VBB pin input voltage), and

α_E is the slope of the switching loss curve (see Section 15.3.2).

14.2.3 Body Diode Steady-state Loss, P_{SD}

Steady-state loss in a body diode of the power MOSFET can be computed by using the V_{SD} vs. I_{SD} curves, listed in Section 15.3.1. As expressed by the curves in Figure 14-3, linear approximations at a range the I_{SD} is actually used are obtained by: $V_{SD} = \alpha \times I_{SD} + \beta$. The values gained by the above calculation are then applied as parameters in Equation (9), below. Hence, the equation to obtain the body diode steady-state loss, P_{SD}, is:

$$P_{SD} = \frac{1}{2\pi}\int_0^{\pi} V_{SD}\,(\varphi) \times I_{SD}(\varphi) \times (1 - \mathrm{DT}) \times d\varphi$$

$$\begin{aligned} &= \frac{1}{2}\alpha\left(\frac{1}{2} - \frac{4}{3\pi}M \times \cos\theta\right) I_M{}^2 \\ &\qquad + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2} - \frac{\pi}{8}M \times \cos\theta\right) I_M\,. \end{aligned} \tag{9}$$

Where:

V_{SD} is the source-to-drain diode forward voltage of the power MOSFET in V,

I_{SD} is the source-to-drain diode forward current of the power MOSFET in A,

DT is the duty cycle, which is given by

$$\mathrm{DT} = \frac{1 + M \times \sin(\varphi + \theta)}{2}\ ,$$

M is the modulation index (0 to 1),

cosθ is the motor power factor (0 to 1),

I_M is the effective motor current in A,

α is the slope of the linear approximation in the V_{SD} vs. I_{SD} curve, and

β is the intercept of the linear approximation in the V_{SD} vs. I_{SD} curve.

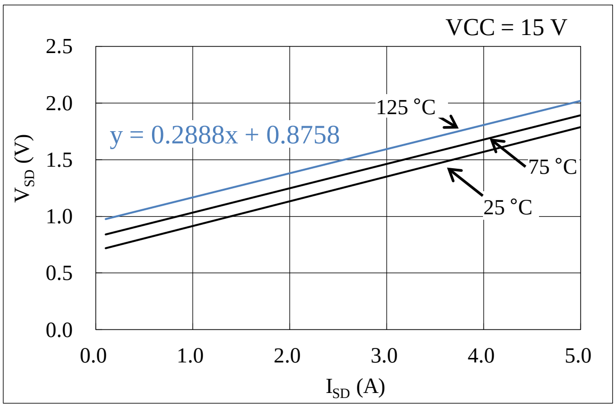


Figure 14-3. Linear Approximate Equation of V_{SD} vs. I_{SD} Curve

14.2.4 Estimating Junction Temperature of Power MOSFET

The junction temperature under all-power-MOSFET operation, T_j, can be estimated with Equation (10):

$$T_j = R_{j-C} \times \{(P_{ON} + P_{SW} + P_{SD}) \times 6\} + T_C\,. \tag{10}$$

Where:

R_{j-C} is the junction-to-case thermal resistance in °C/W under all-power-MOSFET operation, and

T_C is the case temperature in °C, measured at the point defined in Figure 3-1.

15. Performance Curves

15.1 Transient Thermal Resistance Curves

The following graphs represent transient thermal resistance (the ratios of transient thermal resistance), with steady-state thermal resistance = 1.

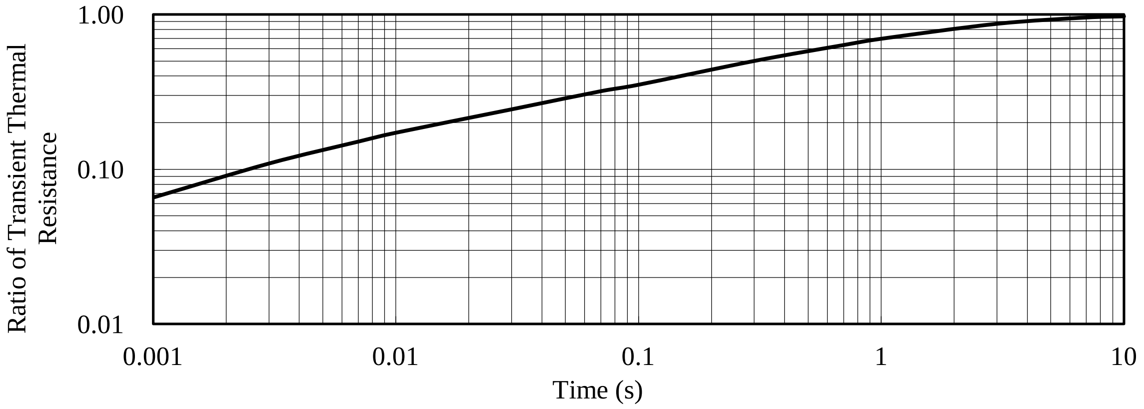


Figure 15-1. SIM681xM Ratio of Transient Thermal Resistance

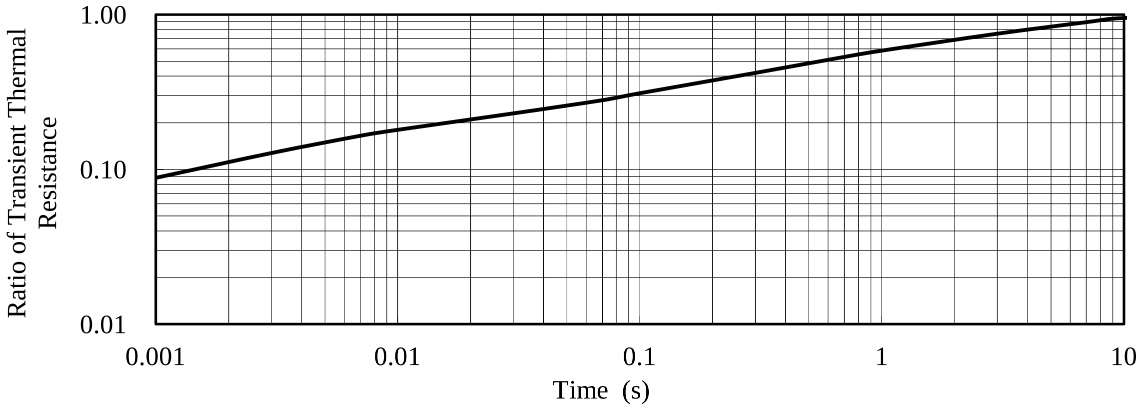


Figure 15-2. SIM682xM Ratio of Transient Thermal Resistance

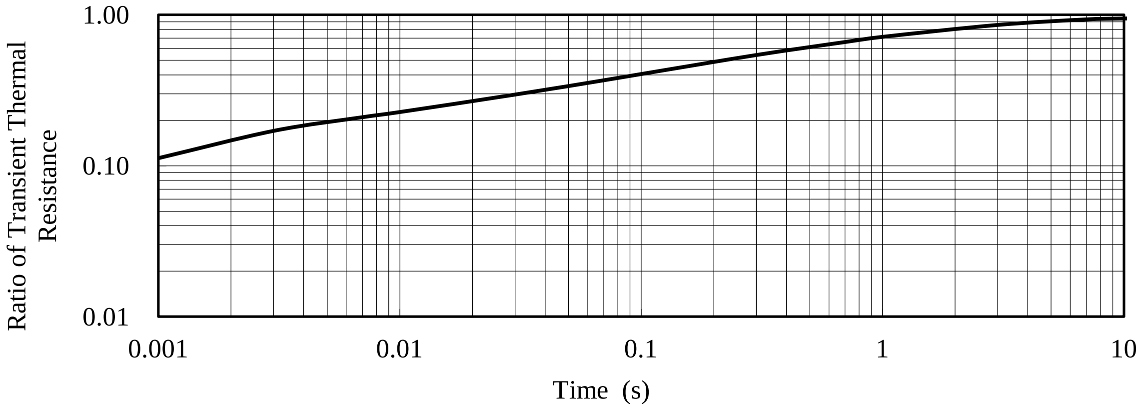


Figure 15-3. SIM6818M Ratio of Transient Thermal Resistance

15.2 Performance Curves of Control Parts

Figure 15-4 to Figure 15-28 provide performance curves of the control parts integrated in the SIM6800M series, including variety-dependent characteristics and thermal characteristics. T_j represents the junction temperature of the control parts.

Table 15-1. Typical Characteristics of Control Parts

Figure Number	Figure Caption
Figure 15-4	Logic Supply Current, I_{CC} vs. T_C (INx = 0 V)
Figure 15-5	Logic Supply Current, I_{CC} vs. T_C (INx = 5 V)
Figure 15-6	VCCx Pin Voltage, V_{CC} – Logic Supply Current, I_{CC} curve
Figure 15-7	Logic Supply Current (1-phase) I_{BS} (HINx = 0 V)
Figure 15-8	Logic Supply Current (1-phase) I_{BS} (HINx = 5 V)
Figure 15-9	VBx Pin Voltage, V_B – Logic Supply Current I_{BS} curve (HINx = 0 V)
Figure 15-10	Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C
Figure 15-11	Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C
Figure 15-12	Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C
Figure 15-13	Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C
Figure 15-14	UVLO_VB Filtering Time vs. T_C
Figure 15-15	UVLO_VCC Filtering Time vs. T_C
Figure 15-16	High Level Input Threshold Voltage, V_{IH} vs. T_C
Figure 15-17	Low Level Input Threshold Voltage, V_{IL} vs. T_C
Figure 15-18	Input Current at High Level (HINx or LINx), I_{IN} vs. T_C
Figure 15-19	High-side Turn-on Propagation Delay vs. T_C (from HINx to HOx)
Figure 15-20	Low-side Turn-on Propagation Delay vs. T_C (from LINx to LOx)
Figure 15-21	Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. T_C
Figure 15-22	Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. T_C
Figure 15-23	SD Pin Filtering Time vs. T_C
Figure 15-24	FO Pin Filtering Time vs. T_C
Figure 15-25	Current Limit Reference Voltage, V_{LIM} vs. T_C
Figure 15-26	Overcurrent Protection Threshold Voltage, V_{TRIP} vs. T_C
Figure 15-27	Overcurrent Protection Hold Time, t_P vs. T_C
Figure 15-28	Overcurrent Protection Blanking Time, $t_{BK(OCP)}$ vs. T_C, Current Limit Blanking Time, $t_{BK(OCL)}$ vs. T_C

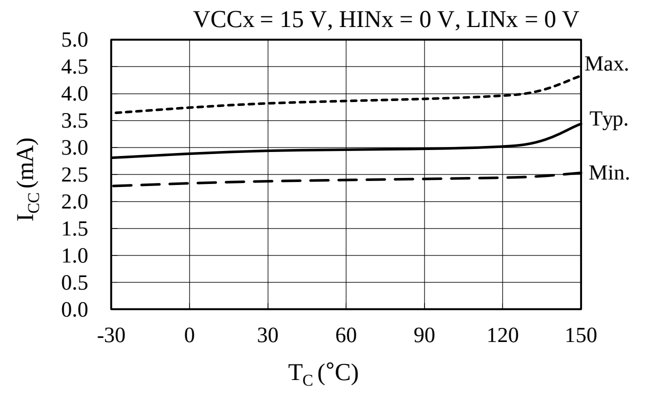


Figure 15-4. Logic Supply Current, I_{CC} vs. T_C (INx = 0 V)

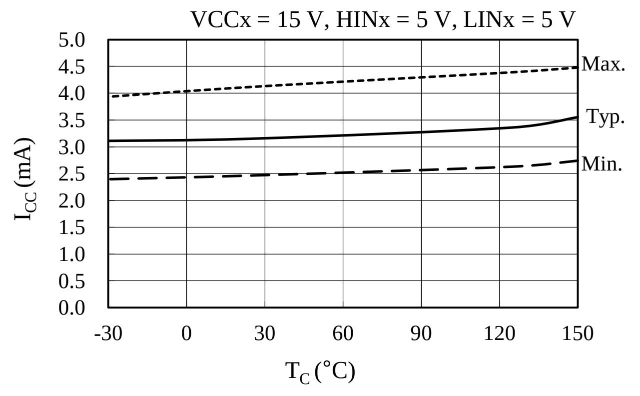


Figure 15-5. Logic Supply Current, I_{CC} vs. T_C (INx = 5 V)

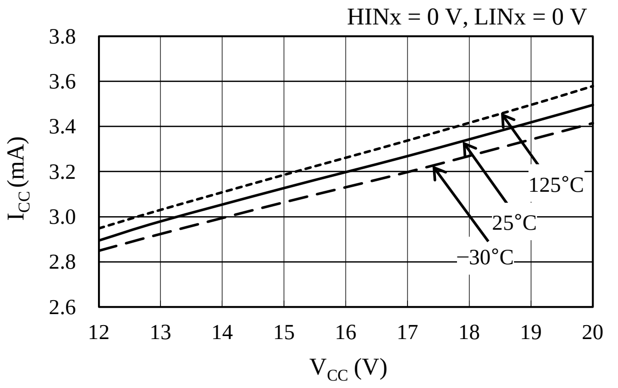


Figure 15-6. VCCx Pin Voltage, V_{CC} – Logic Supply Current, I_{CC} curve

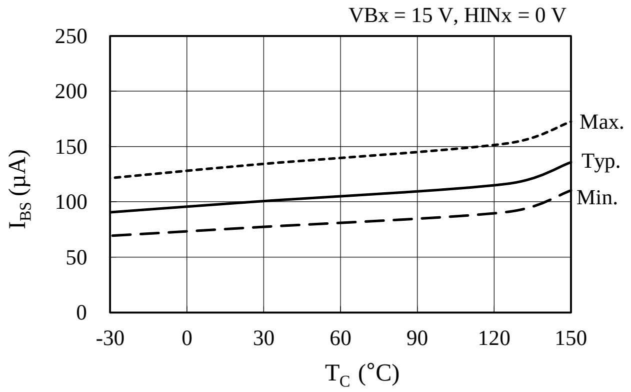


Figure 15-7. Logic Supply Current (1-phase) I_{BS} (HINx = 0 V)

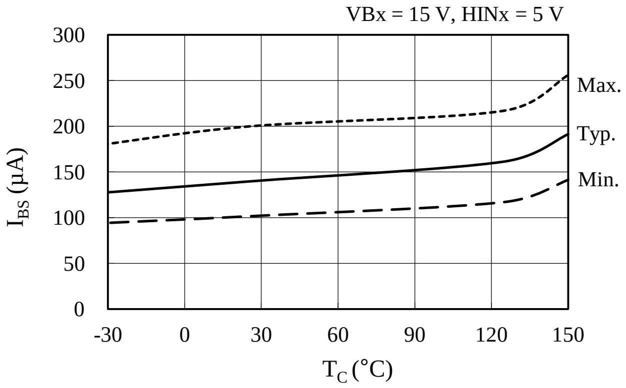


Figure 15-8. Logic Supply Current (1-phase) I_{BS} (HINx = 5 V)

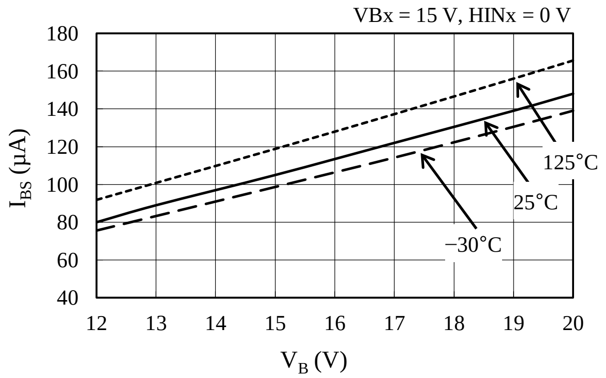


Figure 15-9. VBx Pin Voltage, V_B – Logic Supply Current I_{BS} curve (HINx = 0 V)

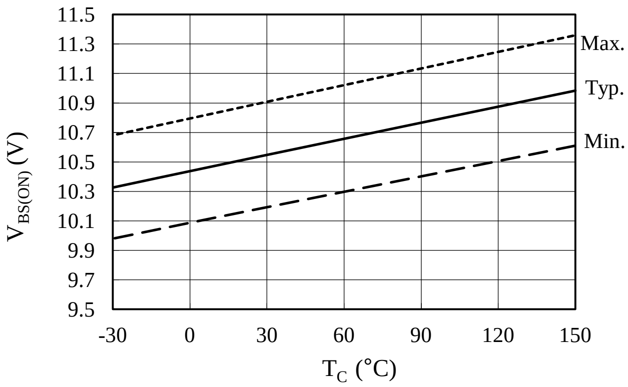


Figure 15-10. Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C

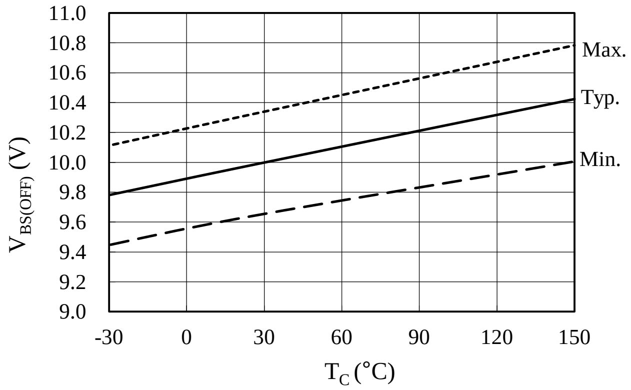
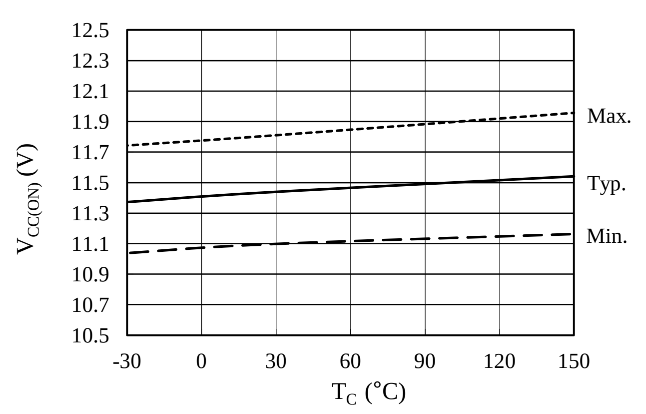


Figure 15-11. Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C



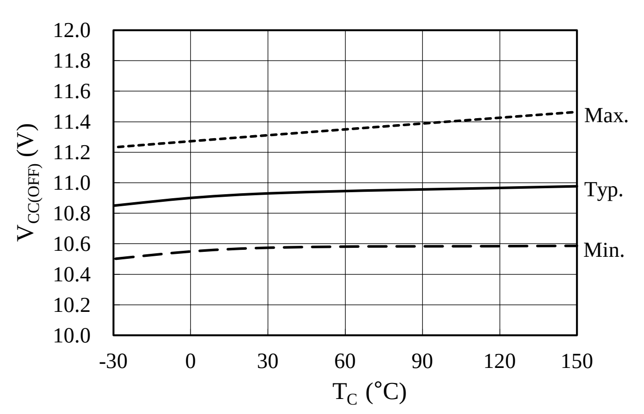
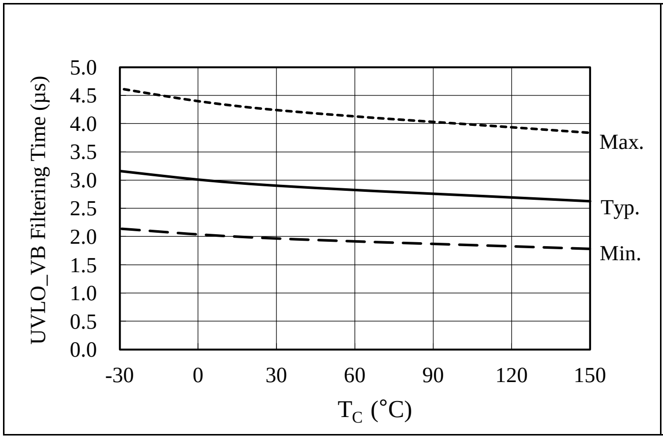


Figure 15-12. Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C

Figure 15-13. Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C



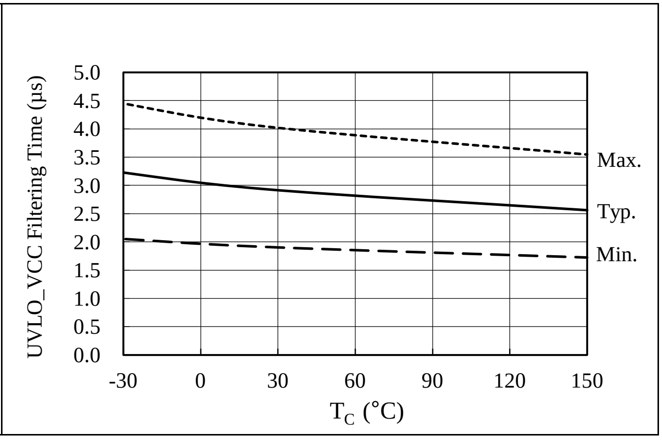
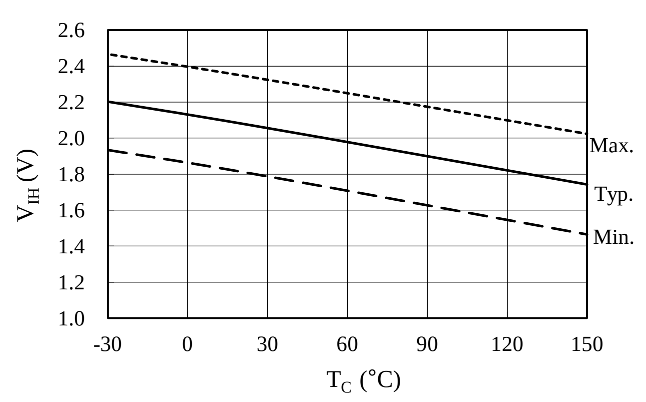


Figure 15-14. UVLO_VB Filtering Time vs. T_C

Figure 15-15. UVLO_VCC Filtering Time vs. T_C



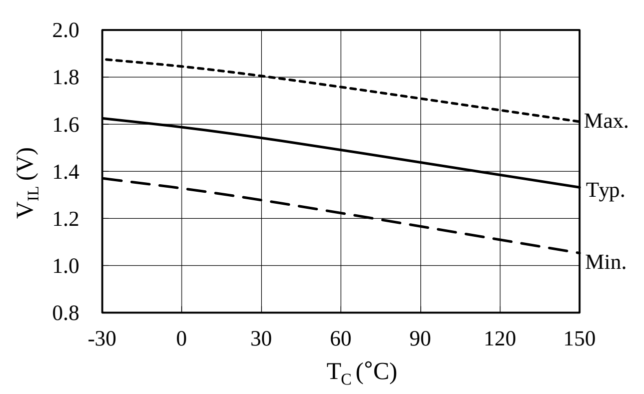


Figure 15-16. High Level Input Threshold Voltage, V_{IH} vs. T_C

Figure 15-17. Low Level Input Threshold Voltage, V_{IL} vs. T_C

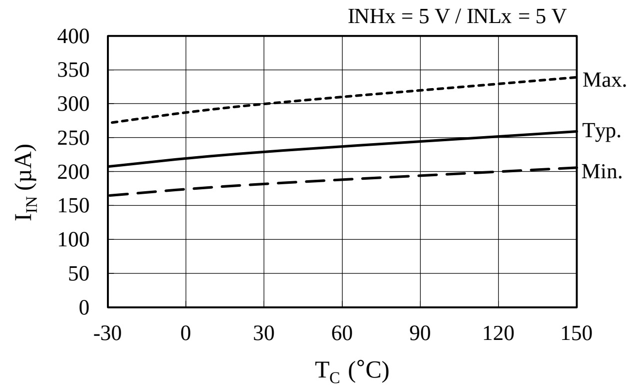


Figure 15-18. Input Current at High Level (HINx or LINx), I_{IN} vs. T_C

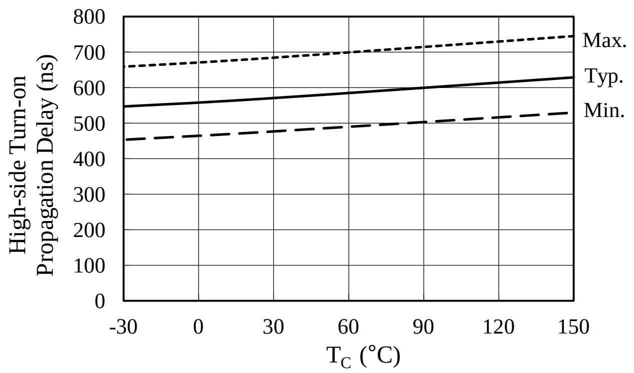


Figure 15-19. High-side Turn-on Propagation Delay vs. T_C (from HINx to HOx)

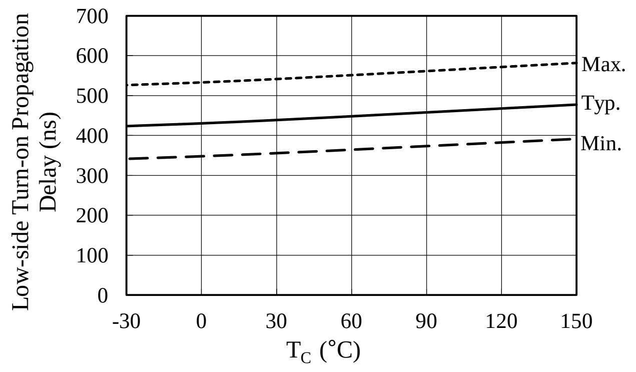


Figure 15-20. Low-side Turn-on Propagation Delay vs. T_C (from LINx to LOx)

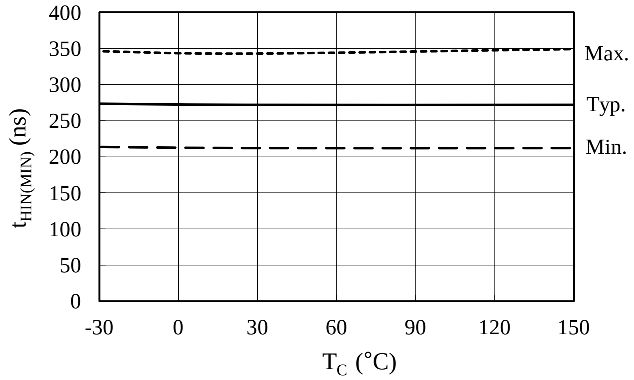


Figure 15-21. Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. T_C

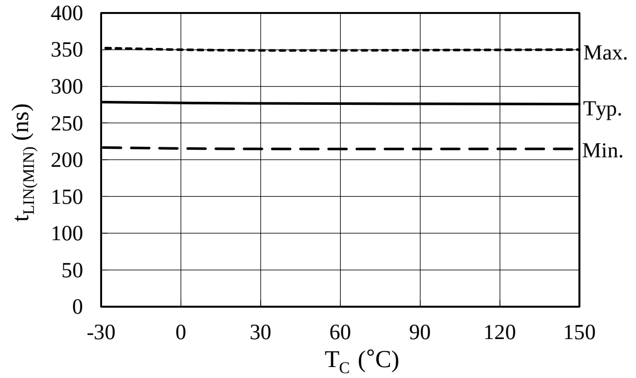


Figure 15-22. Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. T_C

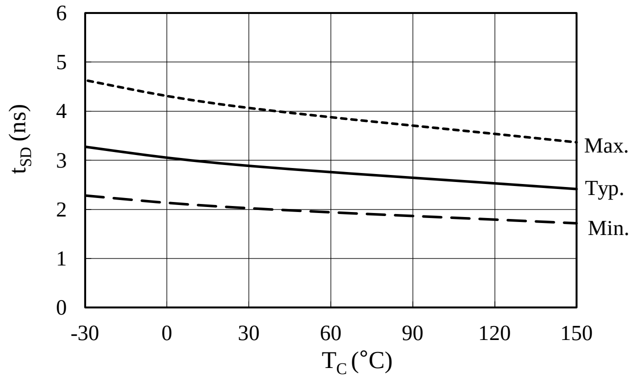


Figure 15-23. SD Pin Filtering Time vs. T_C

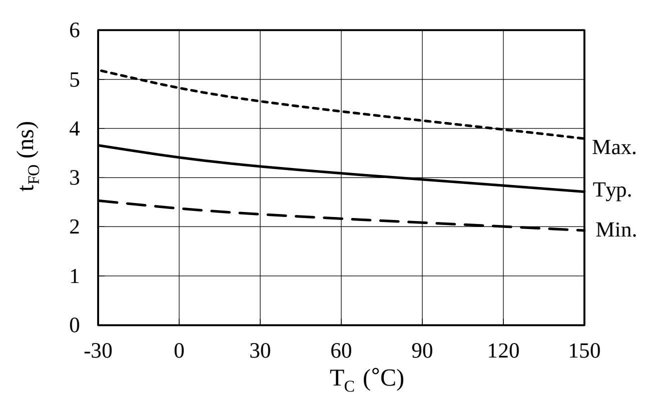


Figure 15-24. FO Pin Filtering Time vs. T_C

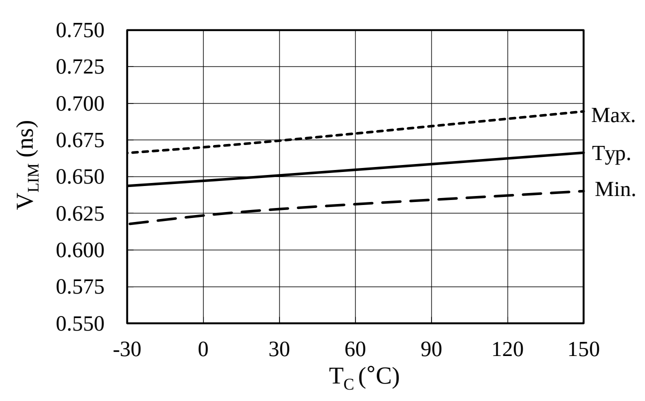


Figure 15-25. Current Limit Reference Voltage, V_{LIM} vs. T_C

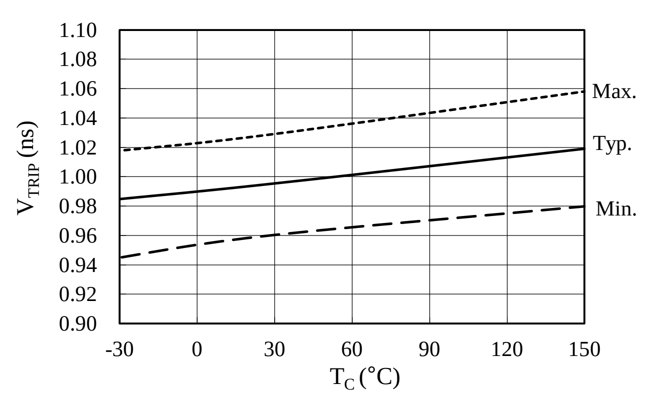


Figure 15-26. Overcurrent Protection Threshold Voltage, V_{TRIP} vs. T_C

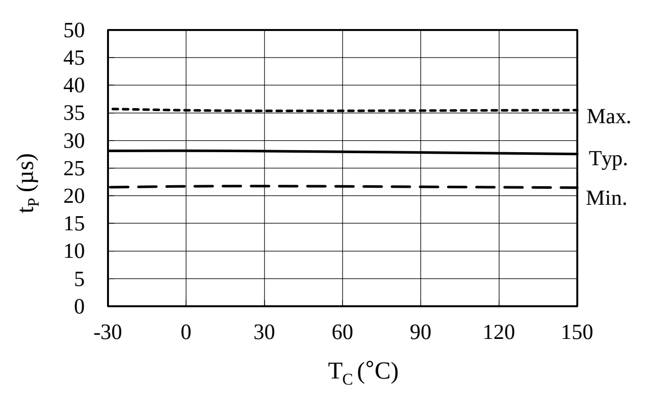


Figure 15-27. Overcurrent Protection Hold Time, t_P vs. T_C

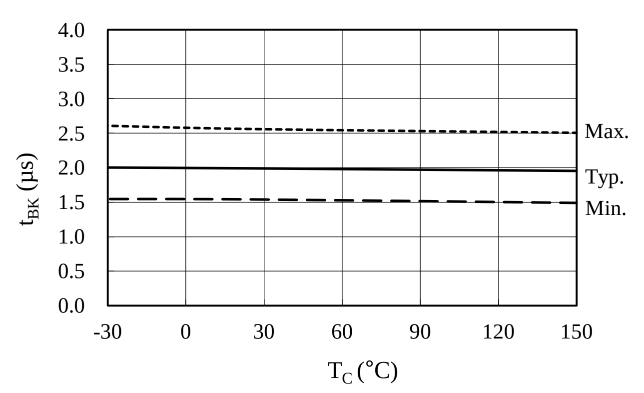


Figure 15-28. Overcurrent Protection Blanking Time, $t_{BK(OCP)}$ vs. T_C, Current Limit Blanking Time, $t_{BK(OCL)}$ vs. T_C

15.3 Performance Curves of Output Parts

15.3.1 Output Transistor Performance Curves

15.3.1.1. SIM6811M

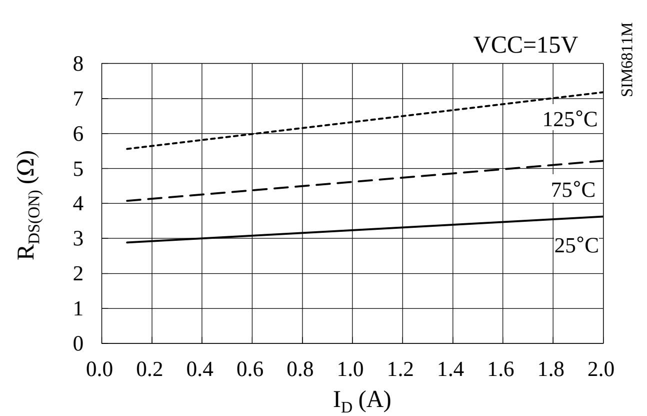


Figure 15-29. Power MOSFET $R_{DS(ON)}$ – I_D curve

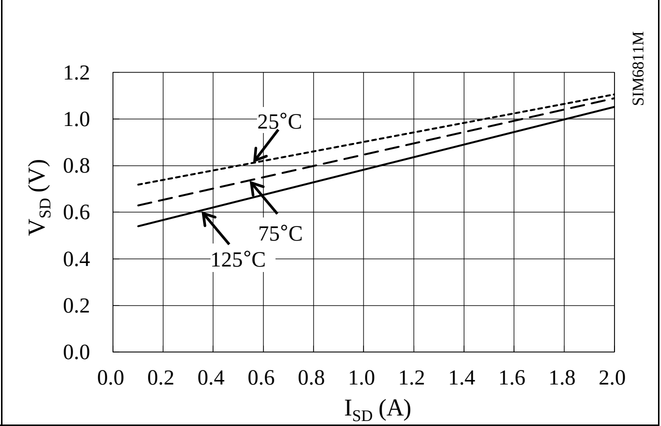


Figure 15-30. Power MOSFET V_{SD} – I_{SD} curve

15.3.1.2. SIM6812M

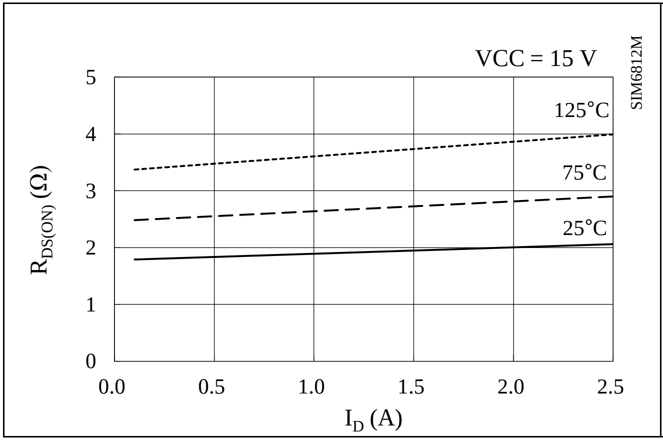


Figure 15-31. Power MOSFET $R_{DS(ON)}$ – I_D curve

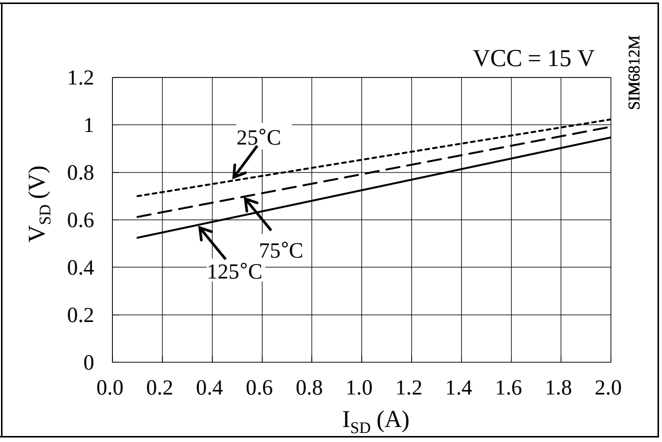


Figure 15-32. Power MOSFET V_{SD} – I_{SD} curve

15.3.1.3. SIM6813M

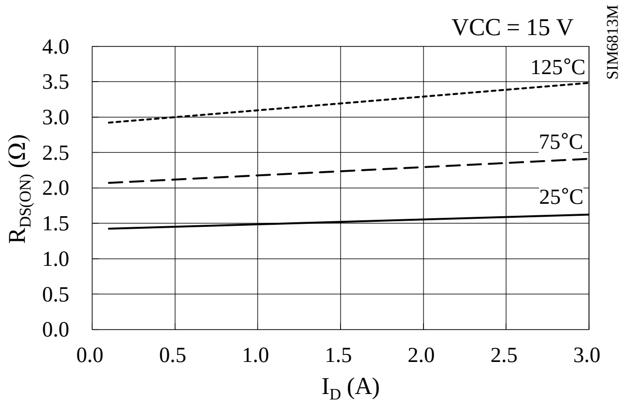


Figure 15-33. Power MOSFET $R_{DS(ON)}$ – I_D curve

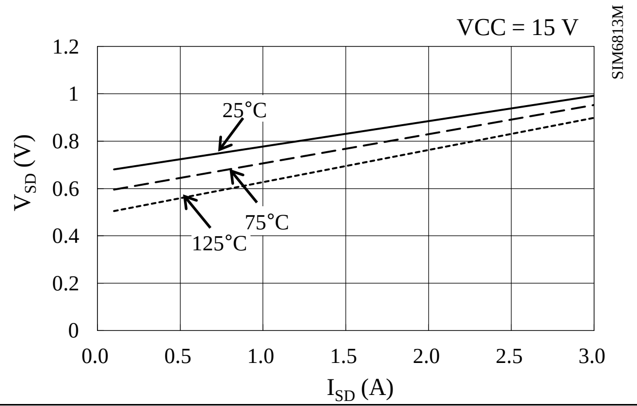


Figure 15-34. Power MOSFET V_{SD} – I_{SD} curve

15.3.1.4. SIM6880M

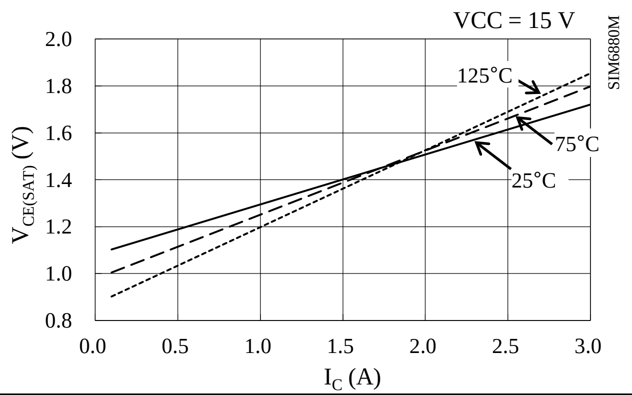


Figure 15-35. IGBT $V_{CE(SAT)}$ – I_C curve

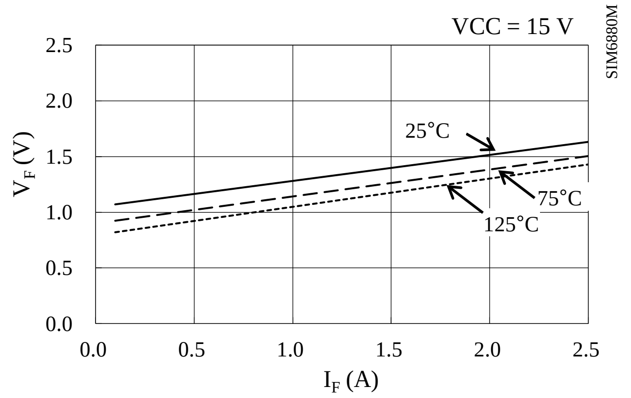


Figure 15-36. FRD V_F – I_F curve

15.3.1.5. SIM6822M and SIM6827M

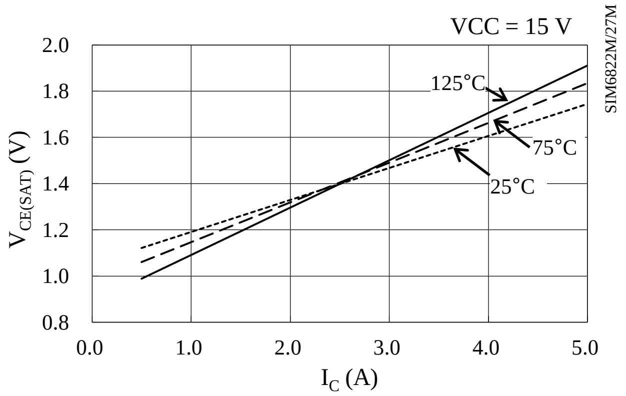


Figure 15-37. IGBT $V_{CE(SAT)}$ – I_C curve

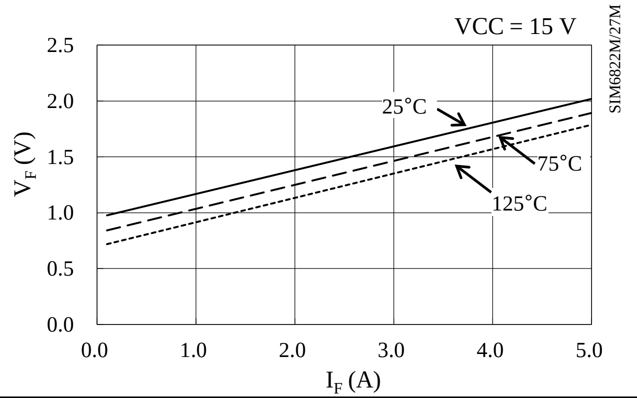


Figure 15-38. FRD V_F – I_F curve

15.3.2 Switching Losses

Conditions: VBB = 300 V, half-bridge circuit with inductive load.
Switching Loss, E, is the sum of turn-on loss and turn-off loss.

15.3.2.1. SIM6811M

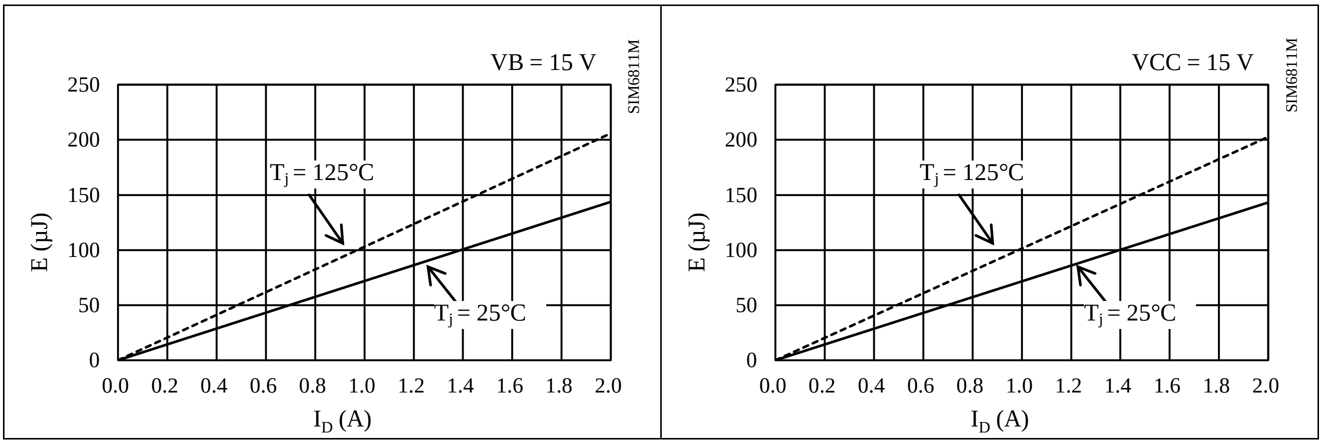


Figure 15-39. High-side Switching Loss

Figure 15-40. Low-side Switching Loss

15.3.2.2. SIM6812M

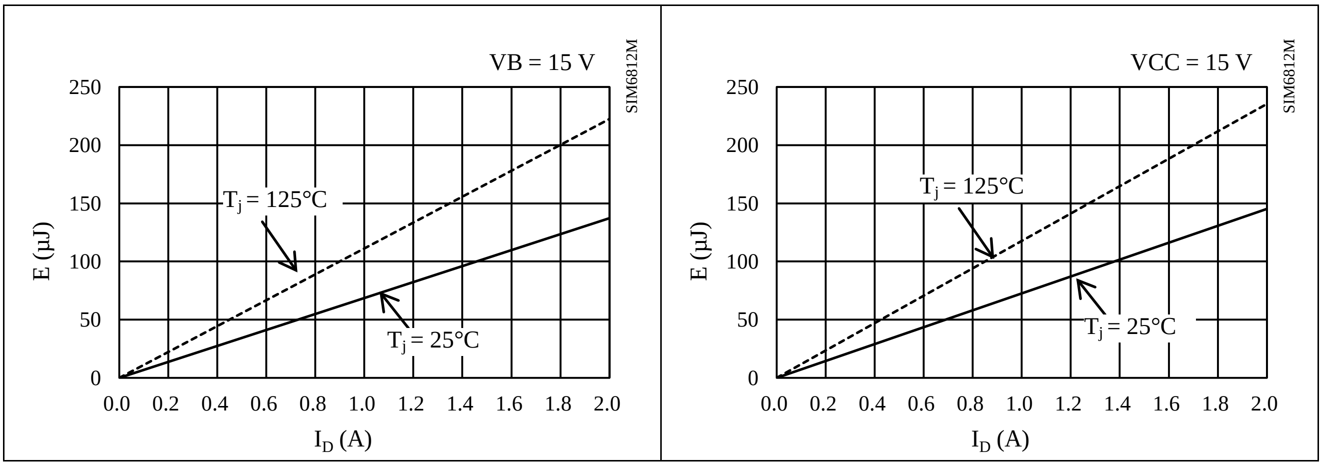


Figure 15-41. High-side Switching Loss

Figure 15-42. Low-side Switching Loss

15.3.2.3. SIM6813M

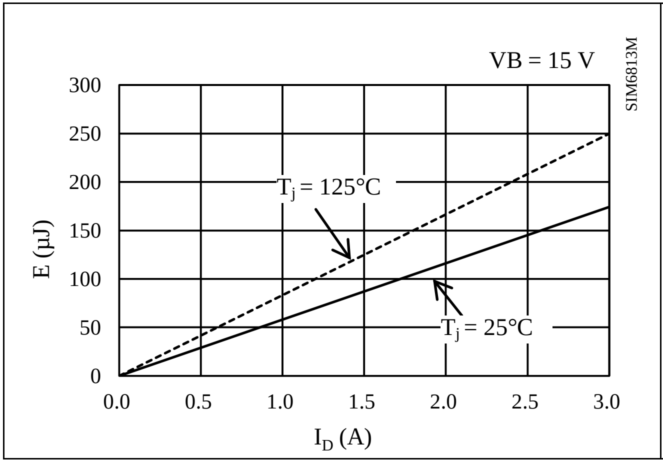


Figure 15-43. High-side Switching Loss

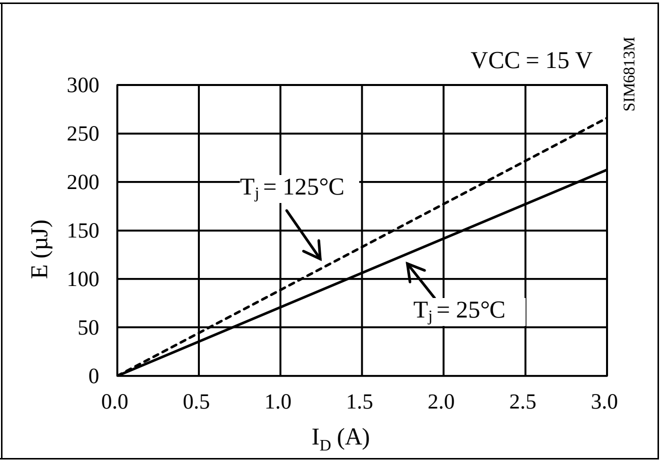


Figure 15-44. Low-side Switching Loss

15.3.2.4. SIM6880M

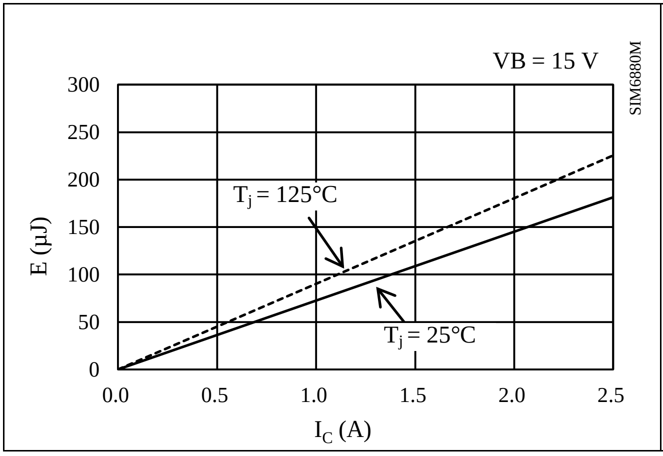


Figure 15-45. High-side Switching Loss

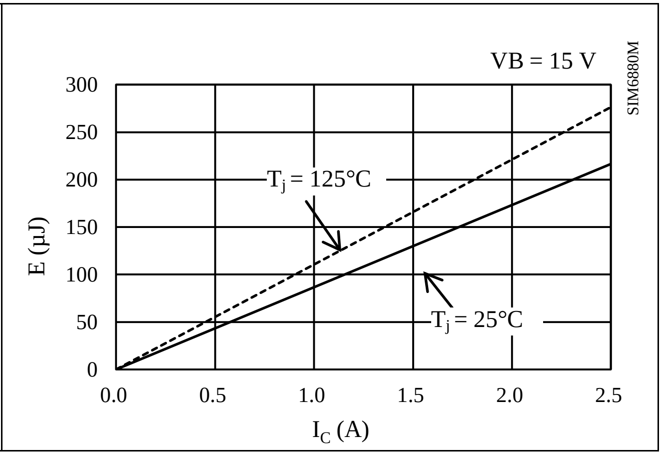


Figure 15-46. Low-side Switching Loss

15.3.2.5. SIM6822M

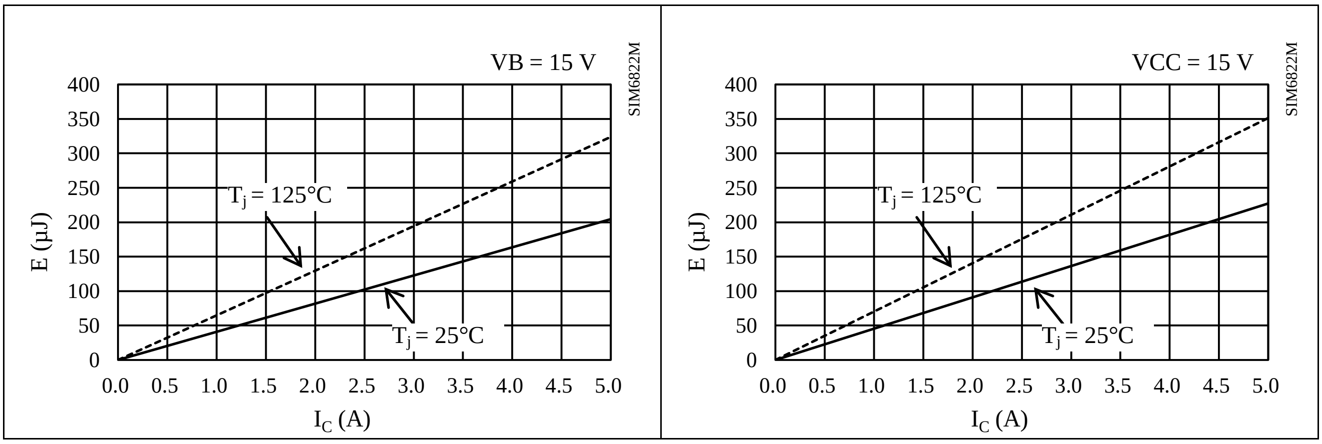


Figure 15-47. High-side Switching Loss

Figure 15-48. Low-side Switching Loss

15.3.2.6. SIM6827M

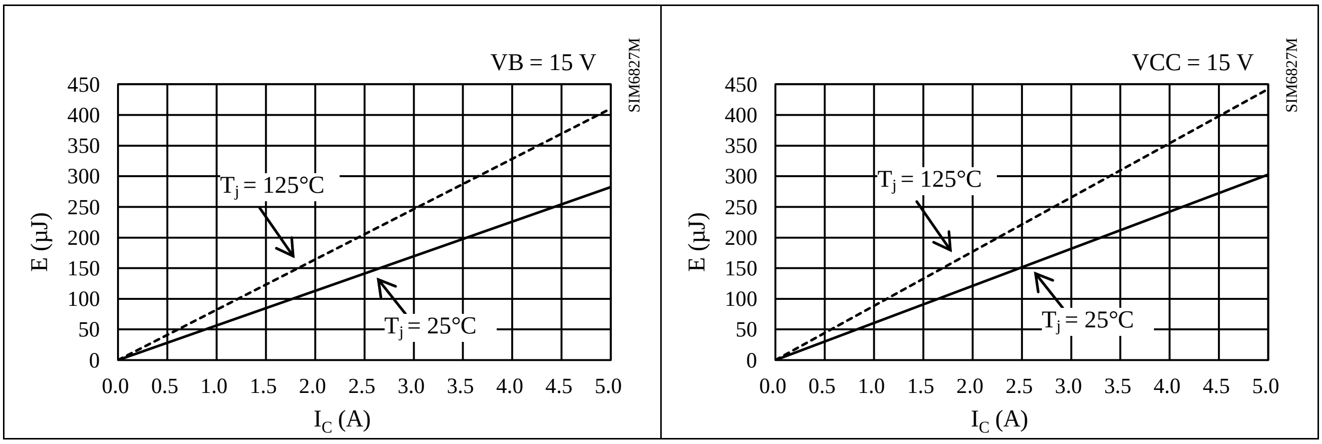


Figure 15-49. High-side Switching Loss

Figure 15-50. Low-side Switching Loss

15.4 Allowable Effective Current Curves

The following curves represent allowable effective currents in sine-wave driving under a 3-phase PWM system. All the values listed in this section, including $R_{DS(ON)}$ or $V_{CE(SAT)}$ of output transistors and switching losses, are typical values.

Operating conditions: VBB pin input voltage, V_{DC} = 300 V; VCC pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_j = 150 °C.

15.4.1 SIM6811M

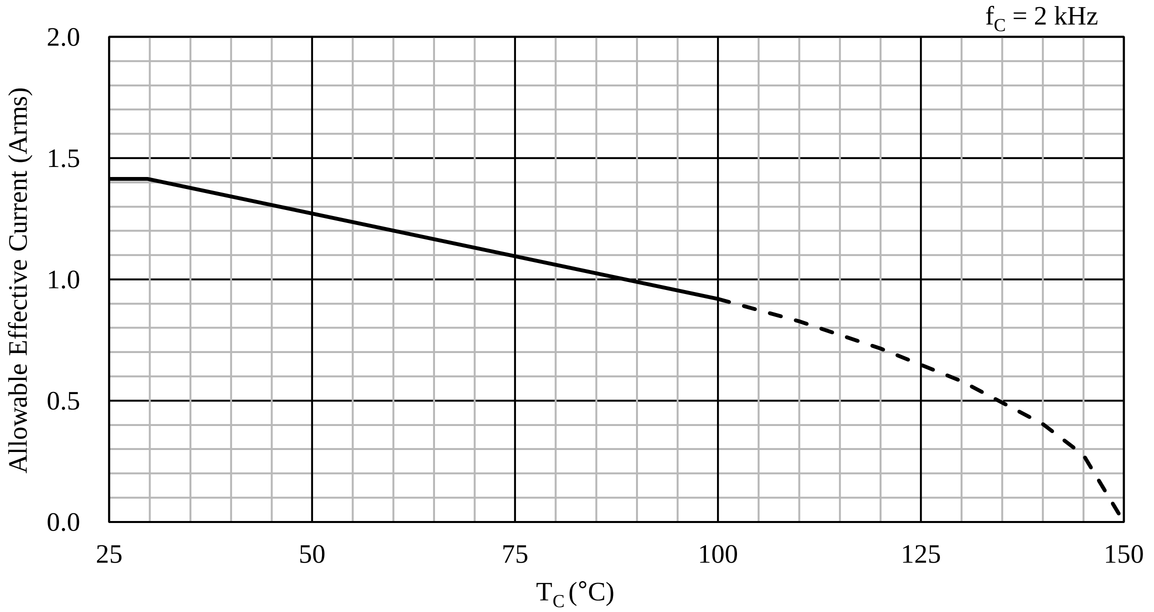


Figure 15-51. SIM6811M Allowable Effective Current Curve (f_C = 2 kHz)

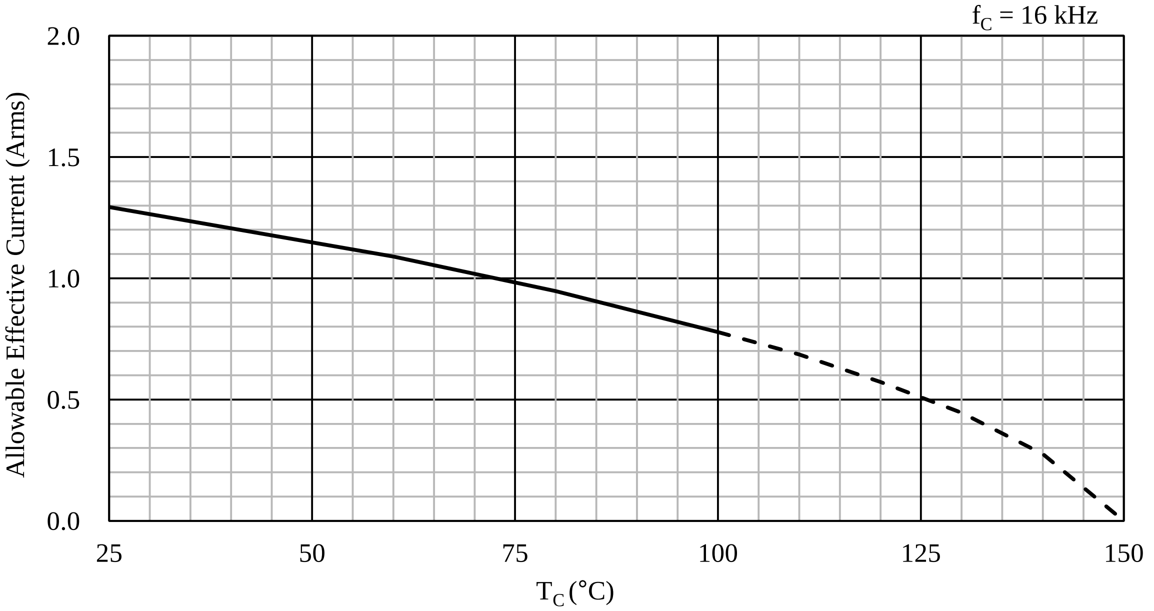


Figure 15-52. SIM6811M Allowable Effective Current Curve (f_C = 16 kHz)

15.4.2 SIM6812M

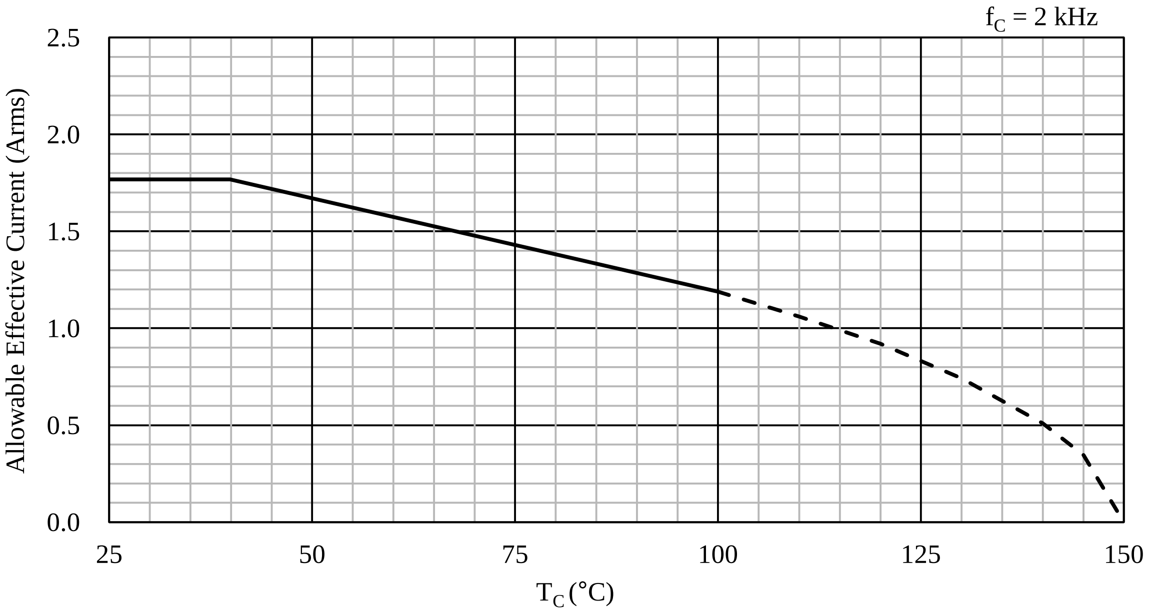


Figure 15-53. SIM6812M Allowable Effective Current Curve (f_C = 2 kHz)

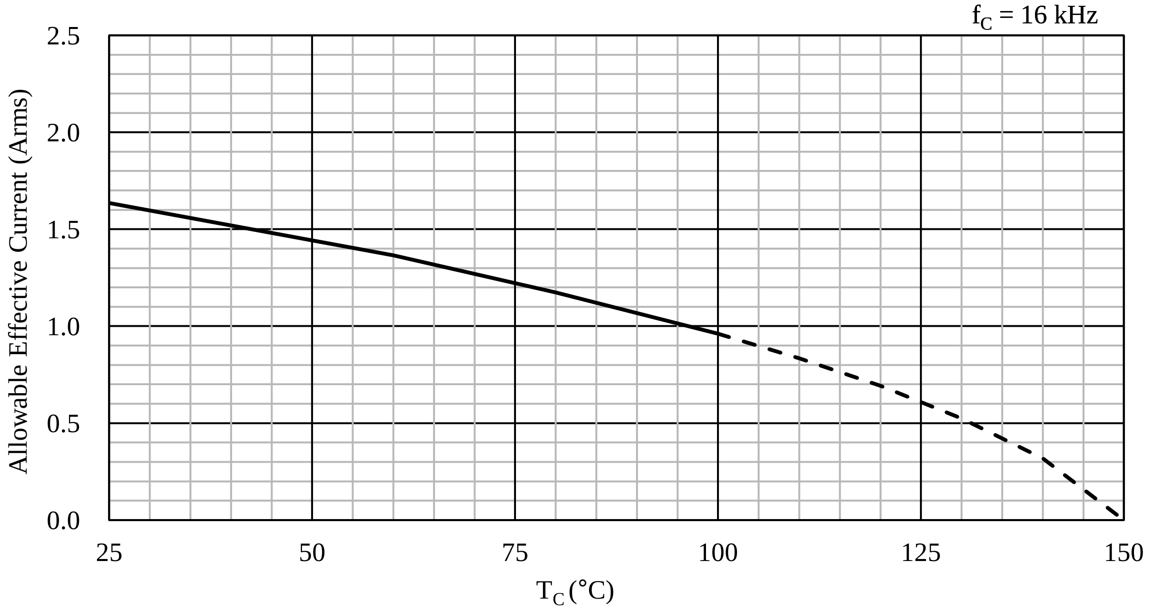


Figure 15-54. SIM6812M Allowable Effective Current Curve (f_C = 16 kHz)

15.4.3 SIM6813M

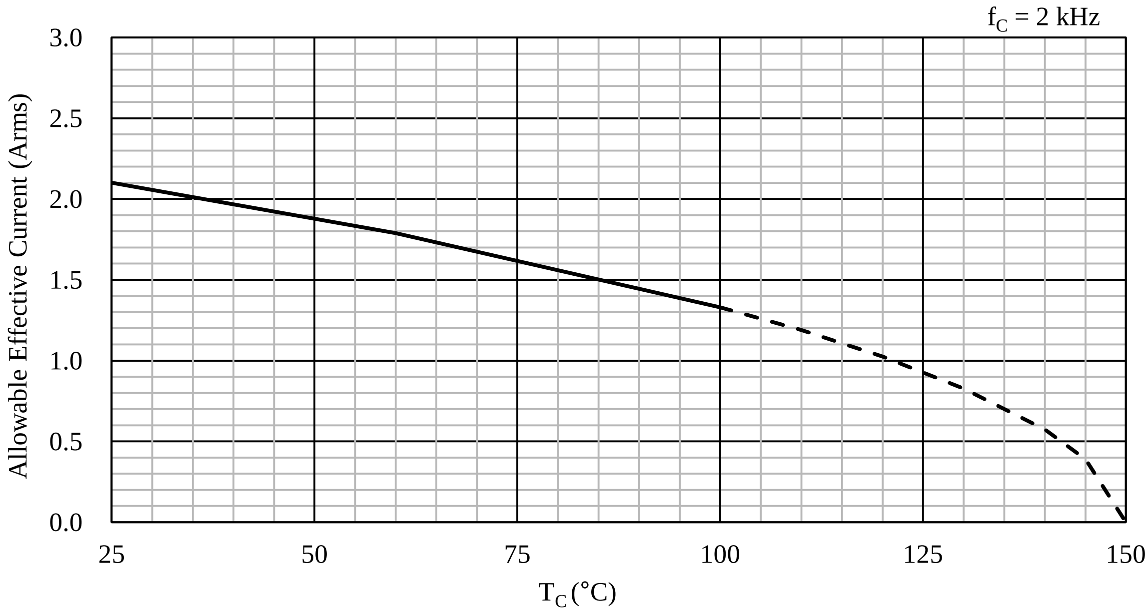


Figure 15-55. SIM6813M Allowable Effective Current Curve (f_C = 2 kHz)

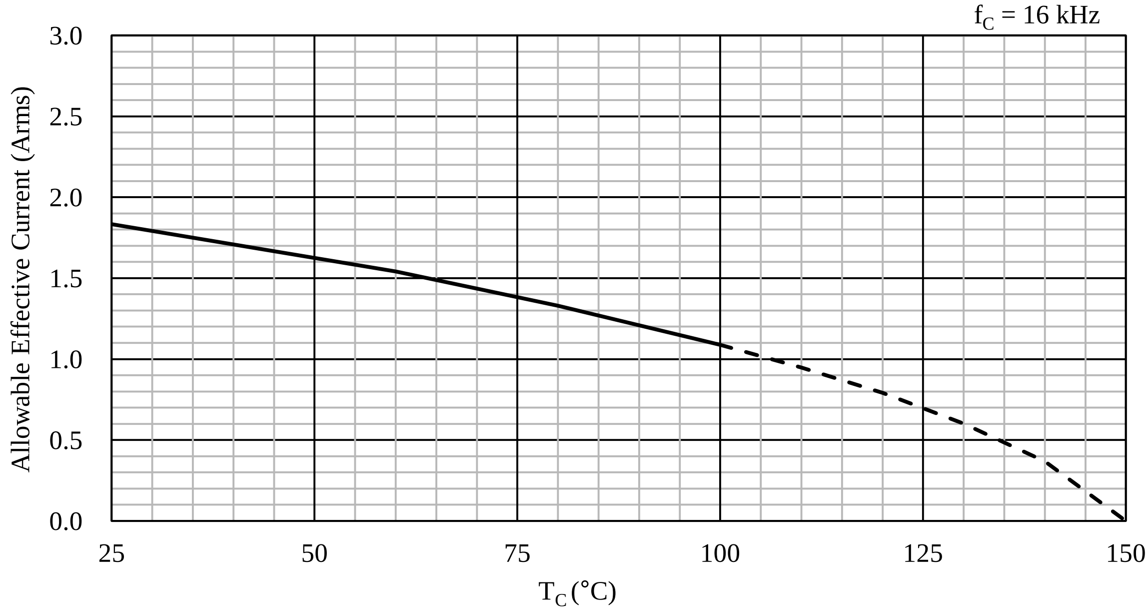


Figure 15-56. SIM6813M Allowable Effective Current Curve (f_C = 16 kHz)

15.4.4 SIM6880M

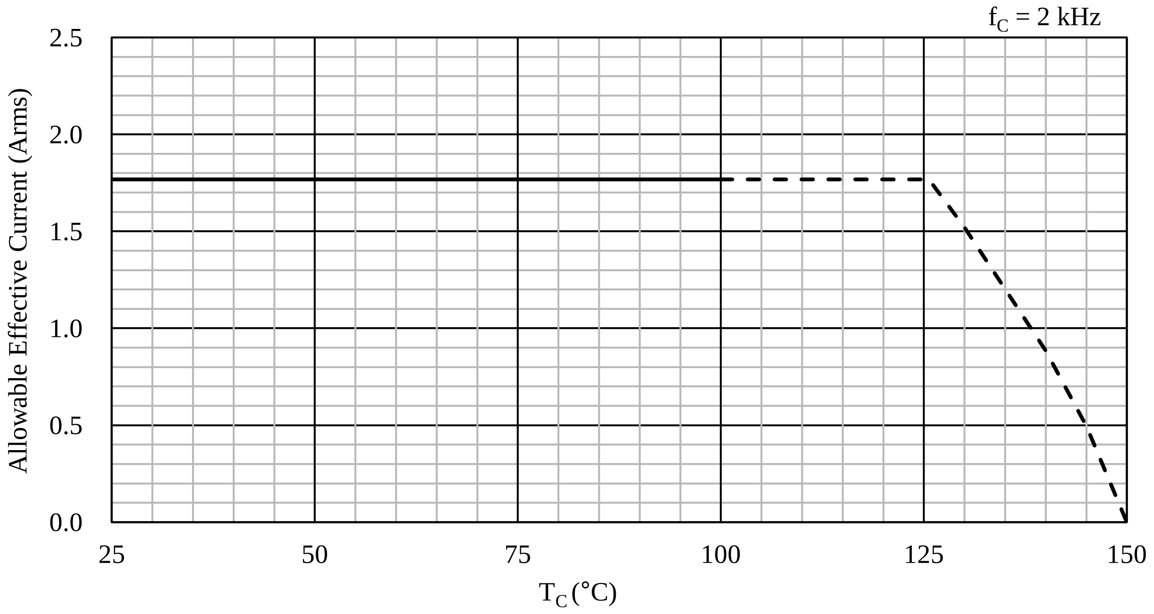


Figure 15-57. SIM6880M Allowable Effective Current Curve (f_C = 2 kHz)

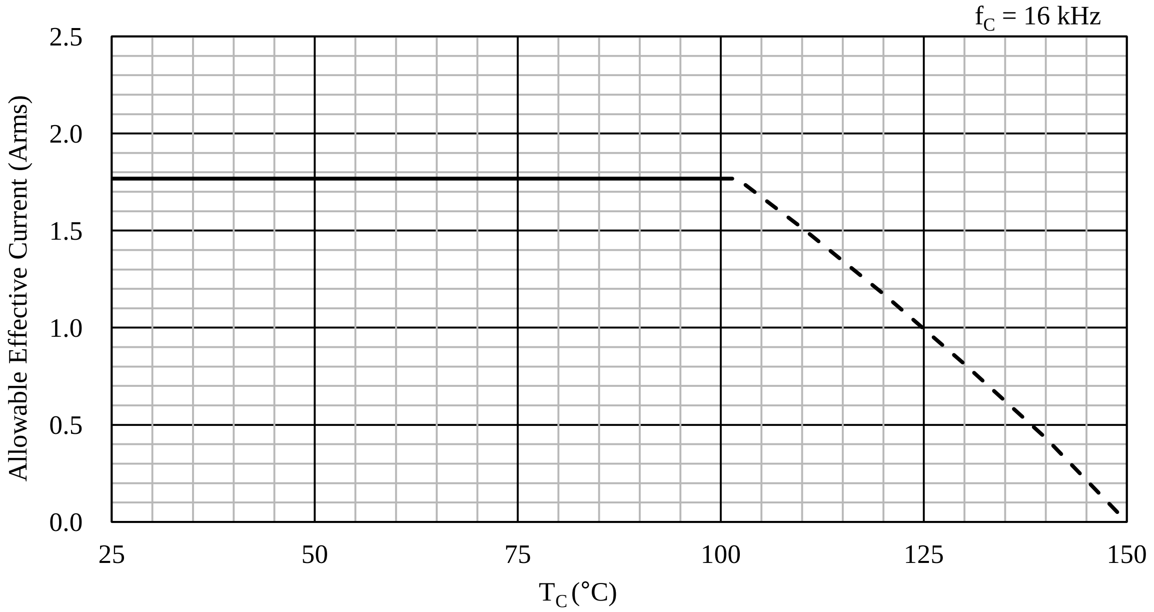


Figure 15-58. SIM6880M Allowable Effective Current Curve (f_C = 16 kHz)

15.4.5 SIM6822M

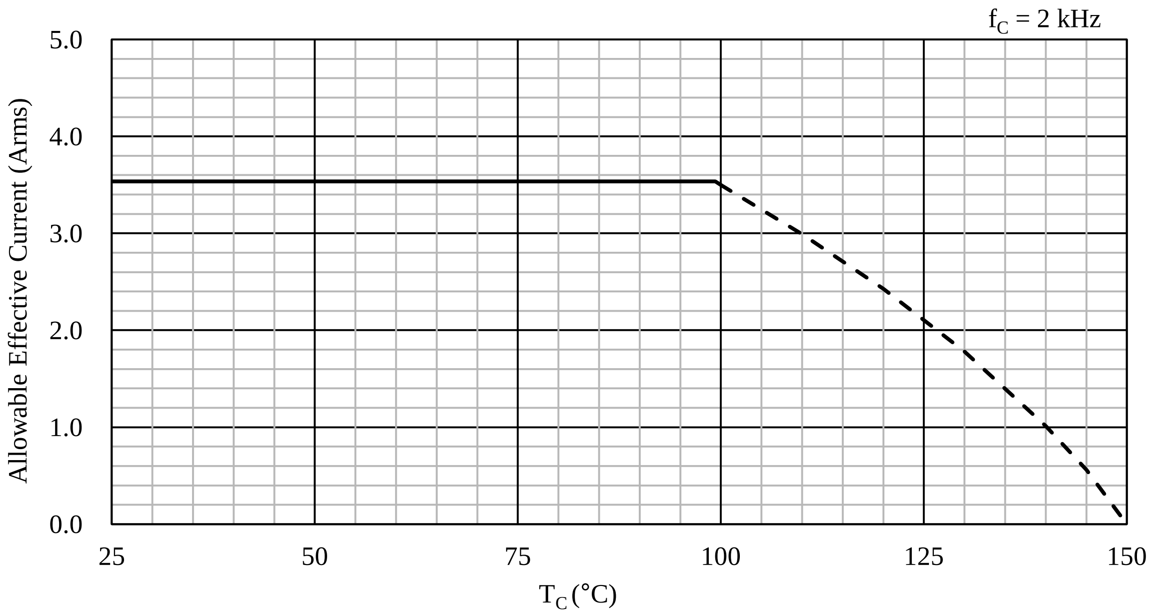


Figure 15-59. Allowable Effective Current Curve (f_C = 2 kHz)

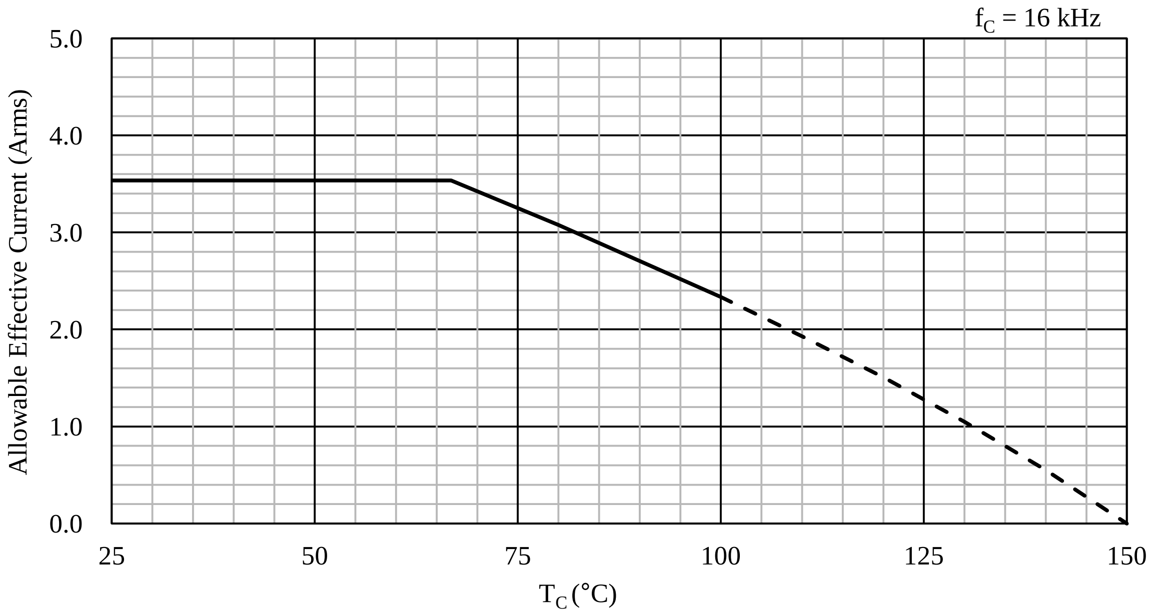


Figure 15-60. SIM6822M Allowable Effective Current Curve (f_C = 16 kHz)

15.4.6 SIM6827M

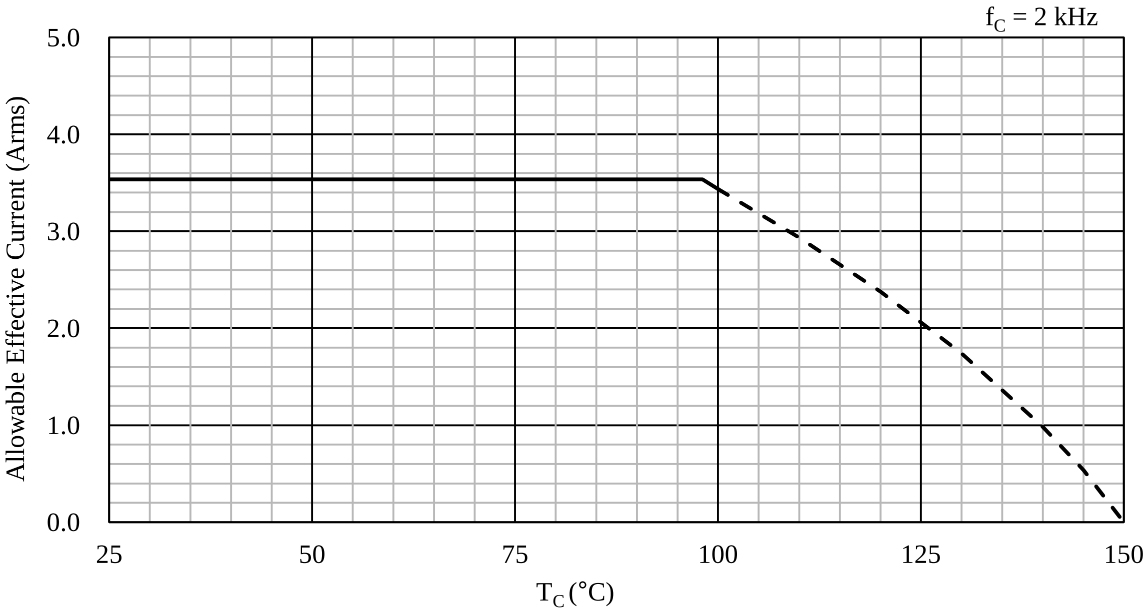


Figure 15-61. SIM6827M Allowable Effective Current Curve (f_C = 2 kHz)

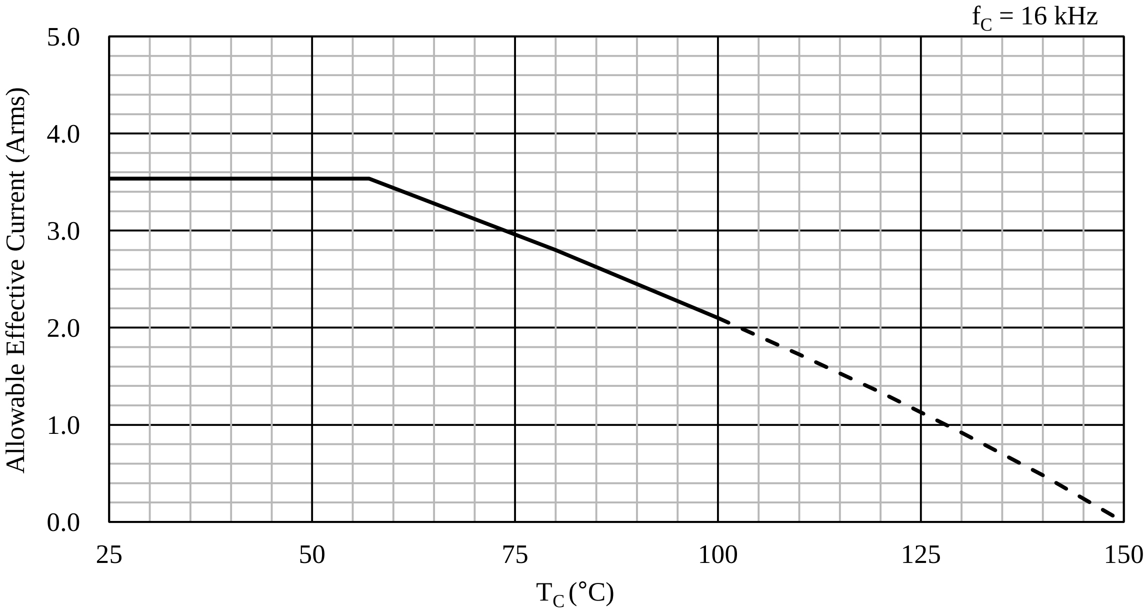


Figure 15-62. SIM6827M Allowable Effective Current Curve (f_C = 16 kHz)

15.5 Short Circuit SOAs (Safe Operating Areas)

This section provides the graphs illustrating the short circuit SOAs of the SIM6800M series devices whose output transistors consist of built-in IGBTs.

Conditions: $V_{DC} \leq 400$ V, 13.5 V ≤ VCC ≤ 16.5 V, $T_j = 125$ °C, 1 pulse.

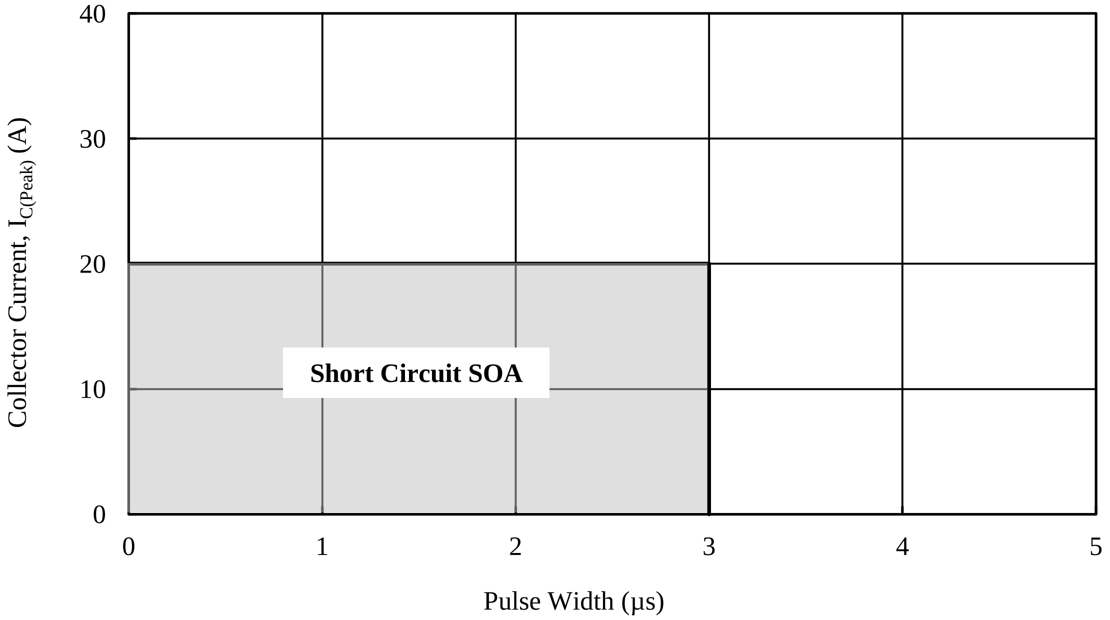


Figure 15-63. Short Circuit SOA of SIM6880M

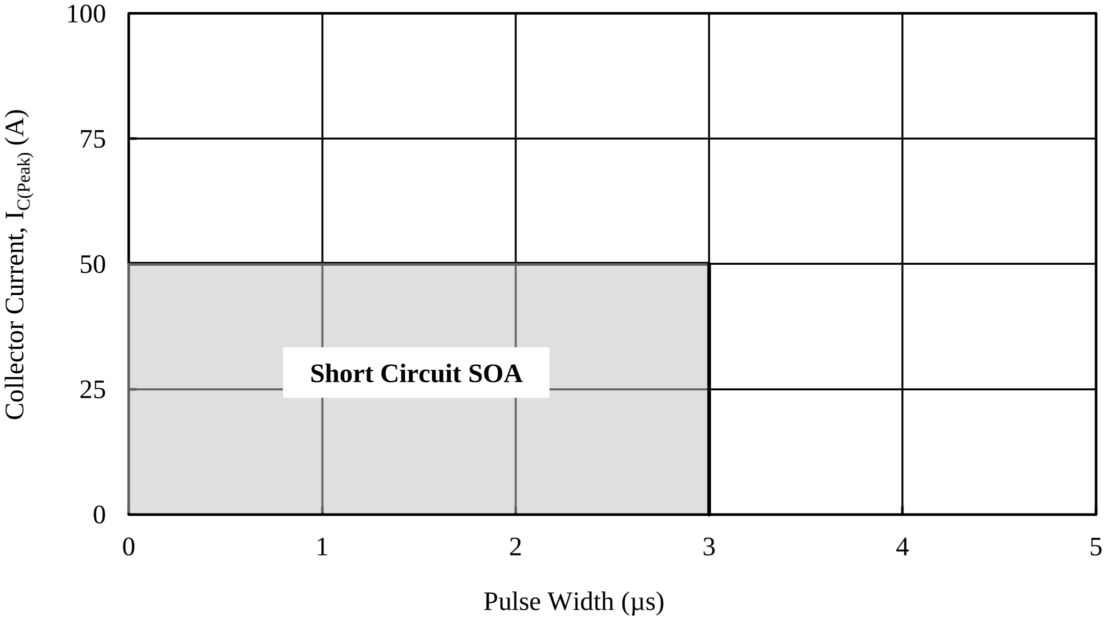


Figure 15-64. Short Circuit SOA of SIM6822M or SIM6827M

16. Pattern Layout Example

This section contains the schematic diagrams of a PCB pattern layout example using an SIM6800M series device. For more details on through holes, see Section 10.

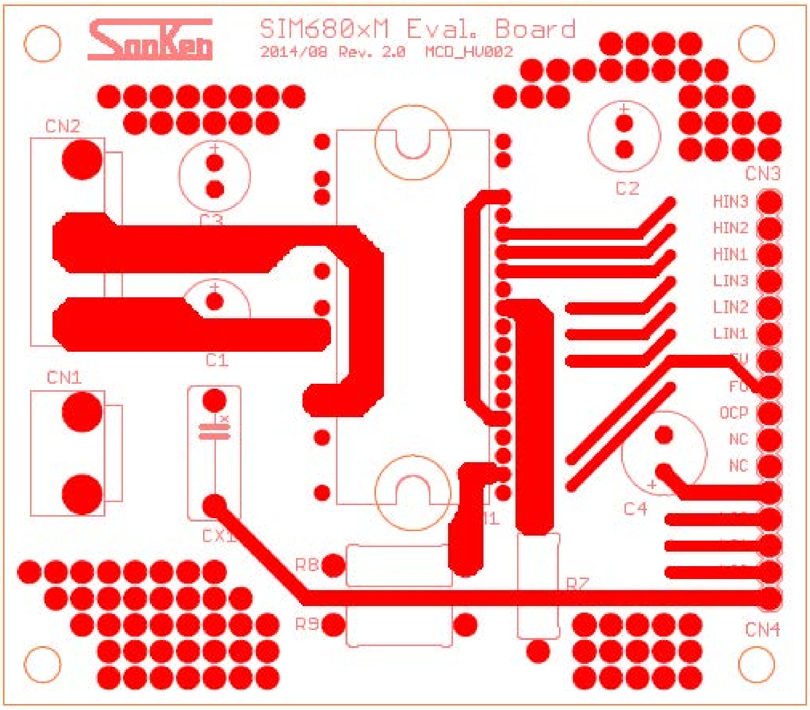


Figure 16-1. Top View

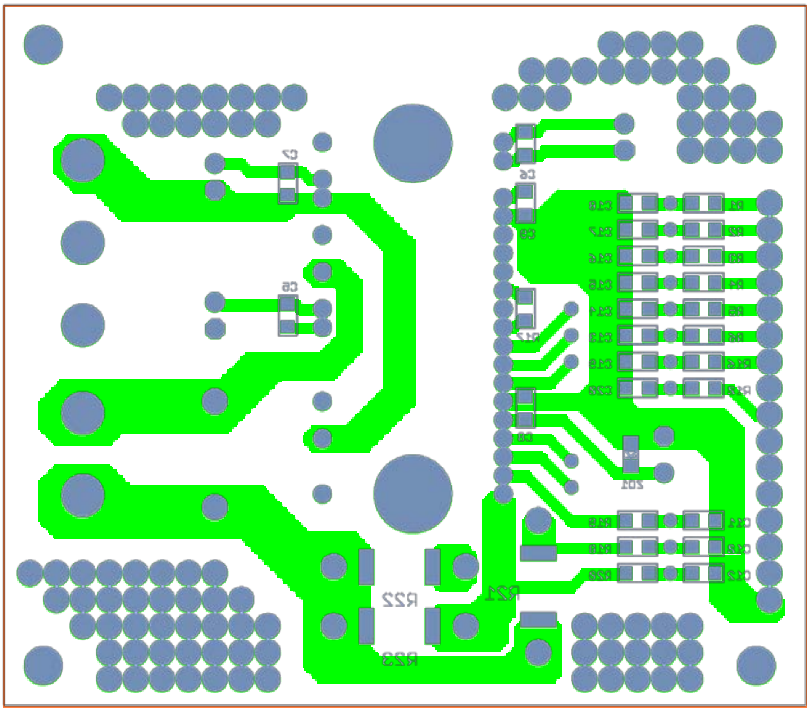


Figure 16-2. Bottom View

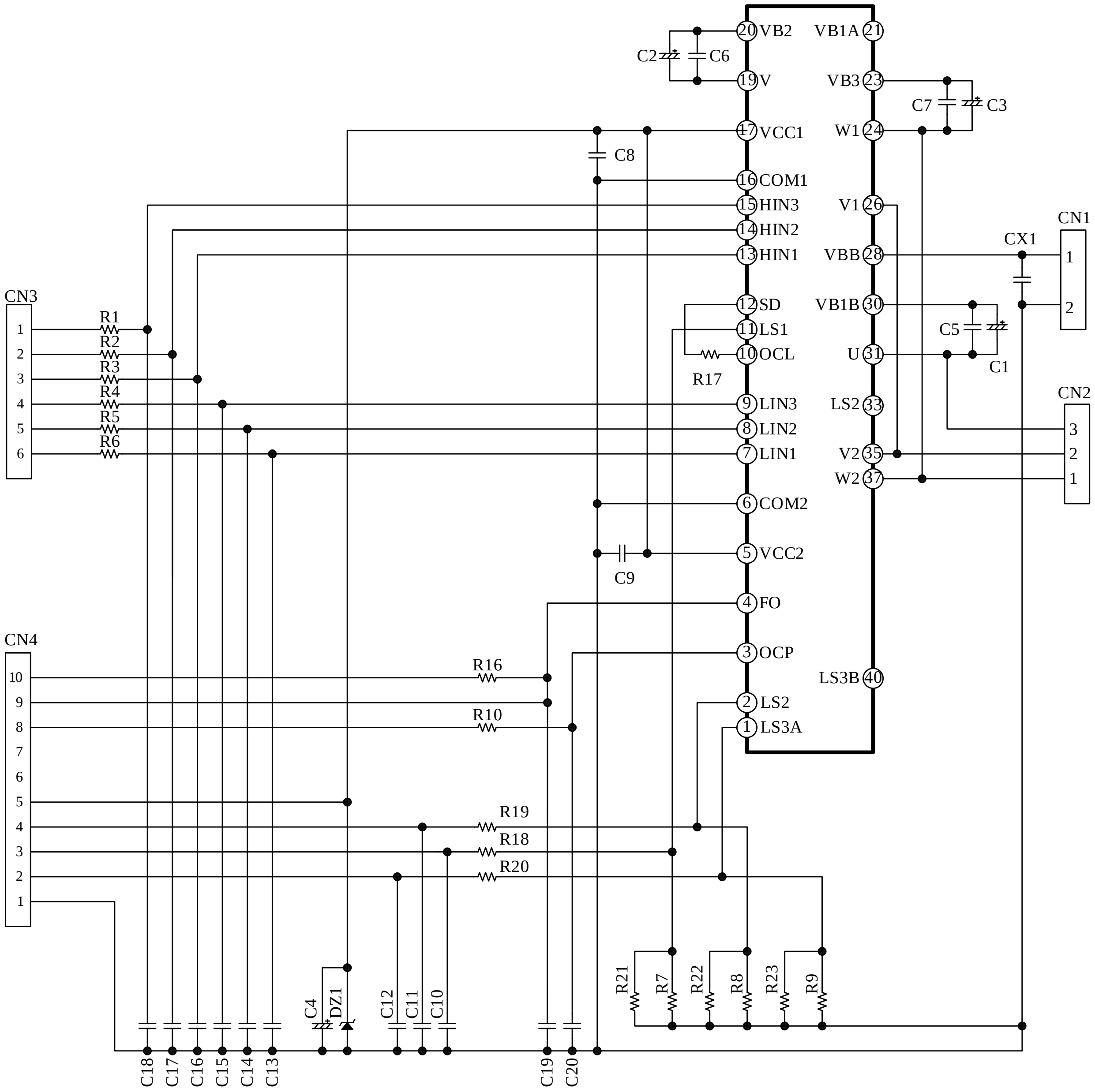


Figure 16-3. Circuit Diagram of PCB Pattern Layout Example

17. Typical Motor Driver Application

This section contains information on the typical motor driver application listed in the previous section, including a circuit diagram, specifications, and the bill of the materials used.

- **Motor Driver Specifications**

IC	SIM6822M
Main Supply Voltage, V_{DC}	300 VDC (typ.)
Rated Output Power	500 W

- **Circuit Diagram**

  See Figure 16-3.

- **Bill of Materials**

Symbol	Part Type	Ratings	Symbol	Part Type	Ratings
C1	Electrolytic	47 µF, 50 V	R3	General	100 Ω, 1/8W
C2	Electrolytic	47 µF, 50 V	R4	General	100 Ω, 1/8W
C3	Electrolytic	47 µF, 50 V	R5	General	100 Ω, 1/8W
C4	Electrolytic	100 µF, 50 V	R6	General	100 Ω, 1/8W
C5	Ceramic	0.1 µF, 50 V	R7*	Metal plate	0.15 Ω, 2W
C6	Ceramic	0.1 µF, 50 V	R8*	Metal plate	0.15 Ω, 2W
C7	Ceramic	0.1 µF, 50 V	R9*	Metal plate	0.15 Ω, 2W
C8	Ceramic	0.1 µF, 50 V	R10	General	100 Ω, 1/8W
C9	Ceramic	0.1 µF, 50 V	R16	General	3.3 kΩ, 1/8W
C10	Ceramic	100 pF, 50 V	R17	General	0 kΩ, 1/8W
C11	Ceramic	100 pF, 50 V	R18	General	100 Ω, 1/8W
C12	Ceramic	100 pF, 50 V	R19	General	100 Ω, 1/8W
C13	Ceramic	100 pF, 50 V	R20	General	100 Ω, 1/8W
C14	Ceramic	100 pF, 50 V	R21	General	Open
C15	Ceramic	100 pF, 50 V	R22	General	Open
C16	Ceramic	100 pF, 50 V	R23	General	Open
C17	Ceramic	100 pF, 50 V	ZD1	Zener diode	V_Z = 21 V (max.)
C18	Ceramic	100 pF, 50 V	IPM1	IC	SIM6822M
C19	Ceramic	0.01 µF, 50 V	CN1	Pin header	Equiv. to B2P3-VH
C20	Ceramic	100 pF, 50 V	CN2	Pin header	Equiv. to B2P5-VH
CX1	Film	0.033 µF, 630 V	CN3	Connector	Equiv. to MA06-1
R1	General	100 Ω, 1/8W	CN4	Connector	Equiv. to MA10-1
R2	General	100 Ω, 1/8W			

* Refers to a part that requires adjustment based on operation performance in an actual application.

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