

Telecom

Power supply

Power conditioner system

# **FMP30N60S1**

#### **FUJI POWER MOSFET**

## **Super J-MOS series**

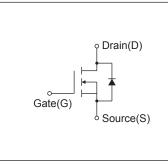
### N-Channel enhancement mode power MOSFET

Features	Outline Drawings [mm]			
Low on-state resistance Low switching loss easy to use (more controllabe switching dV/dt by Rg)				
Applications				
UPS Server				

JEDEC : TO-220AB

PRE-SOLDER





#### Absolute Maximum Ratings at Tc=25°C (unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks
Drain Source Voltage	V <sub>DS</sub>	600	V	
Drain-Source Voltage	VDSX	600	V	V <sub>GS</sub> =-30V
Continuous Drain Current		±30	А	Tc=25°C Note*1
Continuous Drain Current	ID	±19	А	Tc=100°C Note*1
Pulsed Drain Current	DP	±90	А	
Gate-Source Voltage	V <sub>GS</sub>	±30	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	lar	6.6	А	Note *2
Non-Repetitive Maximum Avalanche Energy	Eas	849.2	mJ	Note *3
Maximum Drain-Source dV/dt	dV <sub>DS</sub> /dt	50	kV/µs	V <sub>DS</sub> ≤ 600V
Peak Diode Recovery dV/dt	dV/dt	12	kV/µs	Note *4
Peak Diode Recovery -di/dt	-di/dt	100	A/µs	Note *5
Maximum Bawar Disainstian		2.02	W	T₂=25°C
Maximum Power Dissipation	PD	250	vv	Tc=25°C
On another and Changes Temporature range	Tch	150	°C	
Operating and Storage Temperature range	Tstg	-55 to +150	°C	

Note \*1 : Limited by maximum channel temperature. Note \*2 : T<sub>ch</sub>≤150°C, See Fig.1 and Fig.2 Note \*3 : Starting T<sub>ch</sub>=25°C, I<sub>As</sub>=4A, L=97.3mH, V<sub>DD</sub>=60V, R<sub>G</sub>=50Ω, See Fig.1 and Fig.2 E<sub>AS</sub> limited by maximum channel temperature and avalanche current. Note \*4 : I<sub>F</sub>≤-I<sub>D</sub>, -di/dt=100A/μs, V<sub>DD</sub>≤400V, T<sub>ch</sub>≤150°C. Note \*5 : I<sub>F</sub>≤-I<sub>D</sub>, dV/dt=12kV/μs, V<sub>DD</sub>≤400V, T<sub>ch</sub>≤150°C.

#### Electrical Characteristics at Tc=25°C (unless otherwise specified) Static Ratings

Description	Symbol	Conditions		min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	I₀=250µA V₀s=0V		600	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	I <sub>D</sub> =250μA V <sub>DS</sub> =V <sub>GS</sub>		2.5	3.0	3.5	V
Zero Gate Voltage Drain Current	loss	V <sub>DS</sub> =600V V <sub>GS</sub> =0V	T <sub>ch</sub> =25°C	-	-	25	-μA
		V <sub>DS</sub> =480V V <sub>GS</sub> =0V	T <sub>ch</sub> =125°C	-	-	250	
Gate-Source Leakage Current	lass	V <sub>GS</sub> = ±30V V <sub>DS</sub> =0V		-	10	100	nA
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	I <sub>D</sub> =15A V <sub>GS</sub> =10V		-	0.106	0.125	Ω
Gate resistance	RG	f=1MHz, open drain		-	3.2	-	Ω

#### Dynamic Ratings

Description	Symbol	Conditions	min.	typ.	max.	Unit
Forward Transconductance	<b>g</b> fs	I <sub>D</sub> =15A V <sub>DS</sub> =25V	13	26	-	S
Input Capacitance	Ciss	V <sub>DS</sub> =10V	-	2200	-	
Output Capacitance	Coss	V <sub>GS</sub> =0V	-	4670	-	
Reverse Transfer Capacitance	Crss	f=1MHz	-	430	-	
Effective output capacitance, energy related (Note *6)	C <sub>o(er)</sub>	V <sub>GS</sub> =0V V <sub>DS</sub> =0480V	-	127	-	pF
Effective output capacitance, time related (Note *7)	C <sub>o(tr)</sub>	V <sub>GS</sub> =0V V <sub>DS</sub> =0480V ID=constant	-	450	-	
Turne Ore Time	t <sub>d(on)</sub>	V <sub>DD</sub> =400V, V <sub>GS</sub> =10V I <sub>D</sub> =15A, R <sub>G</sub> =13Ω See Fig.3 and Fig.4	-	31	-	ns
Turn-On Time	tr		-	57	-	
Trum Off Time	t <sub>d(off)</sub>		-	136	-	
Turn-Off Time	tr See Fig.3 and Fig.4		-	17	-	
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> =480V, I <sub>D</sub> =30A V <sub>GS</sub> =10V See Fig.5	-	73	-	nC
Gate-Source Charge	Q <sub>GS</sub>		-	18	-	
Gate-Drain Charge	Q <sub>GD</sub>		-	25	-	
Drain-Source crossover Charge	Qsw		-	11.5	-	1

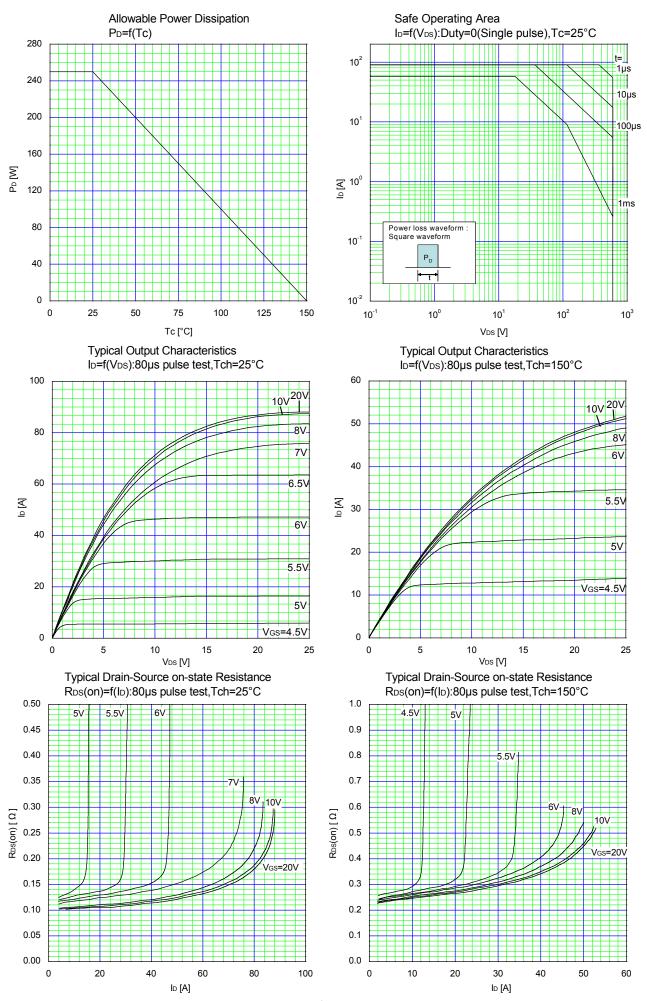
Note \*6 :  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{Ds}$  is rising from 0 to 80% BV<sub>DSS</sub>. Note \*7 :  $C_{o(tr)}$  is a fixed capacitance that gives the same charging times as  $C_{oss}$  while  $V_{Ds}$  is rising from 0 to 80% BV<sub>DSS</sub>.

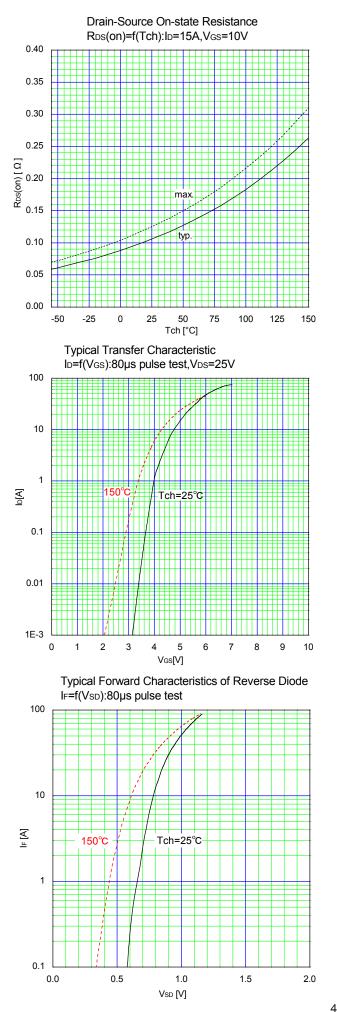
#### Reverse Diode

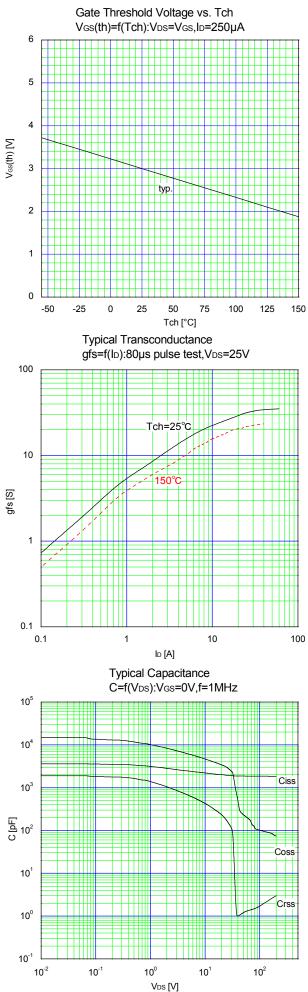
Description	Symbol	Conditions	min.	typ.	max.	Unit
Avalanche Capability	lav	L=21.7mH, Tch=25°C See Fig.1 and Fig.2	6.6	-	-	А
Diode Forward On-Voltage	V <sub>SD</sub>	I⊧=30A, V₀s=0V T₀h=25°C	-	0.9	1.35	V
Reverse Recovery Time	trr	IF=30A, VGS=0V	-	430	-	ns
Reverse Recovery Charge	Qrr	∇₀D=400V -di/dt=100A/μs T₅b=25°C	-	8.6	-	μC
Peak Reverse Recovery Current	Ігр	See Fig.6	-	38	-	А

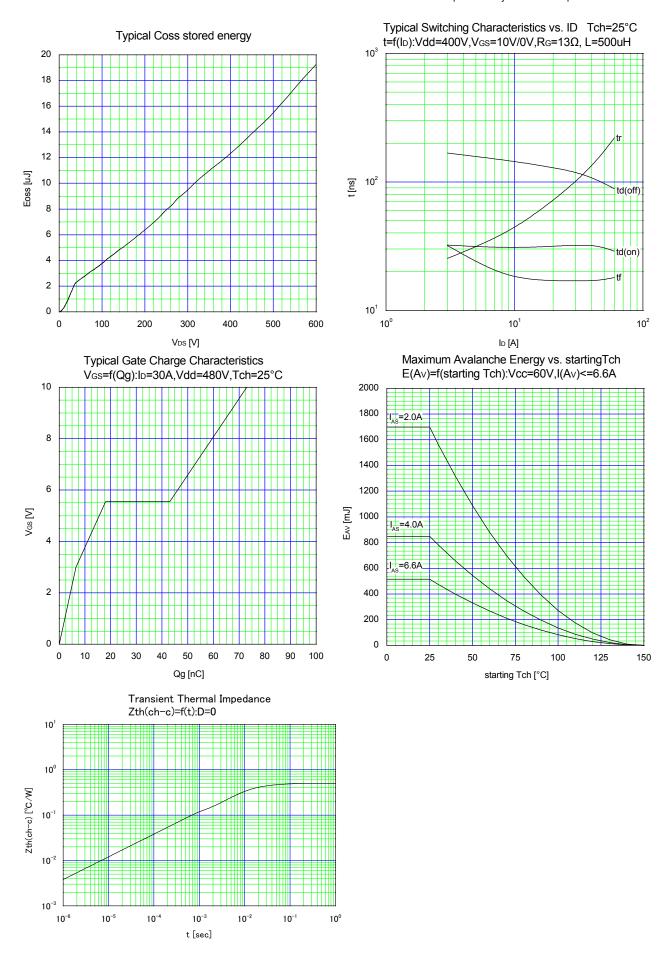
#### Thermal Characteristics

Description	Symbol	min.	typ.	max.	Unit
Channel to Case	Rth(ch-c)	-	-	0.5	°C/W
Channel to Ambient	R <sub>th(ch-a)</sub>	-	-	62	°C/W









VGS

VDS

DI ID

BVDSS

http://www.fujielectric.com/products/semiconductor/

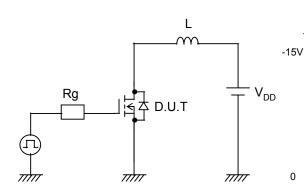
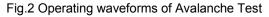


Fig.1 Avalanche Test circuit



IAV

+10V

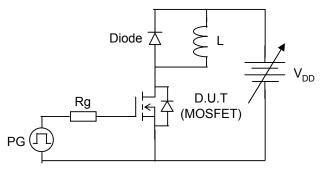


Fig.3 Switching Test circuit

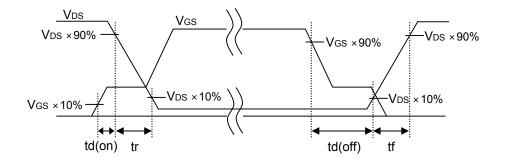


Fig.4 Operating waveform of Switching Test

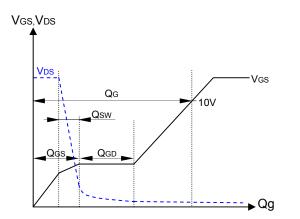
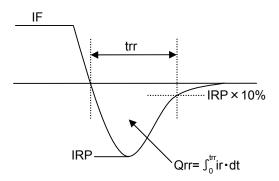
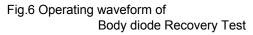


Fig.5 Operating waveform of Gate charge Test

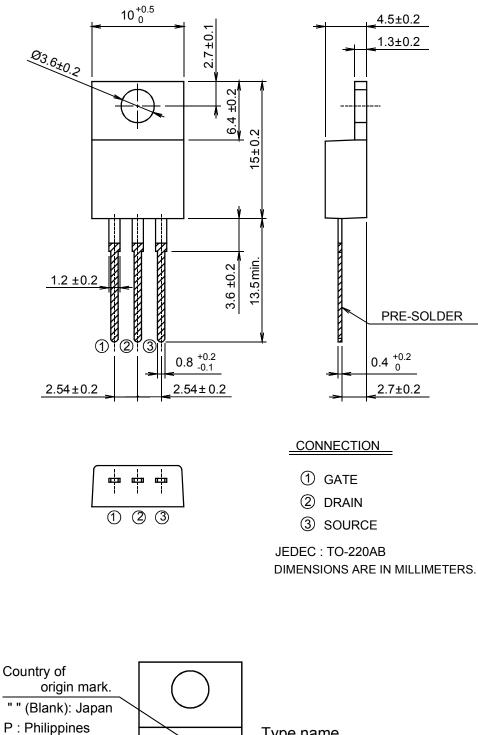


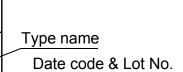


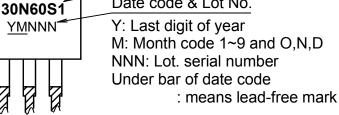
Marking

http://www.fujielectric.com/products/semiconductor/

#### Outview: TO-220 Package







\* The font (font type,size) and the trademark-size might be actually different.

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Trademark

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