

# **FQB4N80 / FQI4N80**

## **N-Channel QFET® MOSFET**

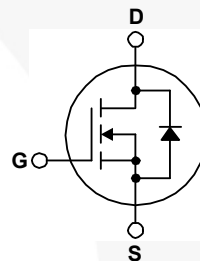
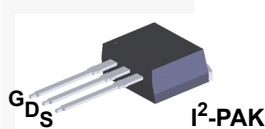
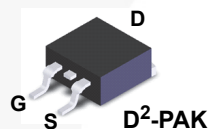
**800 V, 3.9 A, 3.6 Ω**

### **Description**

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### **Features**

- 3.9 A, 800 V,  $R_{DS(on)} = 3.6 \Omega$  (Max.) @  $V_{GS} = 10 V$ ,  $I_D = 1.95 A$
- Low Gate Charge (Typ. 19 nC)
- Low  $C_{rss}$  (Typ. 8.6 pF)
- 100% Avalanche Tested



### **Absolute Maximum Ratings** $T_C = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	FQB4N80TM / FQI4N80TU	Unit
$V_{DSS}$	Drain-Source Voltage	800	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ C$ )	3.9	A
	- Continuous ( $T_C = 100^\circ C$ )	2.47	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	15.6	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	460	mJ
$I_{AR}$	Avalanche Current (Note 1)	3.9	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	13	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	4.0	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ C$ ) *	3.13	W
	Power Dissipation ( $T_C = 25^\circ C$ )	130	W
	- Derate above $25^\circ C$	1.04	W/ $^\circ C$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ C$

### **Thermal Characteristics**

Symbol	Parameter	FQB4N80TM / FQI4N80TU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.96	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> pad of 2 oz copper), Max.	40	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQB4N80TM	FQB4N80	D <sup>2</sup> -PAK	Tape and Reel	330 mm	24 mm	800 units
FQI4N80TU	FQI4N80	I <sup>2</sup> -PAK	Tube	N/A	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	800	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.95	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	$\mu\text{A}$
		$V_{DS} = 640\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 1.95\text{ A}$	--	2.8	3.6	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 1.95\text{ A}$	--	3.8	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	680	880	pF
$C_{oss}$	Output Capacitance		--	75	100	pF
$C_{rss}$	Reverse Transfer Capacitance		--	8.6	12	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 3.9\text{ A},$ $R_G = 25\text{ }\Omega$	--	16	40	ns
$t_r$	Turn-On Rise Time		--	45	100	ns
$t_{d(off)}$	Turn-Off Delay Time		--	35	80	ns
$t_f$	Turn-Off Fall Time	(Note 4)	--	35	80	ns
$Q_g$	Total Gate Charge	$V_{DS} = 640\text{ V}, I_D = 3.9\text{ A},$ $V_{GS} = 10\text{ V}$	--	19	25	nC
$Q_{gs}$	Gate-Source Charge		--	4.2	--	nC
$Q_{gd}$	Gate-Drain Charge	(Note 4)	--	9.1	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	3.9	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	15.6	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 3.9 A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 3.9 A, dI <sub>F</sub> / dt = 100 A/μs	--	575	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	3.65	--	μC

#### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 57\text{ mH}, I_{AS} = 3.9\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 3.9\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Essentially independent of operating temperature

## Typical Characteristics

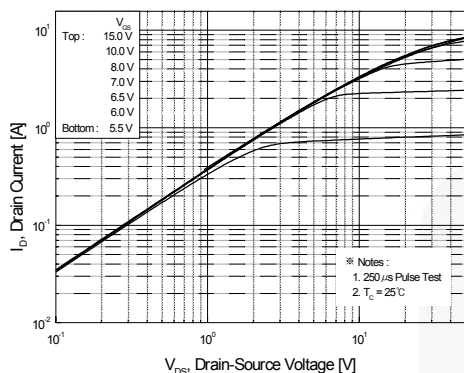


Figure 1. On-Region Characteristics

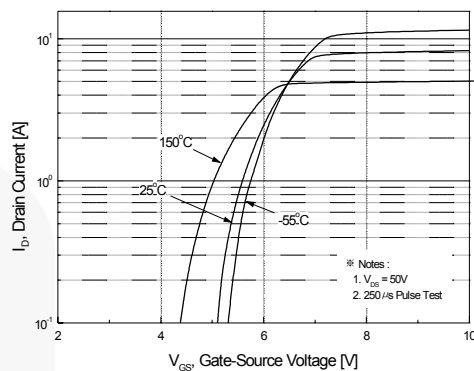


Figure 2. Transfer Characteristics

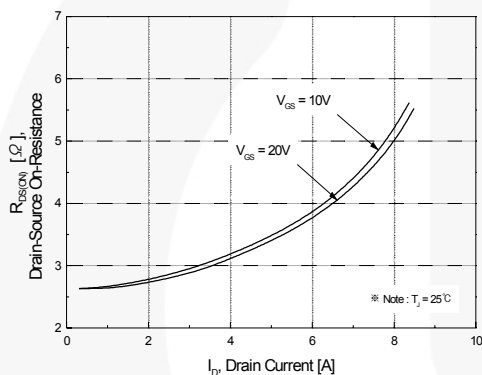


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

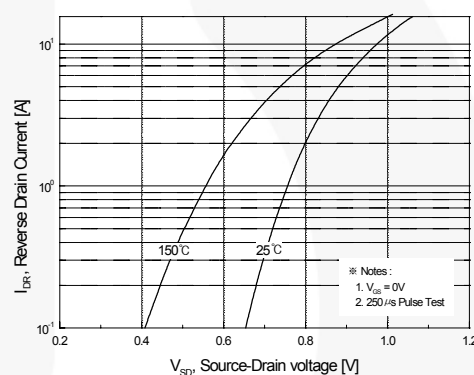


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

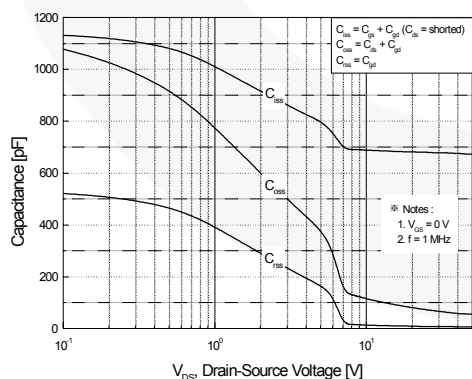


Figure 5. Capacitance Characteristics

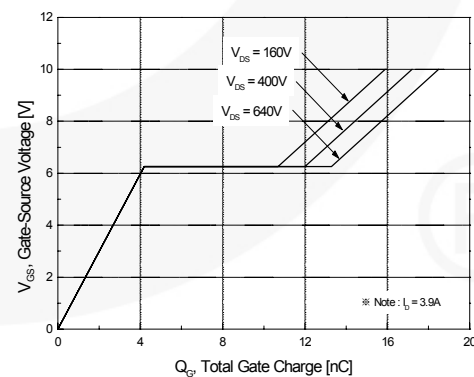
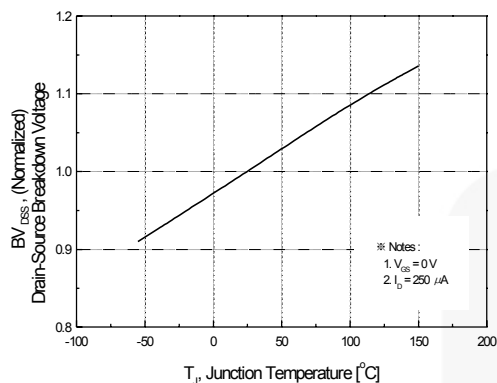
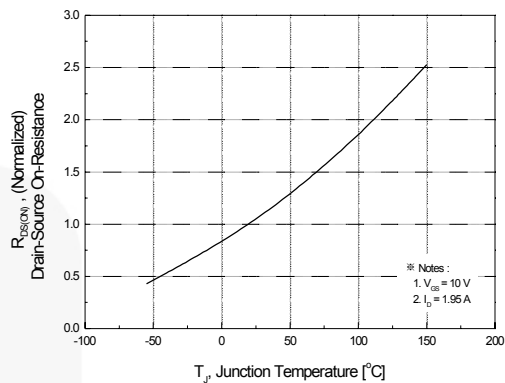


Figure 6. Gate Charge Characteristics

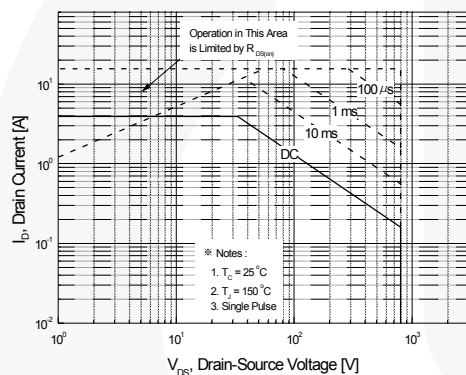
## Typical Characteristics (Continued)



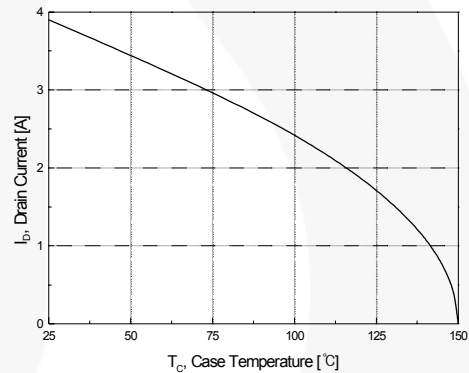
**Figure 7. Breakdown Voltage Variation vs. Temperature**



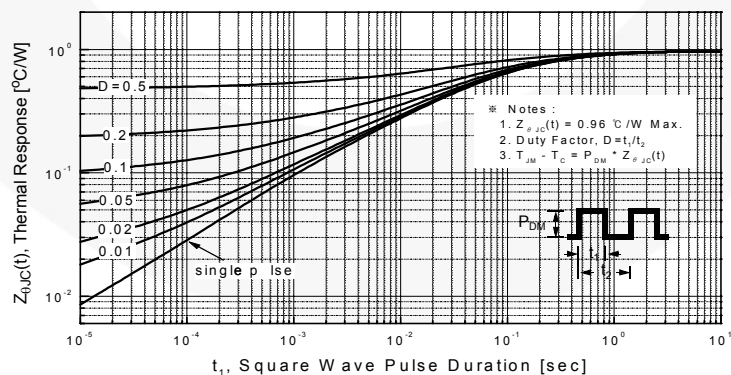
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

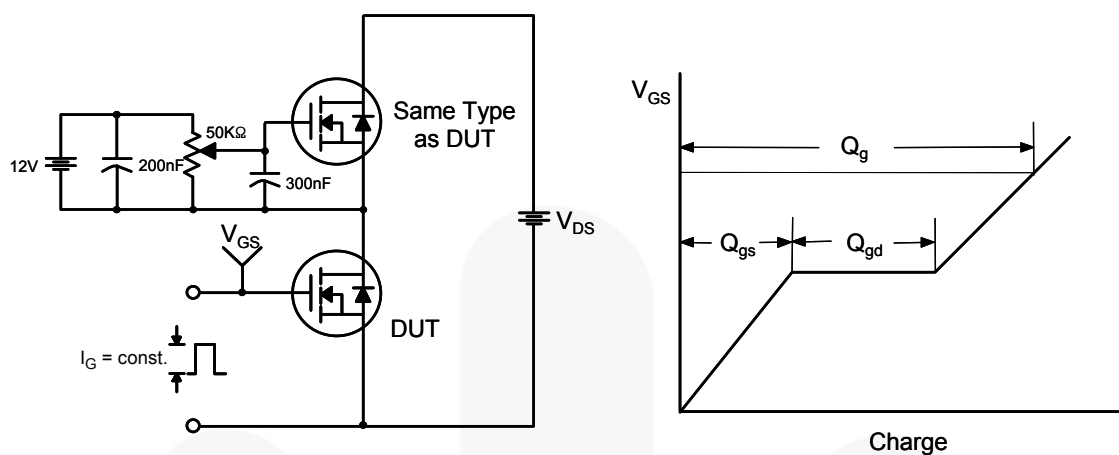


Figure 12. Gate Charge Test Circuit & Waveform

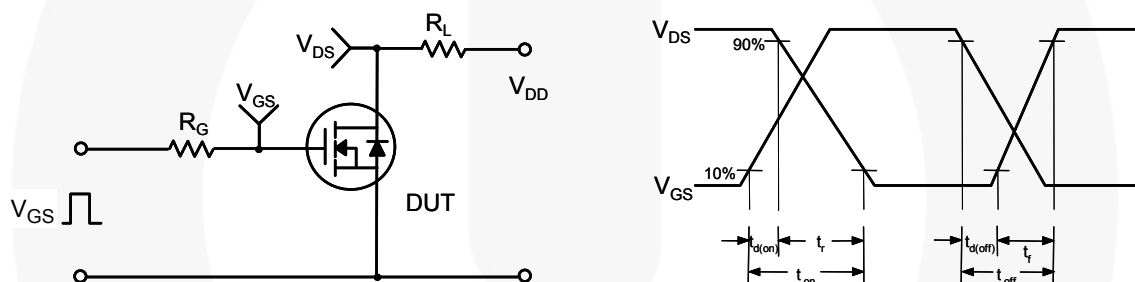


Figure 13. Resistive Switching Test Circuit & Waveforms

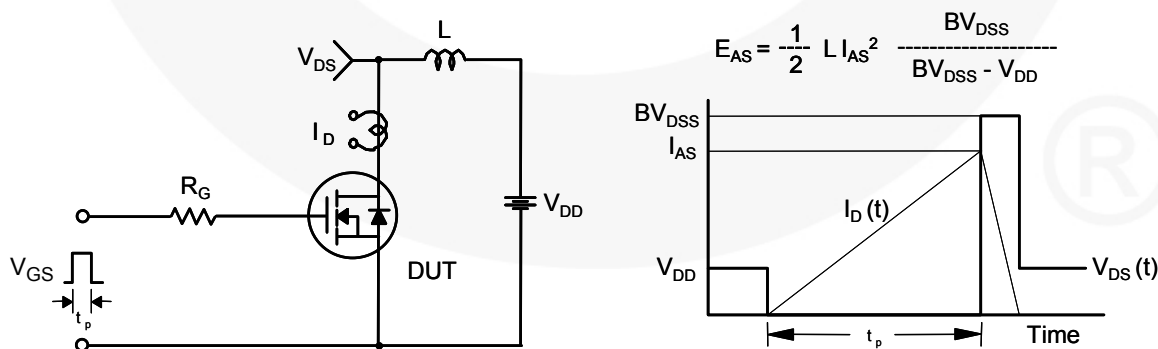


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

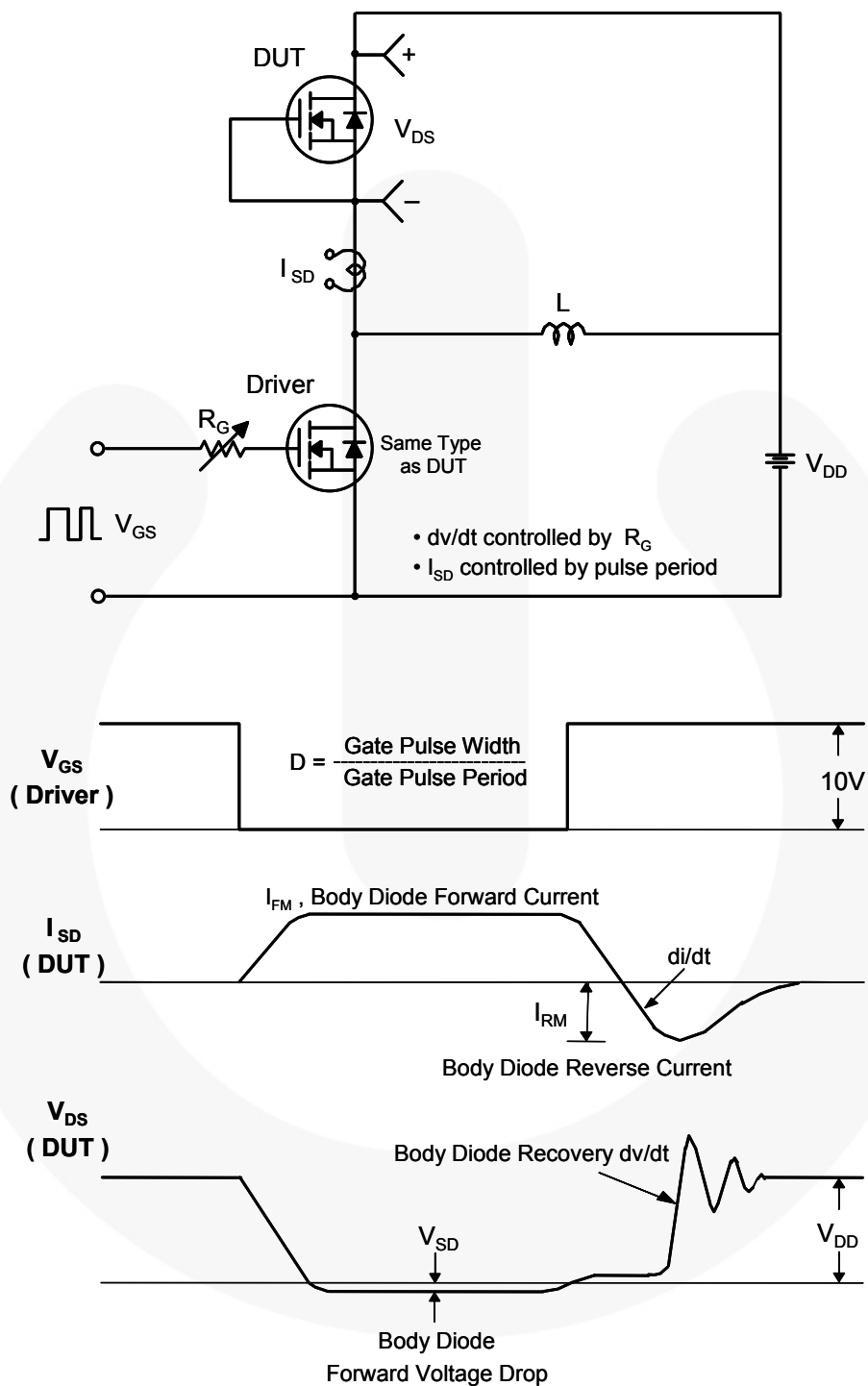
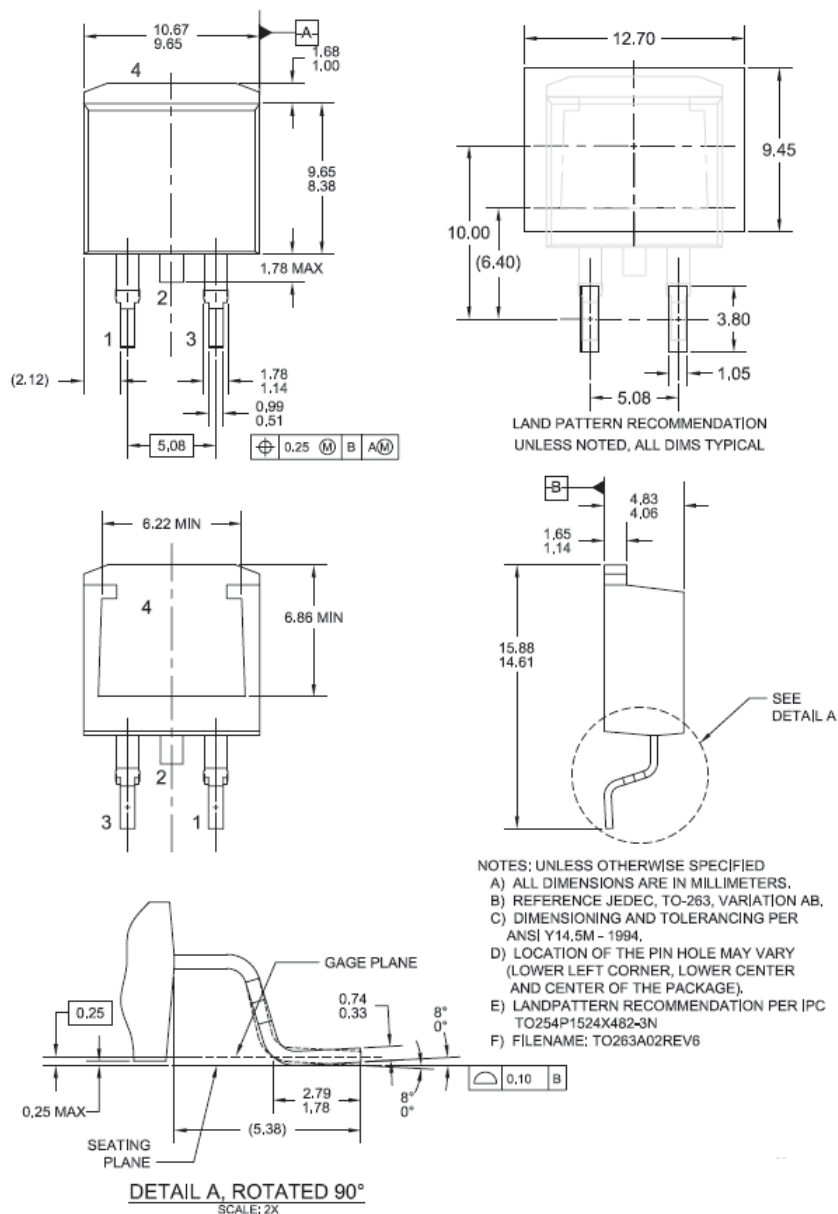


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions

### TO-263 2L (D<sup>2</sup>PAK)



**Figure 16. 2LD, TO263, Surface Mount**

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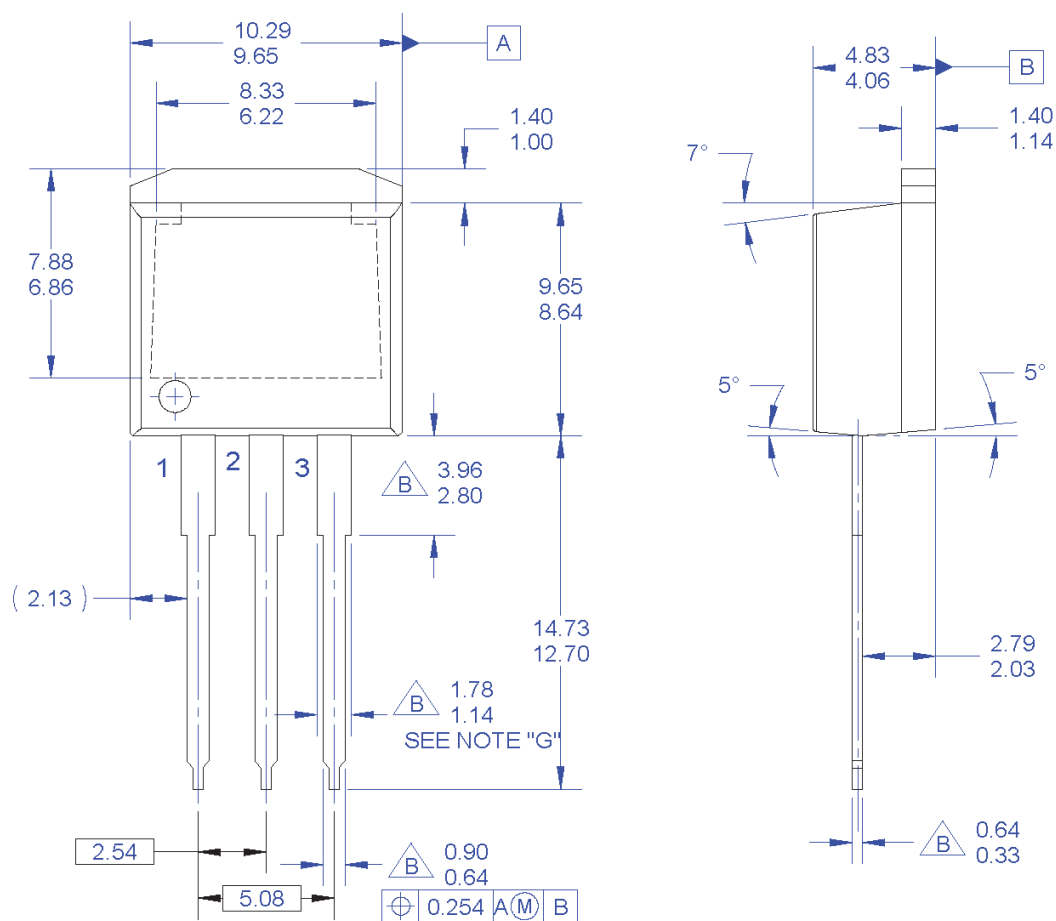
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Dimension in Millimeters

## Mechanical Dimensions

### TO-262 3L (I<sup>2</sup>PAK)



#### NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
- B. DOES NOT COMPLY JEDEC STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
- F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
- G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.
- H. DRAWING FILE NAME: TO262A03REV5

**Figure 17. 3LD, TO262, Jedec Variation AA (I<sup>2</sup>PAK)**

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Dimension in Millimeters





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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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