

HIGH POWER FACTOR FLYBACK PWM CONTROLLER

DESCRIPTION

SD7530 is a high power factor flyback PWM controller special for LED lighting applications.

SD7530 features a high performance analog multiplier for power factor correction (PFC), zero current detector (ZCD) to ensure TM operation. It integrates a current sensing comparator with built-in leading-edge blanking, and a totem-pole output stage capable of -600mA /800mA current suited for big MOSFET.

SD7530 has a built-in soft-start circuit to avoid the over voltage output under light load start, reduce MOSFET's voltage stress, and improve circuit's reliability.

SD7530 has a built-in output short-circuit protection circuit, in this way the current of the system is considerably reduced to avoid the APPLICATIONS damage to IC.

SD7530 includes V_{cc} under voltage lockout, V_{cc} over voltage protection, and over temperature protection, etc.



* LED Daylight lamp

FEATURES

- * Transition Mode (TM) operation
- * High-performance analog multiplier
- Built-in restart timer
- Integrate digital LEB
- Low start-up current (5µA)
- Audio noise free
- * Built-in soft start circuit
- Very low power dissipation of output short-circuit protection (SCP)
- * V_{CC} under vltage lockout with hysteresis (UVLO)
- V_{CC} over-voltage protection (VCCOVP)
- * Over temperature protection (OTP)

ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SD7530S	SOP-8-225-1.27	SD7530S	Halogen free	Tube
SD7530STR	SOP-8-225-1.27	SD7530S	Halogen free	Tape&Reel





BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Rating	Unit
Supply voltage (I _{CC} <20mA)	Vcc	40	V
Peak drive output current	I _{OH} /I _{OL}	-600/800	mA
Voltage on analog input and output pins	-	-0.3 ~ 8	V
Maximum current of zero current detector	-	±10	mA
Power dissipation (ambient temperature: 50°C)	P _{diss}	0.65	W
Operating temperature range	T _{amb}	-40~+120	°C
Storage temperature range	T _{stg}	-55~+150	°C
Junction temperature	Tj	+150	°C
Thermal resistance from chip surface to the ambient	R _{th(j-a)}	150	°C/W °C/W

ELECTRICAL CHARACTERISTICS(Unless otherwise stated, V_{CC}=22V; C_O=1nF; -25°C<T_{amb}<125°C)

Characteristics	Symbol	Test condition	Min.	Тур.	Max.	Unit
Power supply						
Operating voltage range	V _{cc}	After start-up	10.5		32	V
Turn-on threshold	V _{CCon}	*	16.5	17.5	18.5	V
Turn-off threshold	V _{CCoff}	*	8.0	9.0	10.0	V
Hysteresis voltage	V _{CChys}			8.5		V



$\begin{array}{c c c c c c c } Clamp voltage V_z & lcc=20mA & & 40 & & V \\ VCC OVP VCC_{Orp} VCC_{Orp} & 32 & 34 & 36 & V \\ \hline \begin{timestrmatric}{ c c c c c c c c c c c c c c c c c c $	Characteristics	Symbol	Test condition	Min.	Тур.	Max.	Unit	
Supply current Start current Isr Before start-up, $V_{CC}=15V$ 5 10 μ A Quiescent current Ic No switch 4 6 mA Operating current Ic F70KHz 5 7 MA Multiplier VMLT Uncar operation range 0-3 V Gain ** K VMLT = 0 - 4V 0.32 0.38 0.44 1/V Gain ** K VMLT = 0 - 4V 0.32 0.38 0.44 1/V Maximum output slope $\frac{\Delta V_{CS}}{\Delta V_{MULT}}V_{NLT}=0 - 1V 0.32 0.38 0.44 1/V Maximum output slope \frac{\Delta V_{CS}}{\Delta V_{MULT}}V_{NUT}=0 - 1V 0.32 0.38 0.44 1/V Instrument V VCOME=BESC 2.45 2.5 5.5 MV Interstoold V VCOME = 0.5V < V_GC < 32V *$	Clamp voltage	Vz	I _{cc} =20mA		40		V	
Supply current Start current Isr Before start-up, $V_{CC}=15V$ 5 10 μ A Quiescent current Ic No switch 4 6 mA Operating current Ic F70KHz 5 7 MA Multiplier VMLT Uncar operation range 0-3 V Gain ** K VMLT = 0 - 4V 0.32 0.38 0.44 1/V Gain ** K VMLT = 0 - 4V 0.32 0.38 0.44 1/V Maximum output slope $\frac{\Delta V_{CS}}{\Delta V_{MULT}}V_{NLT}=0 - 1V 0.32 0.38 0.44 1/V Maximum output slope \frac{\Delta V_{CS}}{\Delta V_{MULT}}V_{NUT}=0 - 1V 0.32 0.38 0.44 1/V Instrument V VCOME=BESC 2.45 2.5 5.5 MV Interstoold V VCOME = 0.5V < V_GC < 32V *$	VCC OVP	VCCovp		32	34	36	V	
Quiescent current Ic No switch 4 6 mA Operating current Ic f=70kHz 5 7 mA Multiplier Input bias current Incurrent VMULT C 5 7 mA Input voltage range VMULT Unear operation range 0-3 V Gain ** K VMULT= 0 - 4V 0.32 0.38 0.44 1/V Gain ** K VMULT= 0 - 1V 0.32 0.38 0.44 1/V Gain ** K VMULT= 0 - 1V 1.0 1.1 V/V Error amplifier Verent 10,5/ <vcc *<="" td="" x32v=""> 2.44 2.56 V Linear regulation - Vcc = 0.5/V - 32V 2 5 mV Input bias current Inv Viev = 0 - 3V 1 MHz Source current Icom# Vcc = 0.5/N - 3V 1 MH</vcc>	Supply current							
Operating current Icc f=70 Hz 5 7 mA Multiplier Input bias current Input. VMULT = 0 - 4V V Gain ** K VMULT = 1 /v, V_COMP=4V 0.32 0.38 0.44 1/V Maximum output slope ΔV_{CS} $\Delta W_{LT} = 0 + V$ 0.32 0.38 0.44 1/V Maximum output slope ΔV_{CS} $\Delta W_{LT} = 0 + V$ 0.02 0.38 0.44 1/V Maximum output slope ΔV_{CS} $\Delta V_{MULT} = 0 + V$ 0.02 2.55 V Error amplifier V_{REF} $T_{ares} = 25^{\circ}C$ 2.45 2.5 N Input bias current I_{NV} $V_{REF} = 0.5V - 32V$ 2 5 mV Input bias current I_{NV} $V_{REF} = 0.3V$ 1 1 MHz Source current I_{SW} Open loop 60 80 dB Gain bandwidth product G_E	Start current	I _{ST}	Before start-up, V _{CC} =15V		5	10	μA	
Multiplier Input bias current Isource Value T = 0 - 4V 1 μA Input voltage range VMULT Linear operation range 0-3 V Gain ** K Value T=1V, Vcowe=4V 0.32 0.38 0.44 1/V Maximum output slope ΔV_{CS} $V_{MULT}=0 - 1V$ 1.0 1.1 V/V Error amplifier Voltage feedback input V_{REF} $T_{amb}=25^{\circ}C$ 2.45 2.5 2.56 V Linear regulation - Vcc = 10.5V - 32V 2 5 mV Input bias current Inv VRV of a - 3V 1 μA Voltage gain Gv Open loop 60 80 dB Source current Iccomp Vcowe=4V, Vsv=2.4V -2 -3.5 -5 mA Sink current Iccomp Vcowe=4V, Vsv=2.6V 4 5.5 7 mA Upper clamp voltag	Quiescent current	lq	No switch		4	6	mA	
$\begin{array}{c c c c c c c } \mbox{Input bias current} & Inpu$	Operating current	Icc	f=70kHz		5	7	mA	
$ \begin{array}{ c c c c c c c } \mbox{Ind} $	Multiplier	-		_				
Gain ** K VMULT VCOMP 0.32 0.38 0.44 1/V Maximum output slope $\frac{\Delta V_{CS}}{\Delta V_{MULT}}$ VMULT VMULT 1.0 1.1 V/V Error amplifier V_{REF} $T_{arms}=25^{\circ}C$ 2.45 2.5 2.55 V Linear regulation - V_{RCF} 10.5V < V_{CC} <32V *	Input bias current	I _{MULT}	$V_{MULT} = 0 \sim 4V$			-1	μA	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Input voltage range	V _{MULT}	Linear operation range	0~3			V	
Maximum output slope $\overline{\Delta V_{MULT}}$ $V_{COMP=Upper clamp voltage 1.0 1.1 V/V Error amplifier V_{REF} T_{anb}=25^{\circ}C 2.45 2.5 2.55 V Linear regulation - V_{CC} = 10.5V < V_{CC} < 32V * 2.44 2.56 V Input bias current I_{INV} V_{RV} = 0 ~ 3V - - 1 \mu A Voltage gain G_V Open loop 60 80 dB Gain bandwidth product G_B 1 MHz Source current I_{COMP} V_{COMP=4V, V_{INV}=2.4V -2 -3.5 -5 mA Sink current I_{COMP} V_{COMP}=4V, V_{INV}=2.6V 4 5.5 7 mA Upper clamp voltage V_{COMP} I_{Source}=0.5mA 5.0 6.0 6.5 V Lower clamp voltage V_{CSM} I_{Source}=0.5mA 2.0 2.25 2.4 V Current sense comparator$	Gain **	к	V _{MULT} =1V, V _{COMP} =4V	0.32	0.38	0.44	1/V	
	•• • • • •		V _{MULT} =0 ~ 1V					
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Maximum output slope	ΔV_{MULT}	V _{COMP} =upper clamp voltage	1.0	1.1		V/V	
threshold V_{REF} $10.5V < V_{CC} < 32V^*$ 2.44 2.56 V Linear regulation $V_{CC} = 10.5V - 32V$ 2 5 mV Input bias current I_{INV} $V_{INV} = 0 - 3V$ $$	Error amplifier	-		_				
threshold Nm 10.5V< V_{CC} -32V * 2.44 2.56 Linear regulation - V_{CC} -10.5V- 32V 2 5 mV Input bias current I_{INV} $V_{INV} = 0$ -3V 1 μA Voltage gain G_V Open loop 60 80 dB Gain bandwidth product G_B 1 MHz Source current I_{COMP} $V_{COMP=4V, V_{INV}=2.4V$ -2 -3.5 -5 mA Sink current I_{COMP} $V_{COMP=4V, V_{INV}=2.6V$ 4 5.5 7 mA Upper clamp voltage V_{COMP} $I_{source}=0.5mA$ 5.0 6.0 6.5 V Lower clamp voltage V_{COMP} $I_{source}=0.5mA$ 5.0 6.0 6.5 V Lower clamp voltage V_{COMP} $I_{source}=0.5mA$ 5.0 6.0 6.5 V Lower clamp voltage V_{COMP} $I_{source}=0.5mA$ 5.0 1.0 1.08 1.16 V Current sense clamp	Voltage feedback input		T _{amb} =25°C	2.45	2.5	2.55	N	
$\begin{array}{ c c c c c c } \mbox{Input bias current} & I_{INV} & V_{INV} = 0 - 3V & & & &1 & \muA \\ \hline \begin{tabular}{ c c c c } \hline V_{Ottage gain} & G_V & Open loop & 60 & 80 & & dB \\ \hline \begin{tabular}{ c c c c } \hline & G_B & & & 1 & & MHz \\ \hline \begin{tabular}{ c c c c c } \hline & V_{COMP} = 4V, V_{INV} = 2.4V & -2 & -3.5 & -5 & mA \\ \hline \begin{tabular}{ c c c c c } \hline & V_{COMP} = 4V, V_{INV} = 2.4V & -2 & -3.5 & -5 & mA \\ \hline \begin{tabular}{ c c c c c c } \hline & V_{COMP} = 4V, V_{INV} = 2.6V & 4 & 5.5 & 7 & mA \\ \hline \begin{tabular}{ c c c c c c c } \hline & V_{COMP} = 4V, V_{INV} = 2.6V & 4 & 5.5 & 7 & mA \\ \hline \end{tabular}{ c c c c c c c c c c c c c c c c c c c$	threshold	V _{REF}	10.5V< V _{CC} <32V *	2.44		2.56	V	
$\begin{array}{c c c c c c c c c c c } \hline Voltage gain & G_V & Open loop & 60 & 80 & & dB \\ \hline Gain bandwidth product & G_B & & & & & & & & & & & & & & & & & & &$	Linear regulation	-	V _{CC} =10.5V~ 32V		2	5	mV	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Input bias current	I _{INV}	$V_{INV} = 0 \sim 3V$			-1	μA	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Voltage gain	Gv	Open loop	60	80		dB	
$ \begin{array}{c c c c c c } Sink current & I_{COMP} & V_{COMP}=4V, V_{INV}=2.6V & 4 & 5.5 & 7 & mA \\ Upper clamp voltage & V_{COMP} & I_{source}=0.5mA & 5.0 & 6.0 & 6.5 & V \\ Lower clamp voltage & V_{COMP} & I_{sink}=0.5mA & 2.0 & 2.0 & 2.25 & 2.4 & V \\ \hline \\ \hline \\ Current sense comparator & & & & & & & & & & & & & & & & & & &$	Gain bandwidth product	G _B			1		MHz	
$\begin{array}{ c c c c } Upper clamp voltage & V_{COMP} & I_{source}=0.5mA & 5.0 & 6.0 & 6.5 & V \\ Lower clamp voltage & V_{COMP} & I_{sink}=0.5mA * & 2.0 & 2.25 & 2.4 & V \\ \hline \\ \hline \\ \hline \\ Current sense comparator & & & & & & & & & & & & & & & & & & &$	Source current	ICOMP	V _{COMP} =4V, V _{INV} =2.4V	-2	-3.5	-5	mA	
$\begin{tabular}{ c c c c } \hline $Lower clamp voltage V_{COMP} $I_{sink}=0.5mA*$ $2.0 $2.25 $2.4 V \\ \hline $Current sense comparator V_{COMP} $I_{sink}=0.5mA*$ V_{COMP} V_{COMP} V_{COMP} V_{COMP} V_{COMP} V_{COMP} V_{COMP} V_{COMP} U_{COMP} V_{COMP} U_{DUPP} $Clamp V_{COMP} V_{COMP} U_{DUPP} $Clamp V_{COMP} V_{COMP} U_{DUPP} $Clamp V_{COMP} U_{DULT} V_{COMP} U_{DUPT} U_{COMP} U_{DUPT} U_{COMP} U_{DUPT} U_{COMP} U_{DUPT} U_{COMP} U_{DUPT} U_{COMP} U_{COMP} U_{DUPT} U_{COMP} U_{DUPT} U_{COMP} U_{DUPT} U_{COMP} U_{DUPT} U_{COMP} U_{DUPT} U_{DUPT} U_{COMP} U_{DUPT} U_{DUPT} U_{DUPT} U_{DUPT} U_{DUPT} U_{DUPT} U_{DUPT} U_{DUT} U_{COMP} U_{DUPT} U_{COMP} U_{DUPT} U_{COMP} U_{COM} U_{COMP} U_{COM} U_{COMP} U_{COM} U_{COMP} U_{COM} U_{COMP} U_{COM} U_{COMP} U_{COM} U_{C	Sink current	I _{COMP}	V _{COMP} =4V, V _{INV} =2.6V	4	5.5	7	mA	
$\begin{tabular}{ c c c c } \hline Current sense comparator $$V_{CS}=0V$ $$$$	Upper clamp voltage	V _{COMP}	I _{source} =0.5mA	5.0	6.0	6.5	V	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Lower clamp voltage	V _{COMP}	I _{sink} =0.5mA *	2.0	2.25	2.4	V	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Current sense comparat	or						
$ \begin{array}{c} \mbox{Current sense clamp} \\ \mbox{Current sense clamp} \\ \mbox{V}_{CS} \end{array} \begin{array}{c} \mbox{V}_{COMP}=Upper clamp} \\ \mbox{V}_{MULT}=1.5V \end{array} \end{array} \begin{array}{c} 1.0 \end{array} \begin{array}{c} 1.08 \end{array} \begin{array}{c} 1.16 \end{array} \end{array} \begin{array}{c} V \\ \mbox{I} \end{array} \end{array} \\ \mbox{V}_{MULT}=1.5V \end{array} \end{array} \begin{array}{c} \mbox{I} \end{array} \\ \mbox{V}_{MULT}=2.5V \end{array} \begin{array}{c} & 25 \end{array} \begin{array}{c} & & & & & & &$	Input bias current	I _{CS}	V _{CS} =0V			-1	μA	
$ \begin{array}{c} \mbox{Current sense clamp} & V_{CS} & V_{MULT}=1.5V & 1.0 & 1.08 & 1.16 & V \\ \hline & V_{MULT}=0V & & 25 & & \\ \hline & V_{MULT}=2.5V & & 5 & & \\ \hline & V_{MULT}=2.5V & & 5 & & \\ \hline & V_{MULT}=2.5V & & 5 & & \\ \hline & V_{MULT}=2.5V & & 2 & & \mu A \\ \hline & V_{CD} the bias current & I_{ZCD} & V_{ZCD}=1 ~ 4.5V & & 2 & & \mu A \\ \hline & V_{th(det)} & V_{th(det)} & V_{2CD} rise *** & & 1.1 & & V \\ \hline & V_{ZCD} fall *** & & 0.25 & & V \\ \hline & V_{Detect} hysteresis & HY(det) & *** & & 0.85 & & V \\ \hline & Upper clamp voltage & V_{ZCD} & I_{ZCD}=2.5mA & 6.3 & 6.8 & 7.3 & V \\ \hline & Lower clamp voltage & V_{ZCD} & I_{ZCD}=-2.5mA & -0.3 & 0 & 0.3 & V \\ \hline & Source current capability & I_{snk} & -2.5 & & & mA \\ \hline & Sink current capability & I_{snk} & 2.5 & & & mA \\ \hline & Restart timer \\ \hline \end{array}$	Delay to output	t _{d(H-L)}			200	400	ns	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Current sense clamp	V _{CS}		1.0	1.08	1.16	V	
Current sense offset V_{offset} $V_{MULT}=2.5V$ 5mVZero current detectorInput bias current I_{ZCD} $V_{ZCD}=1 \sim 4.5V$ 2 μA Detect threshold $V_{th(det)}$ V_{tcD} rise ***1.1VDetect hysteresisHY(det)***0.25VUpper clamp voltage V_{ZCD} $I_{ZCD}=2.5mA$ 6.36.87.3VLower clamp voltage V_{ZCD} $I_{ZCD}=2.5mA$ -0.300.3VSource current capability I_{src} mARestart timer I_{snk} 2.5mA					25			
Zero current detectorInput bias currentIzcD $V_{ZCD}=1 \sim 4.5V$ 2 μ ADetect threshold $V_{th(det)}$ V_{ZCD} rise ***1.1V $V_{th(det)}$ $V_{th(det)}$ V_{ZCD} fall ***0.25VDetect hysteresisHY(det)***0.85VUpper clamp voltage V_{ZCD} $I_{ZCD}=2.5mA$ 6.36.87.3VLower clamp voltage V_{ZCD} $I_{ZCD}=-2.5mA$ -0.300.3VSource current capability I_{src} mASink current capability I_{snk} 2.5mARestart timer	Current sense offset	V _{offset}			5		mV	
$ \begin{array}{c c c c c c c c c } \hline P_{Vth(det)} & V_{ZCD} \ rise ^{***} & & 1.1 & & V \\ \hline V_{ZCD} \ fall ^{***} & & 0.25 & & V \\ \hline Detect \ hysteresis & HY(det) & ^{***} & & 0.85 & & V \\ \hline Upper \ clamp \ voltage & V_{ZCD} & I_{ZCD} = 2.5mA & 6.3 & 6.8 & 7.3 & V \\ \hline Lower \ clamp \ voltage & V_{ZCD} & I_{ZCD} = 2.5mA & -0.3 & 0 & 0.3 & V \\ \hline Source \ current \ capability & I_{src} & -2.5 & & & mA \\ \hline Sink \ current \ capability & I_{snk} & & & mA \\ \hline Restart \ timer & $	Zero current detector							
$ \begin{array}{c c c c c c c c c } \hline P_{Vth(det)} & V_{ZCD} \ rise ^{***} & & 1.1 & & V \\ \hline V_{ZCD} \ fall ^{***} & & 0.25 & & V \\ \hline Detect \ hysteresis & HY(det) & ^{***} & & 0.85 & & V \\ \hline Upper \ clamp \ voltage & V_{ZCD} & I_{ZCD} = 2.5mA & 6.3 & 6.8 & 7.3 & V \\ \hline Lower \ clamp \ voltage & V_{ZCD} & I_{ZCD} = 2.5mA & -0.3 & 0 & 0.3 & V \\ \hline Source \ current \ capability & I_{src} & -2.5 & & & mA \\ \hline Sink \ current \ capability & I_{snk} & & & mA \\ \hline Restart \ timer & $		I _{ZCD}	V _{ZCD} =1 ~ 4.5V		2		μA	
Detect threshold Vth(det) VzcD fall *** 0.25 V Detect hysteresis HY(det) *** 0.85 V Upper clamp voltage VzcD IzcD=2.5mA 6.3 6.8 7.3 V Lower clamp voltage VzcD IzcD=2.5mA -0.3 0 0.3 V Source current capability Isrc -2.5 mA Sink current capability Isnk 2.5 mA Restart timer mA								
Detect hysteresis HY(det) *** 0.85 V Upper clamp voltage V _{ZCD} I _{ZCD} =2.5mA 6.3 6.8 7.3 V Lower clamp voltage V _{ZCD} I _{ZCD} =2.5mA -0.3 0 0.3 V Source current capability I _{src} -2.5 mA Sink current capability I _{snk} 2.5 mA Restart timer	Detect threshold	V _{th(det)}			0.25		V	
Upper clamp voltage V _{ZCD} I _{ZCD} =2.5mA 6.3 6.8 7.3 V Lower clamp voltage V _{ZCD} I _{ZCD} =-2.5mA -0.3 0 0.3 V Source current capability I _{src} -2.5 mA Sink current capability I _{snk} 2.5 mA Restart timer	Detect hysteresis	HY(det)					V	
Lower clamp voltage V _{ZCD} I _{ZCD} =-2.5mA -0.3 0 0.3 V Source current capability I _{src} -2.5 mA Sink current capability I _{snk} 2.5 mA Restart timer	Upper clamp voltage		I _{ZCD} =2.5mA	6.3	6.8	7.3	V	
Source current capability Isrc -2.5 mA Sink current capability Isnk 2.5 mA Restart timer								
Sink current capability I _{snk} 2.5 mA Restart timer							mA	
Restart timer							_	
			·					
	Restart timer period	t _{d(rst)}		31	38	45	μs	



SD7530_Datasheet

Characteristics	Symbol	Test condition	Min.	Тур.	Max.	Unit		
Over Temperature Prote	Over Temperature Protection							
OTP	T _{OTP}			135		°C		
Temperature hysteresis	T _{HYS}			15		°C		
Gate driver								
Output low voltage	V _{OL}	I _{sink} =100mA		0.6	1.2	V		
Output high voltage	V _{OH}	I _{source} =5mA		15		V		
Peak drive source current	Isrcpk		-0.6			А		
Peak drive sink current	I _{snkpk}		0.8			А		
Voltage rise time	tr			70	110	ns		
Voltage fall time	t _f			40	70	ns		
Output clamp voltage	V _{clamp}	I _{source} =5mA ; V _{CC} =32V	12	15	18	V		

* All the parameters are in tracking

** The multiplier output is given by: $V_{CS} = K \times V_{MULT} \times (V_{COMP} - 2.5)$

*** Parameters guaranteed by design.

PIN CONFIGURATIONS



PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Description
1	INV	Ι	Inverting input of the error amplifier. The pin doubles as an ON/OFF control input.
2	COMP	I/O	Output of the error amplifier. A compensation network is placed between this pin and INV.
3	MULT	Ι	Main input to the multiplier.
4	CS	I	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin.
5	ZCD	Ι	Input to the zero current detector.
6	GND	I/O	Ground.
7	GD	0	Gate driver output.
8	VCC	I/O	Supply voltage.



FUNCTION DESCRIPTION

SD7530 is a high power factor flyback PWM controller special for LED lighting applications. It operates in transition mode, it reduces the switch turn-on loss, improves the conversion efficiency and provides very good power factor correction.

V_{CC} UVLO and V_{CC} OVP

Peripheral/internal circuit at pin Vcc of SD7530 is shown in figure 1. At the beginning of the power on, capacitor C1 is charged by V_{IN} through start resistor R1, and V_{CC} increases slowly. As V_{CC} is up to 17.5V, IC starts to work and output driving pulse. Output voltage should be established in a period during which V_{CC} discharges and diode D2 is reverse biased, and IC is fully powered by start capacitor C1. When output voltage increases to a certain value, diode D2 is forward conduction by auxiliary winding L3's voltage, and then V_{CC} increases rapidly to the desired value. Fig. 2 shows the voltage waveform of V_{CC} during start. IC enters under voltage status as V_{CC} is lower than 9.0V after start.

Moreover, the startup current of SD7530 is very low (less than 5uA), so large startup resistance R1 is

recommended for low power dissipation.

If Vcc exceeds the internal reference 34V, IC enters over voltage protection (OVP), and turns off the PWM until next restart.



Fig.1 Internal /peripheral circuit at pin V_{CC}



Error amplifier

Error amplifier of SD7530 and peripheral circuit are shown in fig.3. Error amplifier compares the voltage of pin INV which is fed back from output by optp-coupler with reference voltage (2.5V), amplifies the difference and outputs Vcomp. Generally, the bandwidth of PFC loop is less than 20Hz for better power factor correction, so compensation capacitor or resistor is connected between output (COMP) and inverting input (INV) of error amplifier in applications.



Fig.3 Error amplifier and peripheral circuit



Multiplier

Multiplier of SD7530 and peripheral/internal circuit are shown in figure 4. Input voltage V_{IN} (output of rectifier bridge) is connected to input of multiplier through pin MULT after voltage dividing by R1a, R1b, and the other input of multiplier is output of error amplifier. Input voltage Vmult at pin MULT is half-sine voltage signal, but output voltage of multiplier Vmo is the half-sine voltage with same phase and different amplitude of input voltage Vmult, and controls the peak inductor current to change simultaneity, so that half-sine input average current is available.

Input and output of multiplier is expressed as:

$$Vmo = K \times Vmult \times (Vcomp - 2.5)$$

Where, K is the gain. (typical value for SD7530 is 0.38)



Fig.4 Multiplier and peripheral circuit

Inductor current detection (turn off MOSFET)

Current sense comparator of SD7530 and peripheral circuit are shown in figure 5. It is used for detecting inductor peak current to turn off MOSFET and make the system to stop working. Sense resistor Rs is connected between source of MOSFET and ground, and the voltage of sense resistor can be behaved on inductor current, which acts as the non-inverting input of current sense comparator through pin CS, compared with output of multiplier, which acts as the inverting input. If peak voltage of sense resistor increases to the limited value of multiplier output, current sense comparator's output overturns to turn off MOSFET.

LEB is added at pin CS to chops off the sense voltage spike at MOSFET on state due to snubber diode reverse recovery.



Fig 5. Current sense comparator and peripheral circuit

Zero current detection (turn on MOSFET)

Microelectronics

Silan

Zero current comparator of SD7530 and peripheral circuit are shown in Fig.6. Zero current detector is used for detecting zero-crossing of inductor current and turning on MOSFET. Dotted terminal of auxiliary winding L3 is connected to pin ZCD via a resistor Rzcd. When inductor current decreases to zero, voltage at dotted terminal is lower than 0.25V, gate drive signal of MOSFET turns to high and MOSFET is turned on, and 0.85V hysteresis is set to avoid error actions.

Clamp circuit at pin ZCD clamps the voltage in 0V~6.0V.



Fig. 6 Zero current comparator and peripheral circuit

Fig. 7 shows the detailed voltage waveforms for zero current detection. After MOSFET is turned off and before the inductor current decreases to zero, the voltage at pin ZCD keeps high and is given as:

$$V_{ZCD} = \frac{(Vo - Vin)}{n}$$

Where, n is the turns ratio of the primary windings L1 and auxiliary windings L3.

During MOSFET off but inductor current is not zero, the inductor current is supplied to the load through secondary winding L2 and diode D1, and decreases linearly to zero, at the mean while the diode D1 is reverse blocked and MOSFET S1 junction capacitor is resonant with the primary windings L1 and input capacitor Cin. Then the drain voltage of MOSFET is going down, voltage at pin ZCD also decreases. When the drain voltage decreases to V_{IN} , the voltage at dotted terminal of auxiliary winding L3 is zero. Due to MOSFET is still off, the drain voltage continuously decreases until the voltage at pin ZCD is lower than 0.25V, then MOSFET is on. When the drain voltage decreases to zero, the resonance stops and the inductor current increases linearly.

As shown in Fig. 7 below, this characteristic allows turning on MOS with low voltage for decreasing the switch turn-on loss

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Fig. 7. The detailed voltage waveforms for zero current detection

Output short-circuit protection

SD7530 integrates output short-circuit protect(SCP) circuit. If output load's short-circuit state is detected by IC, PWM will be turned off automatically, and V_{CC} will gradually decrease until IC restarts automatically.

Soft start

SD7530 integrates soft-start circuit, which is used to reduce the voltage stresses and current surges of IC during start up. This circuit first clamps the output voltage of multiplier at a low level, then improves the output voltage gradually during start up. So that PWM can increase gradually from zero to the steady state.

Over temperature protection

SD7530 integrates over temperature protect(OTP) circuit. IC is shutdown when the temperature is higher than 135°C and recovers when temperature decreases to 120°C.

TYPICAL APPLICATION CIRCUIT





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PACKAGE OUTLINE





MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

Disclaimer :

- Silan reserves the right to make changes to the information herein for the improvement of the design and performance without further notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
- All semiconductor products malfunction or fail with some probability under special conditions. When using Silan
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 with the safety standards strictly and take essential measures to avoid situations in which a malfunction or
 failure of such Silan products could cause loss of body injury or damage to property.
- Silan will supply the best possible product for customers!



ATTACHMENT

Revision History

Date	REV	Description	Page
2012.10.25	1.0	Initial release	
2013.07.24	1.1	Delete the information of SD7530A	