2A, 23V, 350kHz, Synchronous Step-Down DC/DC Converter

FEATURES

- 4.75V to 23V input voltage
- Output adjustable from 0.923V to 18V
- Output current up to 2A
- Integrated 0.13Ω power MOSFET switches
- Shutdown current 1μA typical
- Efficiency up to 93%
- 350kHz fixed frequency
- Programmable soft start
- Over current protection
- Over temperature protection
- RoHS Compliant and 100% Lead (Pb) Free

APPLICATIONS

- Distributed power systems
- Networking systems
- FPGA, DSP, ASIC power supplies
- Notebook computers
- Green electronics or appliance

ORDERING INFORMATION

PART	PACKAGE	RoHS	Ship, Quantity
ZT7182S	SOP-8L(EP)	Yes	Tape and Reel

DESCRIPTION

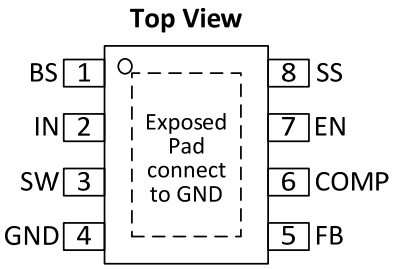
The ZT7182 is a 350kHz fixed frequency PWM synchronous step-down regulator. The ZT7182 is operated from 4.75V to 23V, the generated output is adjustable from 0.923V to 18V, and the output current can be up to 2A.

The integrated two MOSFET switches is with turn on resistance of 0.13Ω. Current mode control provides fast transient response and cycle-by-cycle over current protection. The shutdown current is 1μA typical. Adjustable soft start prevents inrush current at turn on. The ZT7182 is with thermal shutdown.

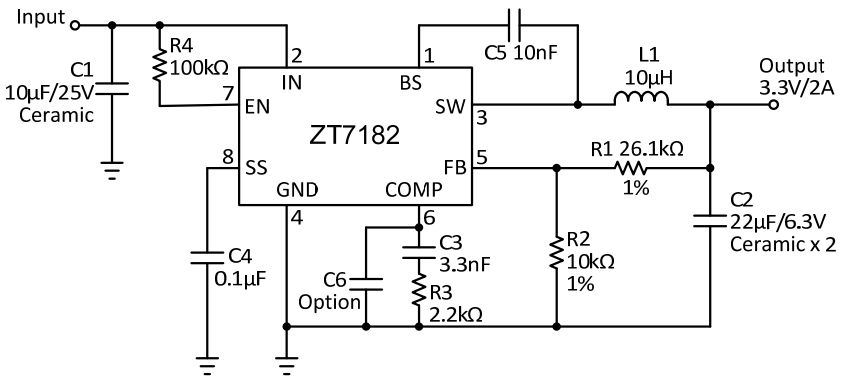
The ZT7182 is available in the SOP-8L package, and it is RoHS compliant and 100% lead (Pb) free.

Pins Configuration

Top View



Typical Application Circuit



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Absolute Maximum Ratings

Supply Voltage V_{IN} ..... –0.3V to +24V
Switch Node V_{SW} ..... –0.3V to V_{IN}+0.3V
Boost V_{BS} ..... V_{SW}–0.3V to V_{SW}+6V
All Other Pins ..... –0.3V to +6V
Junction Temperature ..... +150°C
Lead Temperature ..... +260°C
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electro-Static Discharge Sensitivity

This integrated circuit can be damaged by ESD. It is recommended that all integrated circuits be handled with proper precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure.

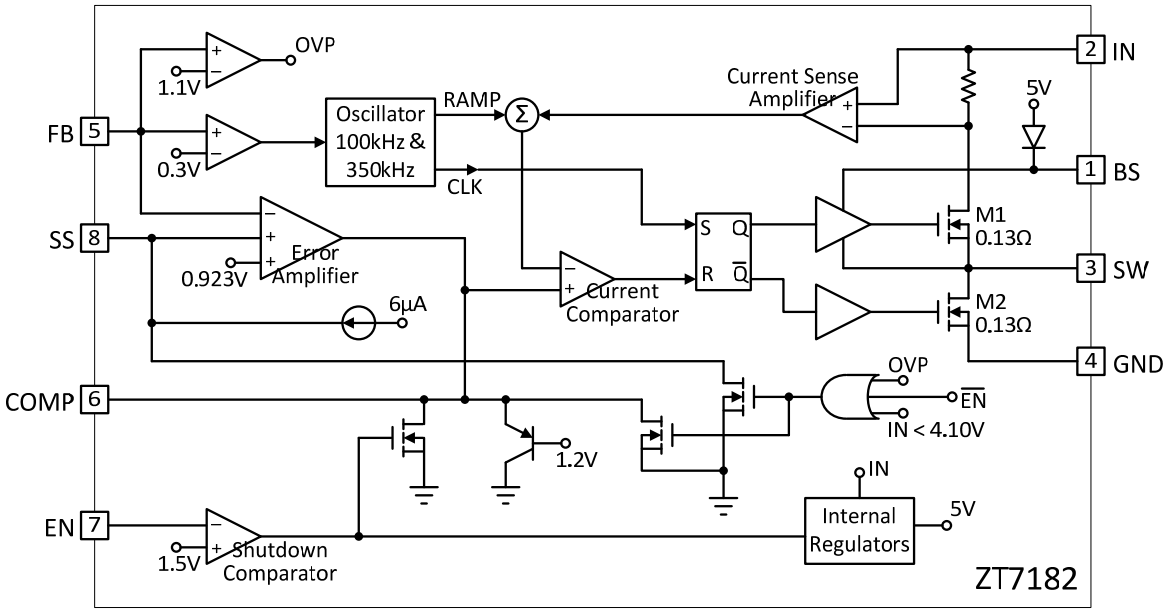
Package Thermal Characteristics

Thermal Resistance, θ_{JA} ..... 42°C/W
Thermal Resistance, θ_{JC} ..... 10°C/W

Pins Description

Pin	Symbol	Description
1	BS	High-side gate drive boost input.
2	IN	Power input.
3	SW	Power switching output.
4	GND	Ground.
5	FB	Feedback input.
6	COMP	Compensation node.
7	EN	Enable input.
8	SS	Soft start control input.

Functional Block Diagram



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Electrical Specifications

(T_A = +25°C, V_{IN} = +12V, unless otherwise noted.)

PARAMETER	Symbol	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{IN}		4.75		23	V
Output Voltage	V_{OUT}		0.923		18	V
Shutdown Supply Current		V_{EN} = 0V		1	3.0	μA
Supply Current		V_{EN} = 2.0V, V_{FB} = 1.0V		1.3	1.5	mA
Feedback Voltage	V_{FB}	4.75V ≤ V_{IN} ≤ 23V	0.900	0.923	0.946	V
Feedback Over-voltage Threshold				1.1		V
Error Amplifier Voltage Gain *	A_{EA}			400		V/V
Error Amplifier Transconductance	G_{EA}	ΔI_C = ±10μA		800		μA/V
High-Side Switch-On Resistance *	$R_{DS(ON)1}$			130		mΩ
Low-side Switch-On Resistance *	$R_{DS(ON)2}$			130		mΩ
High-Side Switch Leakage Current		V_{EN} = 0V, V_{SW} = 0V			10	μA
Upper Switch Current Limit		Minimum duty cycle	2.4	3.4		A
Lower Switch Current Limit		From drain to source		1.1		A
COMP to Current Sense Transconductance	G_{CS}			3.5		A/V
Oscillation Frequency	F_{OSC1}			350		kHz
Short Circuit Oscillation Frequency	F_{OSC2}	V_{FB} = 0V		100		kHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 1.0V		90		%
Minimum On Time *				220		ns
EN Shutdown Threshold Voltage		V_{EN} rising	1.1	1.5	2.0	V
EN Shutdown Threshold Voltage Hysteresis				210		mV
EN Lockout Threshold Voltage			2.2	2.5	2.7	V
EN Lockout Hysteresis				210		mV
Input Under Voltage Lockout Threshold		V_{IN} rising	3.80	4.10	4.40	V
Input Under Voltage Lockout Threshold Hysteresis				210		mV
Soft-Start Current		V_{SS} = 0V		6		μA
Soft-Start Period		C_{SS} = 0.1μF		15		ms
Thermal Shutdown *				160		°C

* Guaranteed by design, not tested.

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APPLICATION INFORMATION

Overview

The ZT7182 is a synchronous rectified, current-mode, step-down regulator. It regulates input voltages from 4.75V to 23V down to an output voltage as low as 0.923V, and supplies up to 2A of load current.

The ZT7182 uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal transconductance error amplifier. The voltage at the COMP pin is compared to the switch current measured internally to control the output voltage.

The converter uses internal N-Channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BS is needed to drive the high side gate. The boost capacitor is charged from the internal 5V rail when SW is low.

When the ZT7182 FB pin exceeds 20% of the nominal regulation voltage of 0.923V, the over voltage comparator is tripped and the COMP pin and the SS pin are discharged to GND, forcing the high-side switch off.

Pins Description

BS: High-Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 0.01µF or greater capacitor from SW to BS to power the high side switch.

IN: Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.75V to 23V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC.

SW: Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.

GND: Ground.

FB: Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback threshold is 0.923V.

COMP: Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required.

EN: Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off. Pull up with 100kΩ resistor for automatic startup.

SS: Soft-Start Control Input. SS controls the soft start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1µF capacitor sets the soft-start period to 15ms. To disable the soft-start feature, leave SS unconnected.

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB pin. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \times R2 / (R1 + R2)$$

Where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Thus the output voltage is:

$$V_{OUT} = 0.923 \times (R1 + R2) / R2$$

R2 can be as high as 100kΩ, but a typical value is 10kΩ. Using the typical value for R2, R1 is determined by:

$$R1 = 10.83 \times (V_{OUT} - 0.923) \text{ (k}\Omega\text{)}$$

Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the

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maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = [V_{OUT} / (f_S \times \Delta I_L)] \times (1 - V_{OUT}/V_{IN})$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP} = I_{LOAD} + [V_{OUT} / (2 \times f_S \times L)] \times (1 - V_{OUT}/V_{IN})$$

Where I_{LOAD} is the load current.

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI requirements.

Optional Schottky Diode

During the transition between high-side switch and low-side switch, the body diode of the low-side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional Schottky diode may be paralleled between the SW pin and GND pin to improve overall efficiency. Table 1 lists example Schottky diodes and their Manufacturers.

Part Number	Voltage and Current Rating	Vendor
B130	30V, 1A	Diodes Inc.
SK13	30V, 1A	Diodes Inc.
MBRS130	30V, 1A	International Rectifier

Table 1: Diode selection guide.

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times [(V_{OUT}/V_{IN}) \times (1 - V_{OUT}/V_{IN})]^{1/2}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where $I_{C1} = I_{LOAD}/2$. For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1µF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple for low ESR capacitors can be estimated by:

$$\Delta V_{IN} = [I_{LOAD}/(C1 \times f_S)] \times (V_{OUT}/V_{IN}) \times (1 - V_{OUT}/V_{IN})$$

Where C1 is the input capacitance value.

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = [V_{OUT}/(f_S \times L)] \times (1 - V_{OUT}/V_{IN}) \times [R_{ESR} + 1 / (8 \times f_S \times C2)]$$

Where C2 is the output capacitance value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = [V_{OUT}/(8 \times f_S^2 \times L \times C2)] \times (1 - V_{OUT}/V_{IN})$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = [V_{OUT}/(f_S \times L)] \times (1 - V_{OUT}/V_{IN}) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The ZT7182 can be optimized for a wide range of capacitance and ESR values.

Compensation Components

ZT7182 employs current mode control for easy

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compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP pin is the output of the internal transconductance error amplifier. A series capacitor and resistor combination sets a pole-zero combination to control the characteristics of the control system.

The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{EA} \times V_{FB}/V_{OUT}$$

Where A_{EA} is the error amplifier voltage gain; G_{CS} is the current sense transconductance and R_{LOAD} is the load resistor value.

The system has two poles of importance. One is due to the compensation capacitor (C3) and the output resistor of the error amplifier, and the other is due to the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = G_{EA} / (2\pi \times C3 \times A_{EA})$$

$$f_{P2} = 1 / (2\pi \times C2 \times R_{LOAD})$$

Where G_{EA} is the error amplifier transconductance.

The system has one zero of importance, due to the compensation capacitor (C3) and the compensation resistor (R3). This zero is located at:

$$f_{Z1} = 1 / (2\pi \times C3 \times R3)$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$f_{ESR} = 1 / (2\pi \times C2 \times R_{ESR})$$

In this case, a third pole set by the compensation capacitor (C6) and the compensation resistor (R3) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$f_{P3} = 1 / (2\pi \times C6 \times R3)$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system instability. A good rule of thumb is to set the crossover frequency below one-tenth of the switching frequency.

To optimize the compensation components, the following procedure can be used.

1. Choose the compensation resistor (R3) to set the desired crossover frequency.

Determine the R3 value by the following equation:

$$R3 = [(2\pi \times C2 \times f_C) / (G_{EA} \times G_{CS})] \times (V_{OUT}/V_{FB})$$

$$< [(2\pi \times C2 \times 0.1 \times f_S) / (G_{EA} \times G_{CS})] \times (V_{OUT}/V_{FB})$$

Where f_C is the desired crossover frequency which is typically below one tenth of the switching frequency.

2. Choose the compensation capacitor (C3) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero, f_{Z1}, below one-forth of the crossover frequency provides sufficient phase margin.

Determine the C3 value by the following equation:

$$C3 > 4 / (2\pi \times R3 \times f_C)$$

Where R3 is the compensation resistor.

3. Determine if the second compensation capacitor (C6) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency, or the following relationship is valid:

$$1 / (2\pi \times C2 \times R_{ESR}) < f_S/2$$

If this is the case, then add the second compensation capacitor (C6) to set the pole f_{P3} at the location of the ESR zero. Determine the C6 value by the equation:

$$C6 = (C2 \times R_{ESR}) / R3$$

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BS diode are:

- V_{OUT} = 5V or 3.3V; and
- Duty cycle is high: $D = V_{OUT}/V_{IN} > 65\%$

In these cases, an external BS diode is recommended from the output of the voltage regulator to BS pin, as shown in Figure 1.

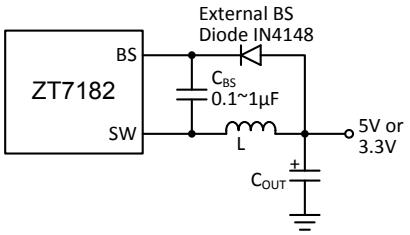

Figure 1: Add optional external bootstrap diode to enhance efficiency.

The recommended external BS diode is IN4148, and the BS capacitor is 0.1 ~ 1μF.

When $V_{IN} \leq 6V$, for the purpose of promote the efficiency, it can add an external Schottky diode

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between IN and BS pins, as shown in Figure 2.

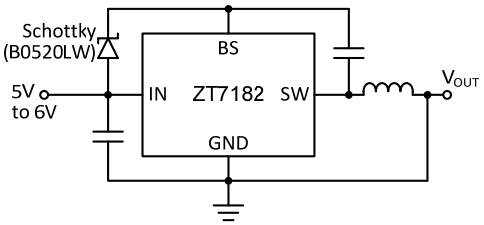

Figure 2: Add a Schottky diode to promote efficiency when $V_{IN} \leq 6V$.

PCB Layout Guide

PCB layout is very important to achieve stable operation. Please follow the guidelines below.

1) Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.
2) Bypass ceramic capacitors are suggested to be put close to the V_{IN} Pin.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Rout SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

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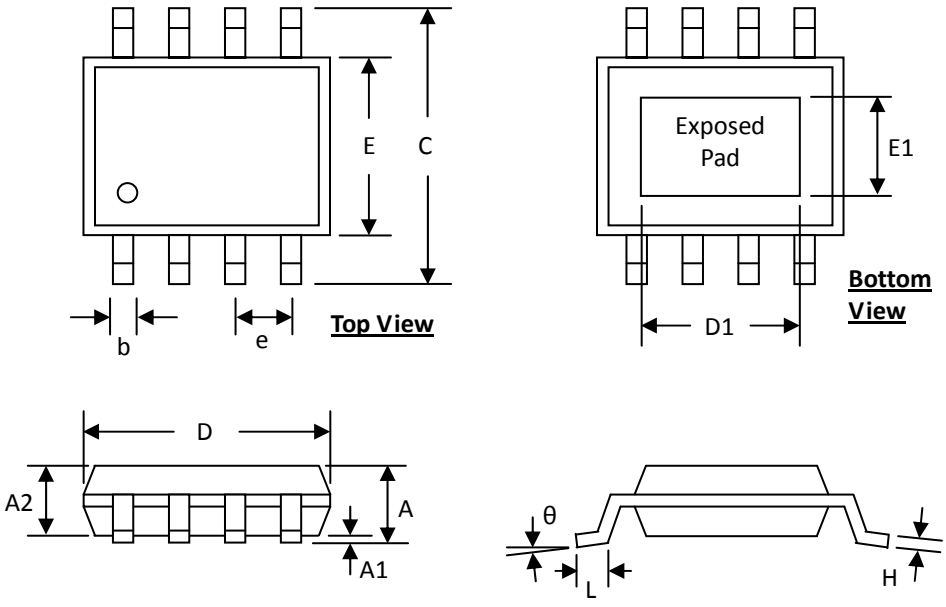
PACKAGE DIMENSIONS SOP-8L(EP)



SYMBOLS	DIMENSION (MM)		DIMENSION (INCH)	
	MIN	MAX	MIN	MAX
A	1.30	1.70	0.051	0.067
A1	0.00	0.15	0.000	0.006
A2	1.25	1.52	0.049	0.060
b	0.33	0.51	0.013	0.020
C	5.80	6.20	0.228	0.244
D	4.80	5.00	0.189	0.197
D1	3.15	3.45	0.124	0.136
E	3.80	4.00	0.150	0.157
E1	2.26	2.56	0.089	0.101
e	1.27 BSC		0.050 BSC	
H	0.19	0.25	0.0075	0.0098
L	0.41	1.27	0.016	0.050
θ	0°	8°	0°	8°

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