

H7N0603DL, H7N0603DS

Silicon N Channel MOS FET
High speed power Switching

REJ03G0123-0200

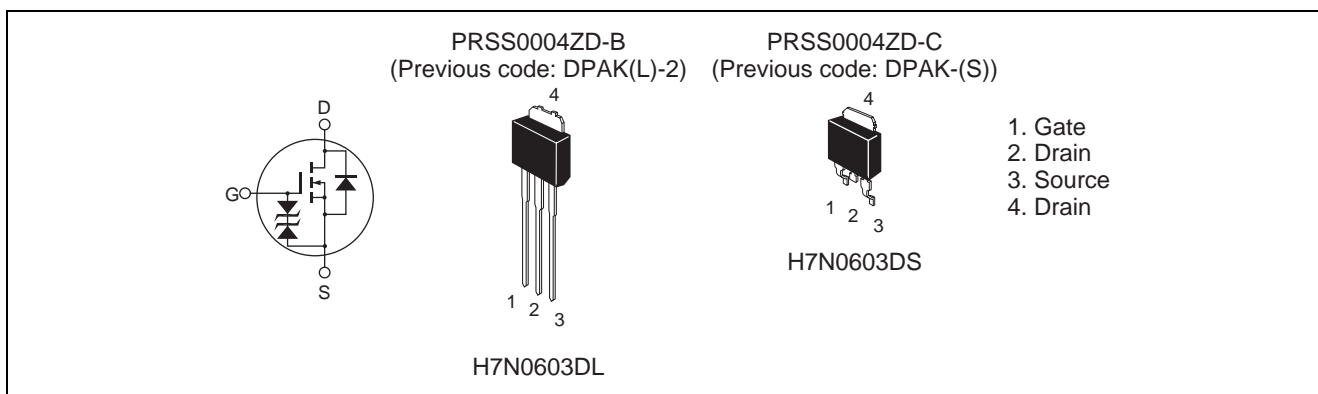
Rev.2.00

Jan.26.2005

Features

- Low on - resistance
 $R_{DS(on)} = 11\text{ m}\Omega$ typ.
- Low drive current
- Capable of 4.5 gate drive

Outline



Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	60	V
Gate to source voltage	V_{GS}	± 20	V
Drain current	I_D	30	A
Drain peak current	I_D (pulse) ^{Note1}	120	A
Body drain diode reverse drain current	I_{DR}	30	A
Avalanche current	I_{AP} ^{Note3}	25	A
Avalanche energy	E_{AR} ^{Note3}	53.6	mJ
Channel dissipation	P_{ch} ^{Note2}	40	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10\text{ }\mu\text{s}$, duty cycle $\leq 1\%$

2. $T_c = 25^\circ\text{C}$

3. $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50\Omega$

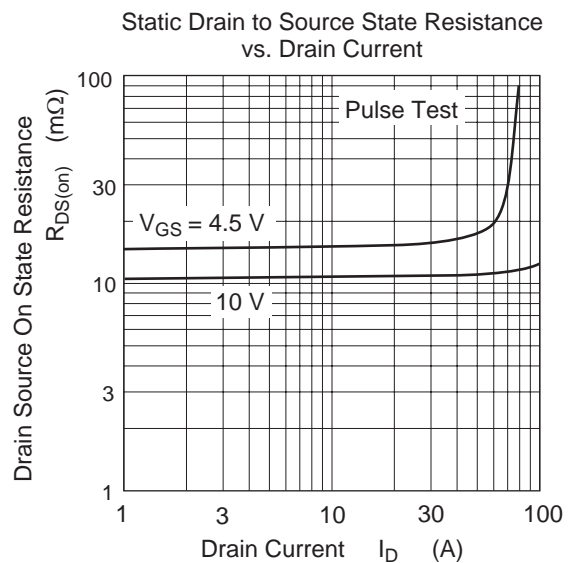
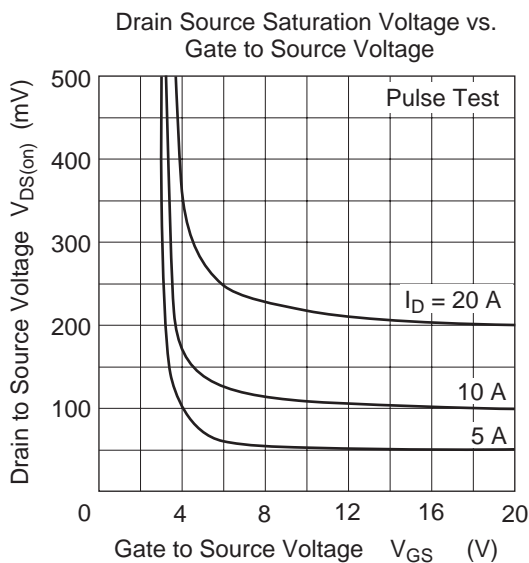
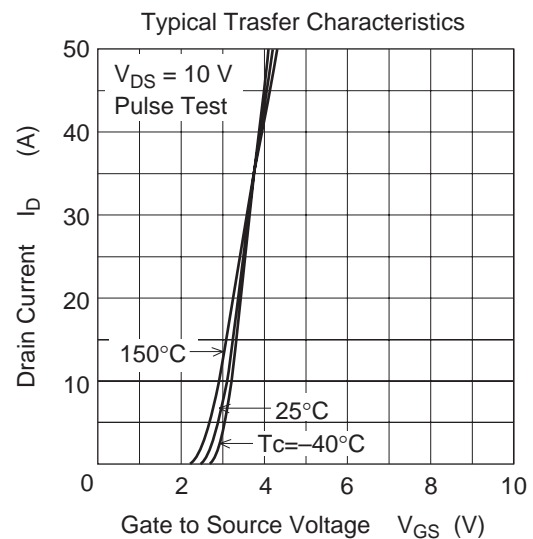
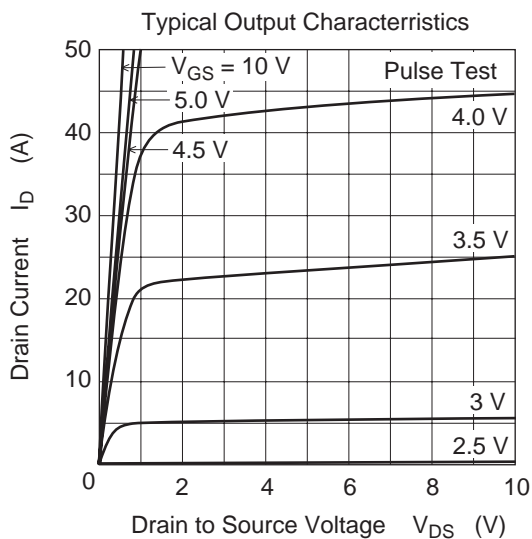
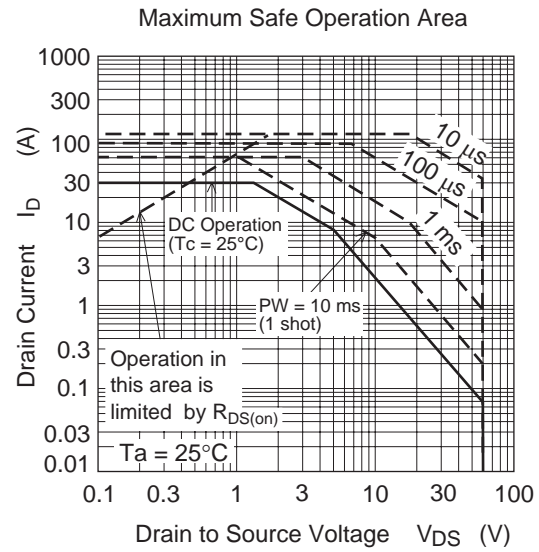
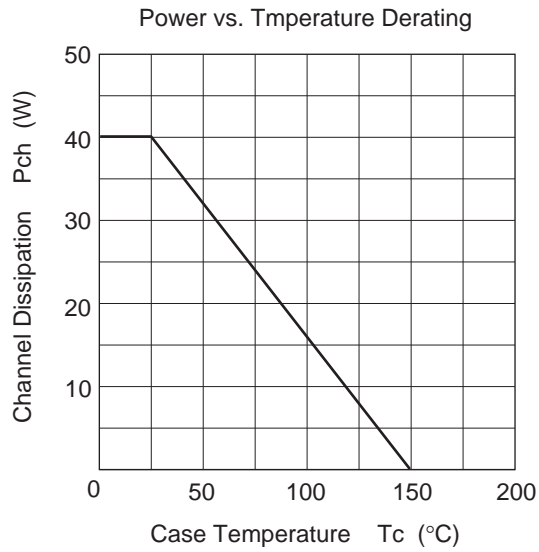
Electrical Characteristics

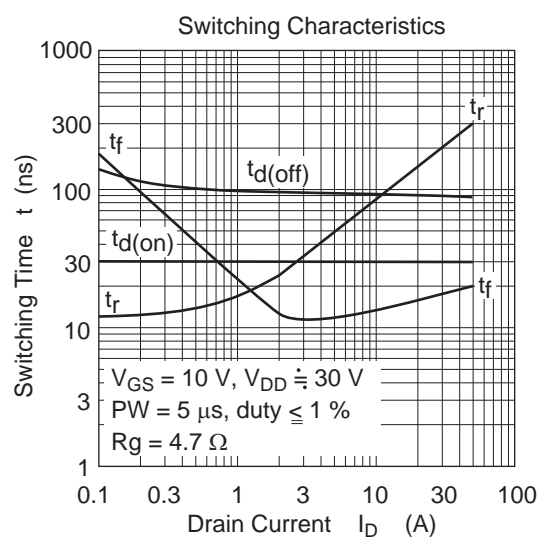
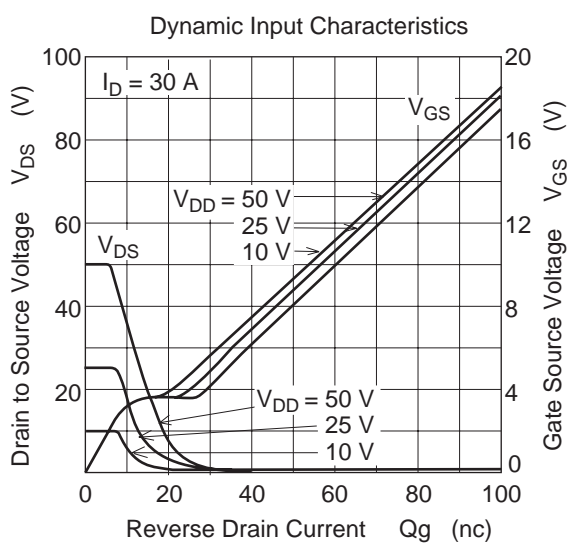
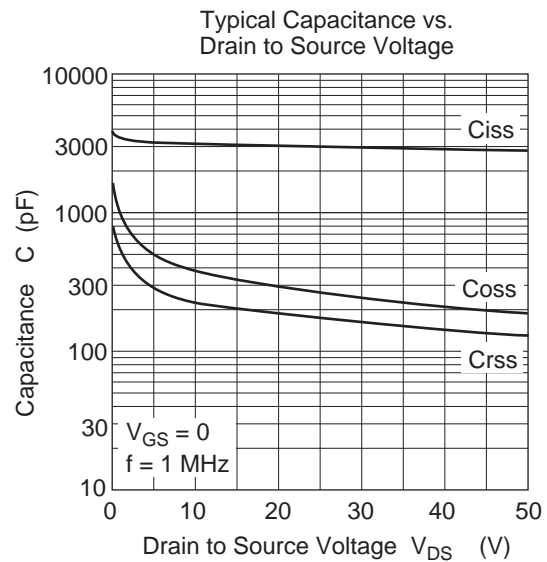
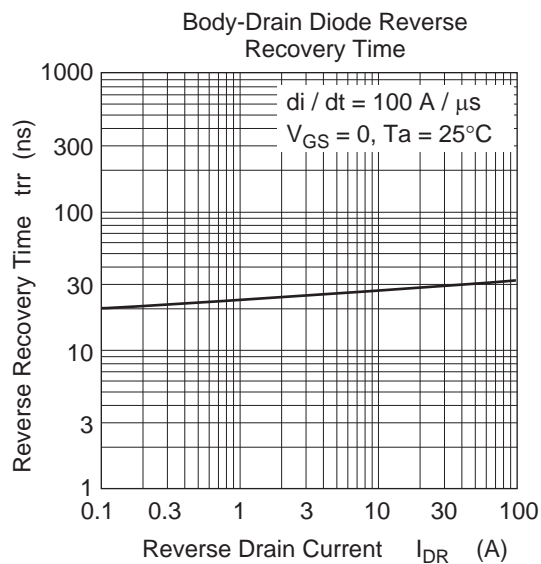
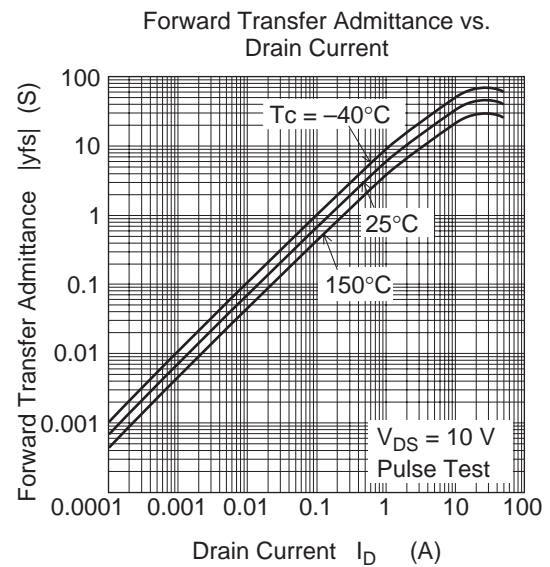
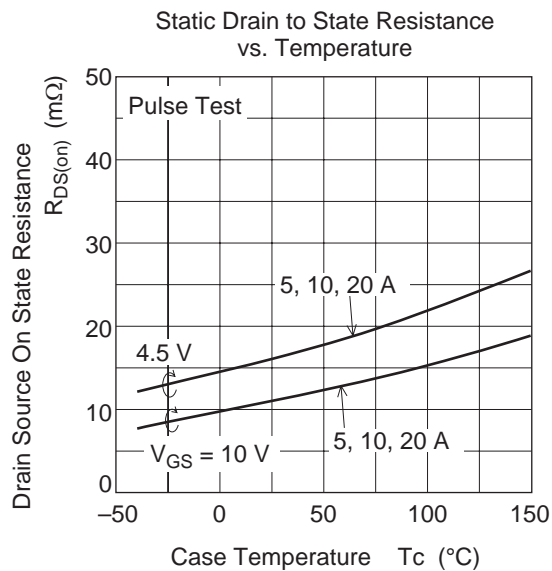
(Ta = 25°C)

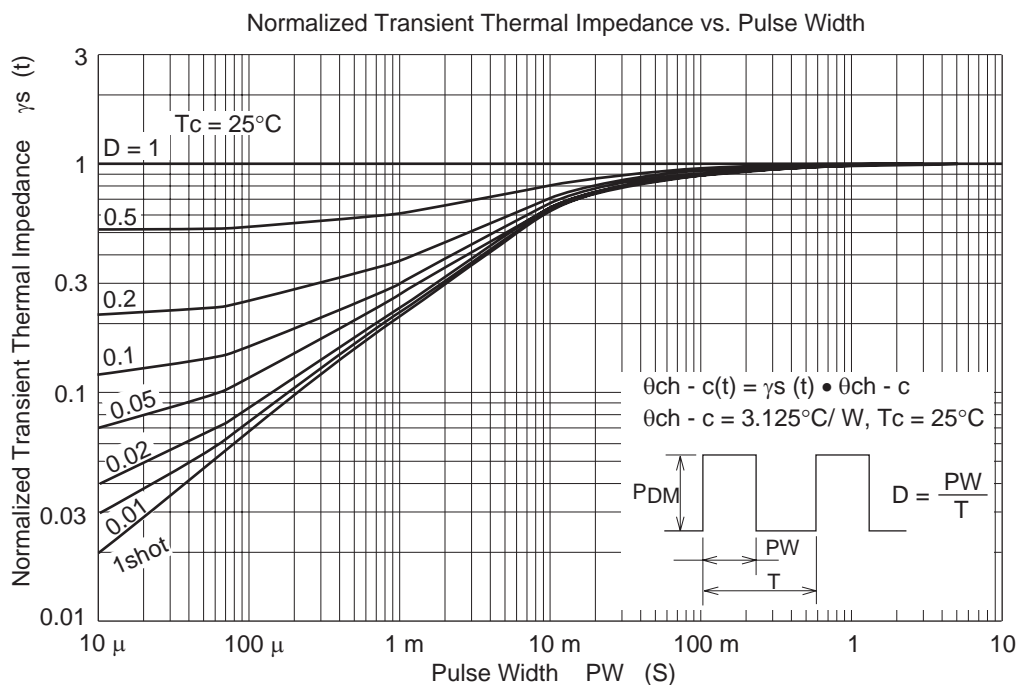
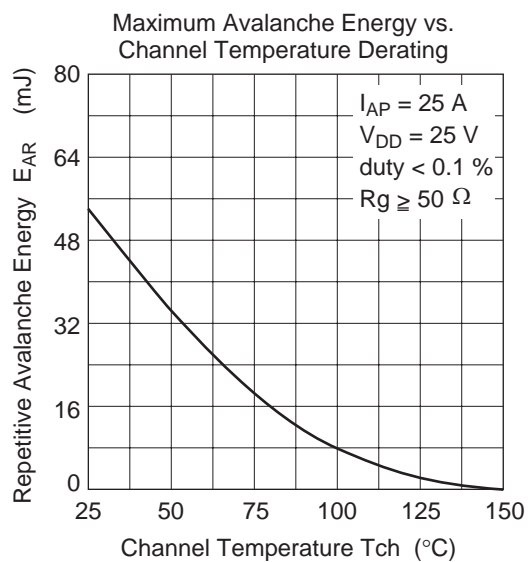
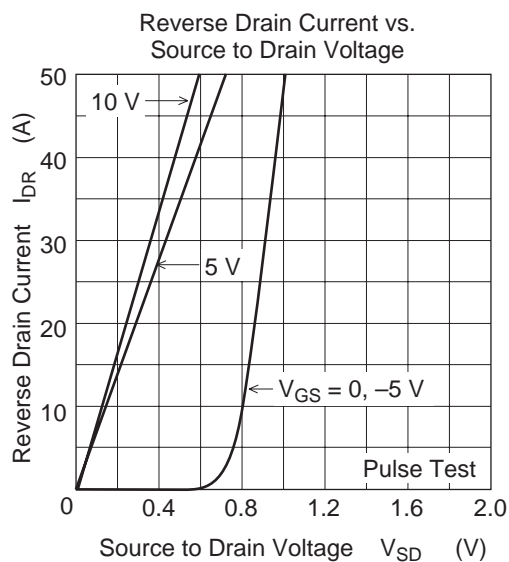
Item	Symbol	Min	Typ	Max	Unit	Test condition
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 60 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	2.5	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	11	15	$\text{m}\Omega$	$I_D = 15 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note1}
		—	16	22	$\text{m}\Omega$	$I_D = 15 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note1}
Forward transfer capacitance	$ y_{fs} $	24	40	—	S	$I_D = 15 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note1}
Input capacitance	C_{iss}	—	3200	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	385	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	225	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Q_g	—	56	—	nC	$V_{DD} = 25 \text{ V}$
Gate to source charge	Q_{gs}	—	11	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	12	—	nC	$I_D = 30 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$
Rise time	t_r	—	125	—	ns	$R_L = 2.0 \text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	—	90	—	ns	$R_g = 4.7 \text{ }\Omega$
fall time	t_f	—	17	—	ns	
Body - drain diode forward voltage	V_{DF}	—	0.9	—	V	$I_F = 30 \text{ A}$, $V_{GS} = 0$ ^{Note1}
Body – drain diode reverse recovery time	t_{rr}	—	30	—	ns	$I_F = 30 \text{ A}$, $V_{GS} = 0$ $diF / dt = 100 \text{ A} / \mu\text{s}$

Notes: 1. Pulse Test

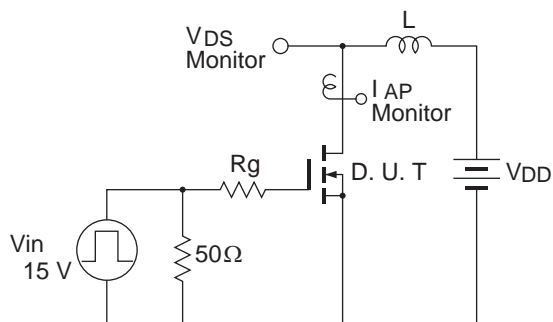
Main Characteristics





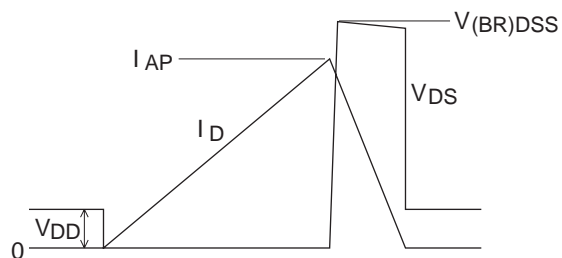


Avalanche Test Circuit

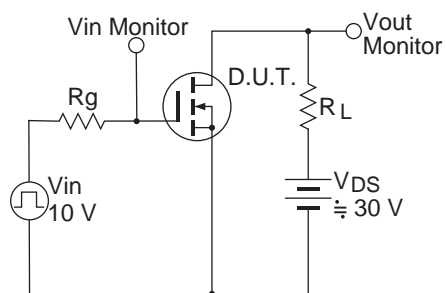


Avalanche Waveform

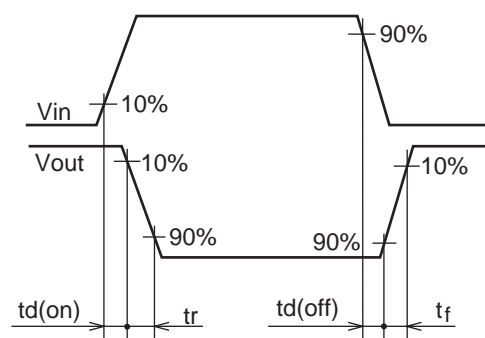
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test circuit

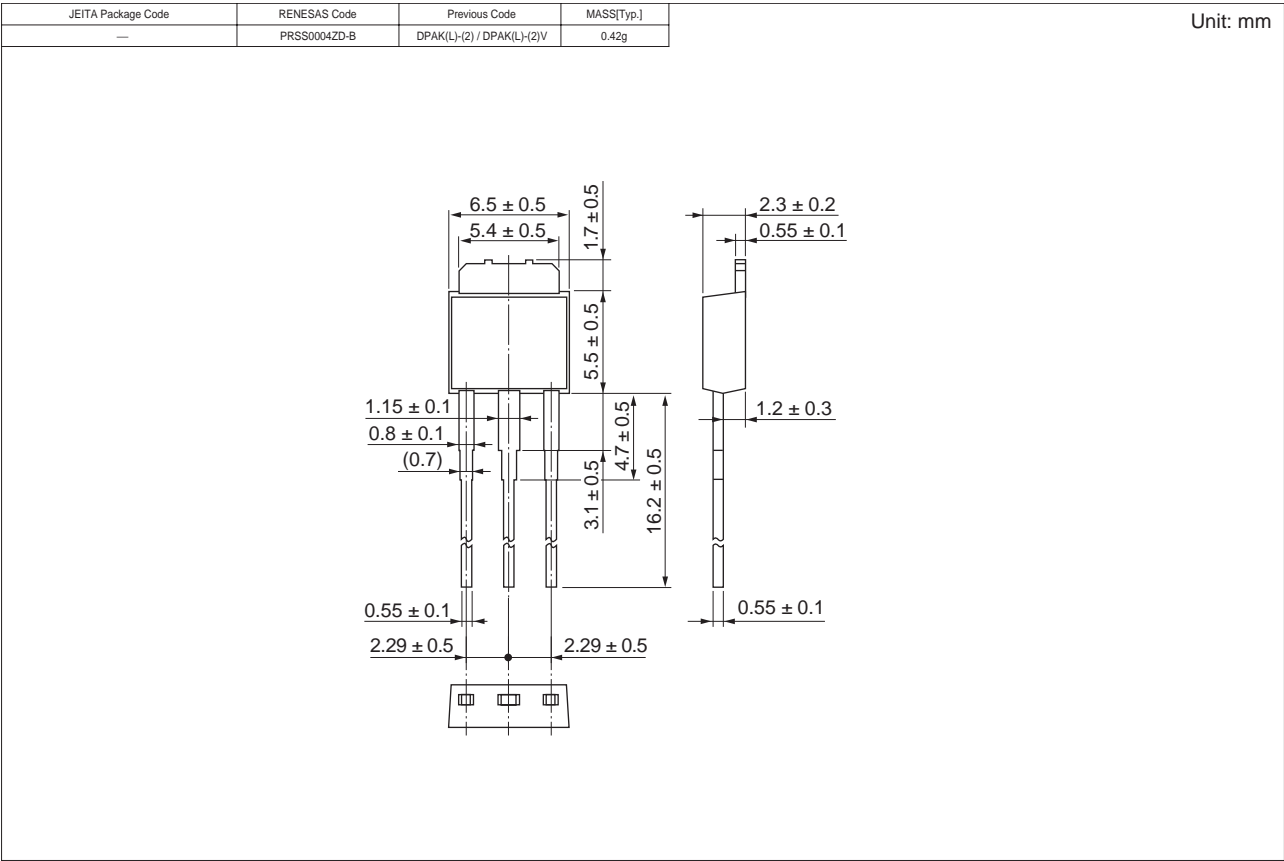


Switching Time Waveform

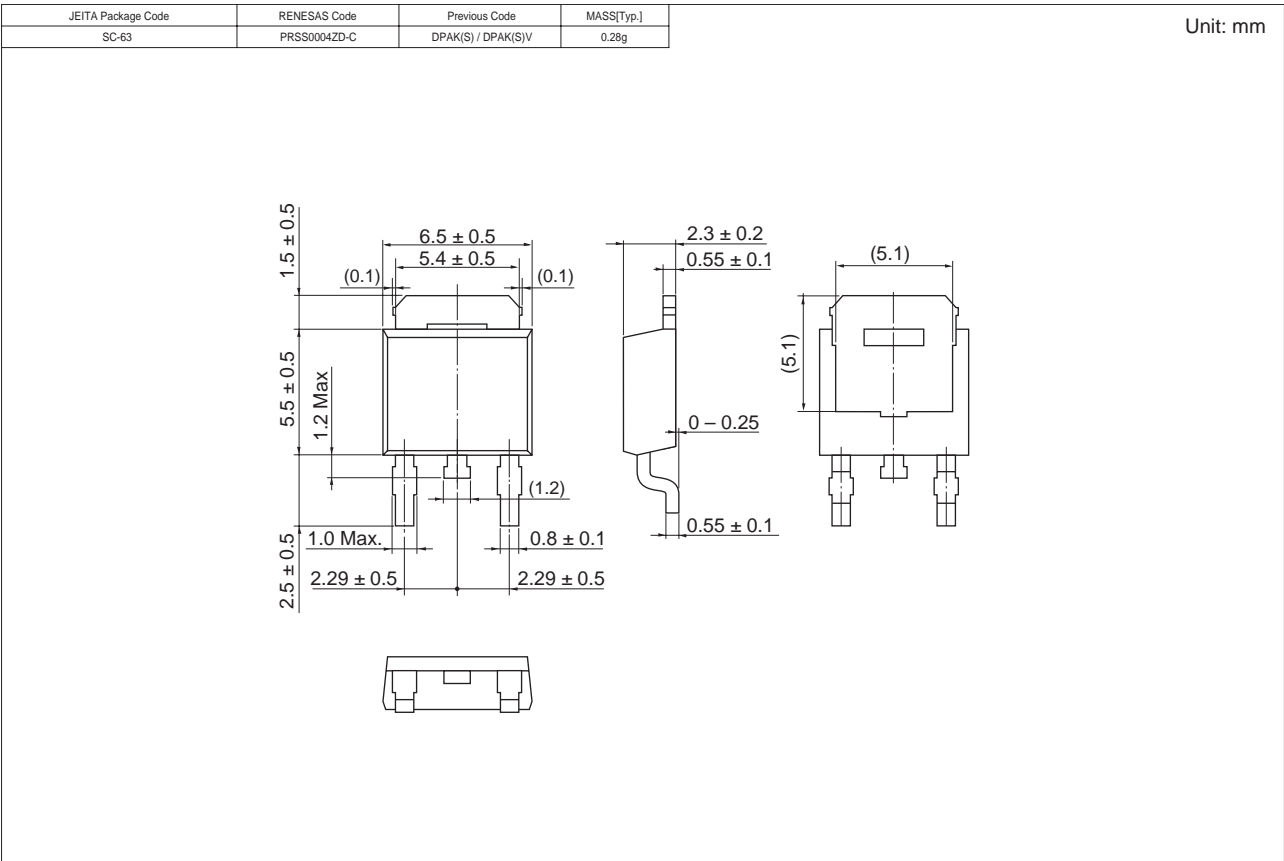


Package Dimensions

• H7N0603DL



• H7N0603DS



Ordering Information

Part Name	Quantity	Shipping Container
H7N0603DL	100 pcs	Sack
H7N0603DSTL	3000 pcs	Taping
H7N0603DL-E	100 pcs	Sack
H7N0603DSTL-E	3000 pcs	Taping

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