SGS-THOMSON MICROELECTRONICS

STVHD90

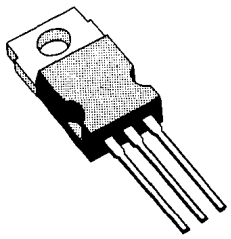
N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STVHD90	50 V	0.023 Ω	52 A

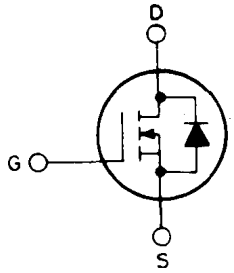
- VERY HIGH DENSITY
- VERY LOW $R_{DS\ (on)}$
- VERY HIGH CURRENT
- HIGH TRANSCONDUCTANCE/C_{rss} RATIO
- LOW DRIVE ENERGY
- ULTRA FAST SWITCHING

N - channel enhancement mode very high density POWER MOS transistors. Easy drive and low on voltage make this device ideal for automotive and industrial applications requiring high current and low on-losses. Typical uses are actuators lamp and motor control in the automotive and industrial enviroments. It can also be used in DC/DC converters.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	50	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c=25°C$	52	A
I_D	Drain current (cont.) at $T_c=125°C$	32	A
I_{DM} (•)	Drain current (pulsed)	200	A
I_{DLM}	Drain inductive current clamped	200	A
P_{tot}	Total dissipation at $T_c<25°C$	125	W
	Derating factor	1	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	1	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8	T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				100	nA
ON (*)							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 30 A			23	mΩ
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 30 A		30		mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz		2500 850 120	3000 1000 150	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 40 V V_i = 50 V (see test circuit)	I_D = 25 A R_i = 50 Ω			40 100 250 170	ns ns ns ns
Q_g	Total Gate Charge	V_{DD} = 25 V V_{GS} = 10 V	I_D = 30 A		56		nC

ELECTRICAL CHARACTERISTICS (Continued)

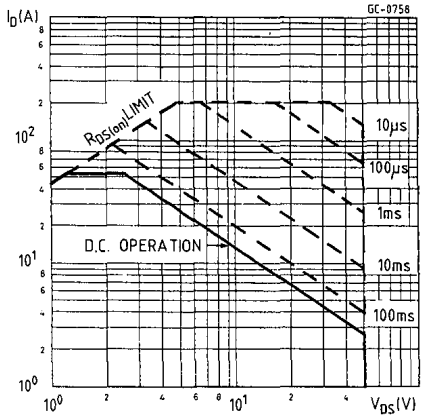
Parameters	Test Conditions	Min.	Typ.	Max.	Unit

SOURCE DRAIN DIODE

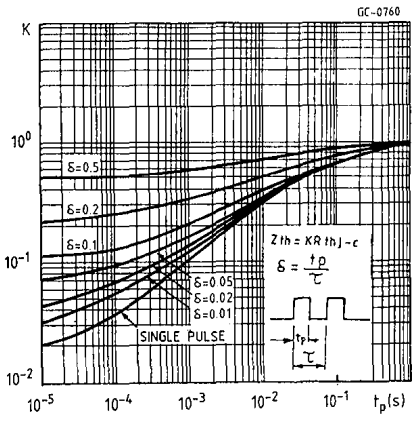
I_{SD} I_{SDM} (•)	Source-drain current Source-drain current (pulsed)				52 200	A A
V_{SD}	Forward on voltage	I_{SD} = 52 A	V_{GS} = 0			1.5	V
t_{rr} Q_{rr}	Reverse recovery time Reverse recovery charge	I_{SD} = 52 A di/dt = 100 A/μs	V_{GS} = 0		70 110		ns μC

(•) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%

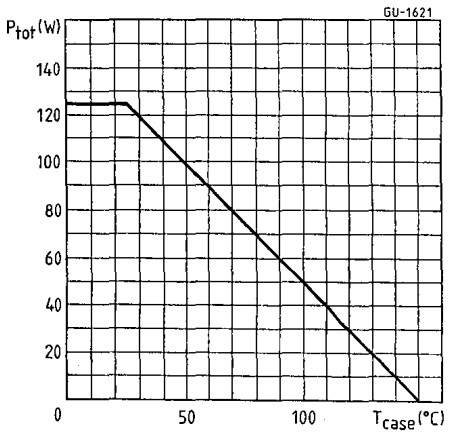
Safe operating areas



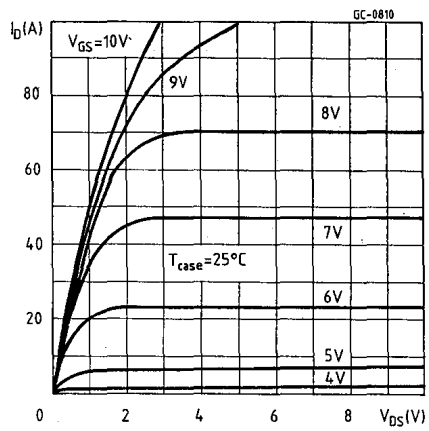
Thermal impedance



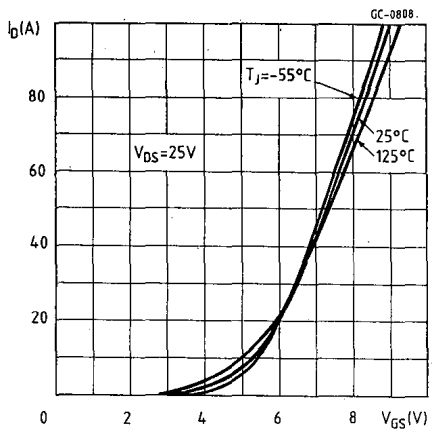
Derating curve



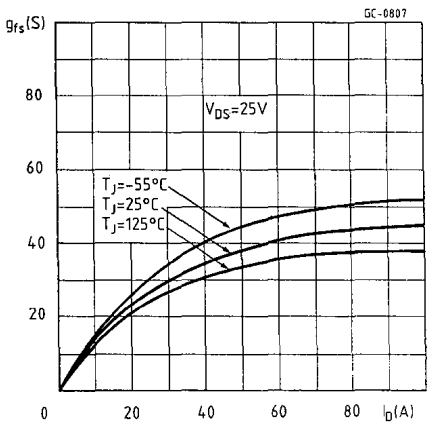
Output characteristics



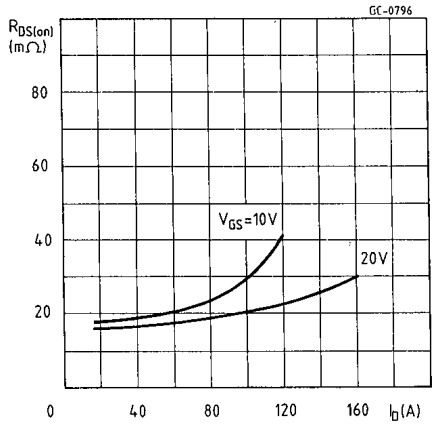
Transfer characteristics



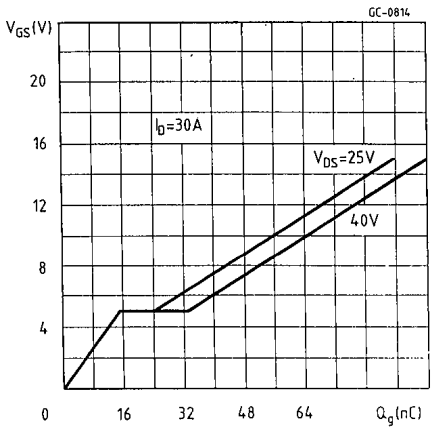
Transconductance



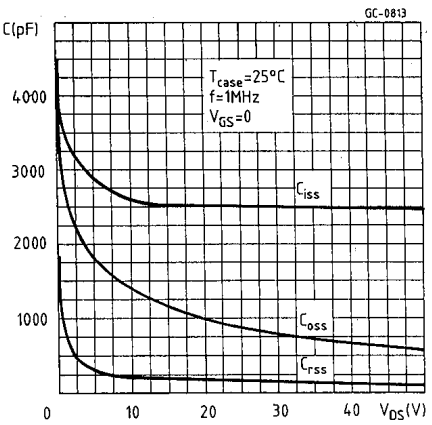
Static drain-source on resistance



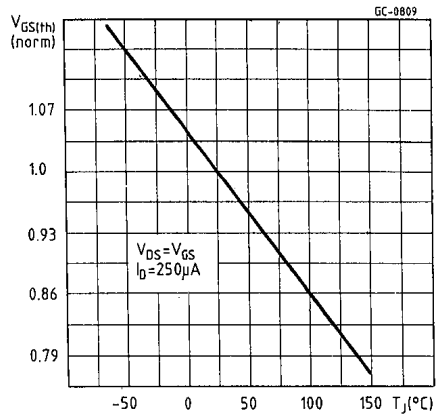
Gate charge vs gate-source voltage



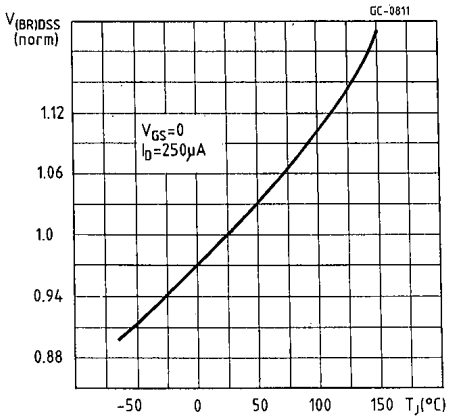
Capacitance variation



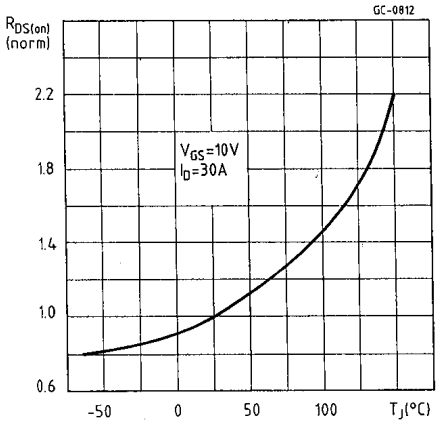
Normalized gate threshold voltage vs temperature



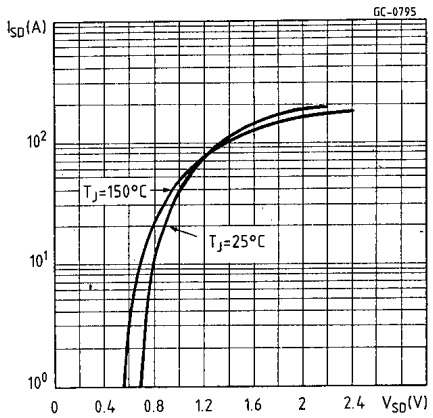
Normalized breakdown voltage vs temperature



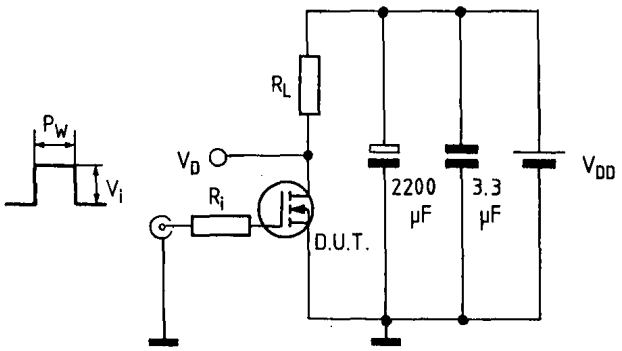
Normalized on resistance vs temperature



Static drain diode forward characteristics

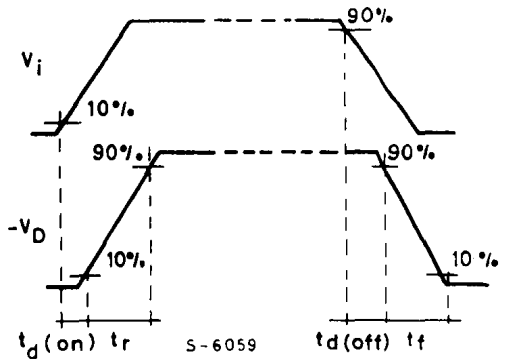


Switching times test circuit for resistive load

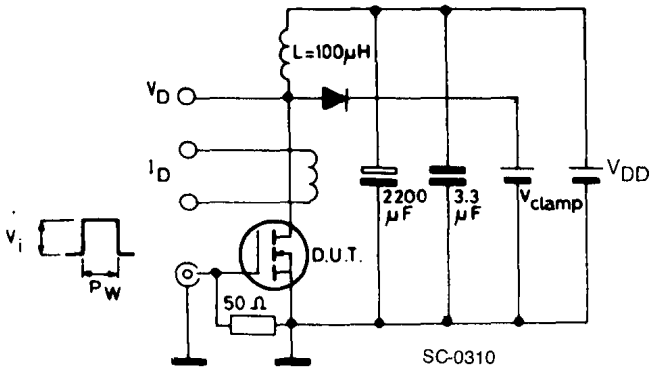


Pulse width ≤ 100 µs
Duty cycle ≤ 2%

Switching time waveforms for resistive load

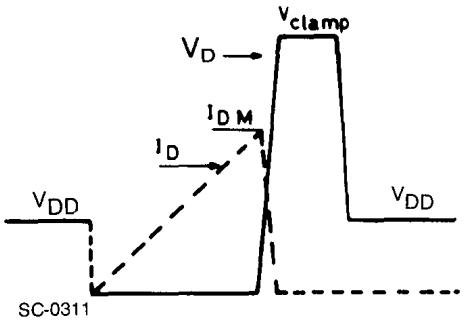


Clamped inductive load test circuit

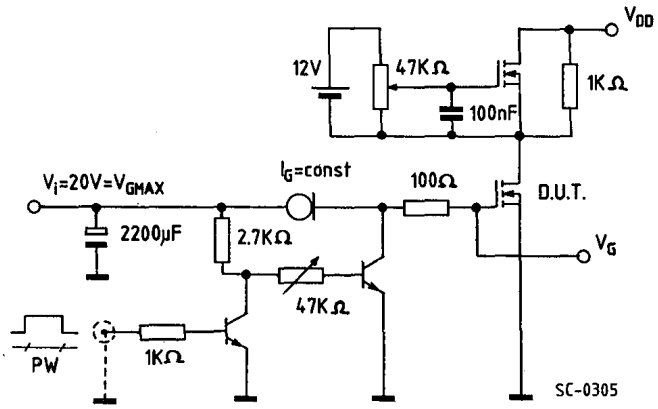


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms



Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement Jedec test circuit