PN8024R

Chipown

Non-isolated PWM converters

General Description

The PN8024R consists of an integrated Pulse Width Modulator (PWM) controller and power MOSFET，specifically designed for small power non-isolated switching power supply. PN8024R offers fully intelligentized protection including Cycle-by-Cycle current limiting (OCP); Over Voltage Protection (OVP), Under Voltage Lockout and Over Temperature Protection (OTP). Excellent EMI performance is achieved with Pulse Frequency Modulation. PN8024R also consists of the high voltage start-up circuit to ensure that start quickly. The application need less component device.

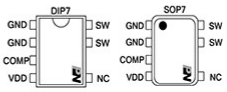
Features

- Be optimized with 12V output non-isolated application
- 85~265V_{AC} wide input voltage scope
- Frequency modulation for low EMI
- Internal HV Start-up Circuit
- Semi enclosed steady output power >3.6W @230VAC, DIP-7
- Semi enclosed steady output power >3.0W @230VAC, SOP-7
- Excellent constant voltage regulation and High efficiency
- Excellent Protection Coverage:
  - Adjustable Over Current Protection（OCP）
  - Over Temperature Protection（OTP）
  - over voltage protection (OVP)

Applications

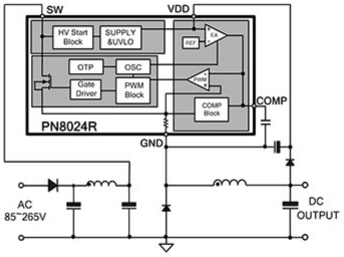
- non-isolated assistant power supply

Package/Order Information



Order Code	Package
PN8024RSSC-R1	SOP-7
PN8024RNSC-T1B	DIP-7

Typical Circuit



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Pin Definitions

Table 1. Pin Definitions

Pin Number	Pin Name	Pin Function Description
1、2	GND	Ground
3	COMP	Voltage feedback.
4	VDD	Positive Supply voltage Input.
5	NC	No connection
6、7	SW	HV MOSFET Drain pin.

Typical Power

Table 2. Typical power

Part number	Input Voltage	Steady output power (1)	Peak Power(2)
PN8024R SOP-7	150-265 V_{AC}	3W(12V250mA)	4.2W(12V350mA)
	85-265 V_{AC}	2.4W(12V200mA)	3.6W(12V300mA)
PN8024R DIP-7	150-265 V_{AC}	3.6W(12V300mA)	4.8W(12V400mA)
	85-265 V_{AC}	3.0W(12V250mA)	4.2W(12V350mA)

Note:

1. Maximum output power in a semi enclosed design measured at 75°C ambient temperature, Duration:2 hours
2. Peak power in a semi enclosed design measured at 75°C ambient temperature, Duration:1 min

Absolute Maximum Ratings

Supply voltage Pin V_{DD}..... -0.3~32V

High-Voltage Pin, SW.....-0.3~650V

COMP Supply Voltage.....-0.3~5.5V

Junction Operating Temperature..... -40~150℃

Storage Temperature Range.....-55~150℃

Lead Temperature (Soldering, 10secs).....260℃

Package Thermal Resistance (SOP-7).....80℃/W

Package Thermal Resistance (DIP-7).....40℃/W

ESD voltage Protection (HBM, ESDA/JEDEC JDS-001-2012)..... ±4kV

ESD voltage Protection (1) (Air discharge to pins of PN8024R with ESD Generator).....8kV

The biggest drain pulse current (T_{pulse}=100us).....3A

Note: 1. Enterprise internal standards, for reference only.

Electrical Characteristics(T_A =25°C, V_{DD} = 15V; unless otherwise specified)

Table 3. Power Supply Section

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
B_{VDSS}	Break-down voltage	I_{SW} =1mA, V_{COMP} = GND	650	690		V
I_{OFF}	Off-state drain current	V_{SW} =600 V, V_{COMP} = GND			100	uA
$R_{DS(on)}$ DIP-7	Drain-source on state resistance	I_{SW} = 0.5A, VCOMP = 3V		13.5		Ω
$R_{DS(on)}$ SOP-7	Drain-source on state resistance	I_{SW} = 0.5A, VCOMP = 3V		8.0		Ω

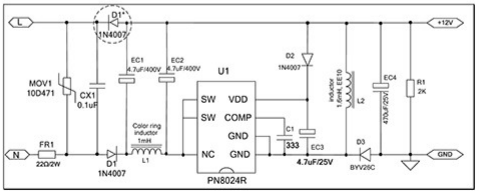
Table 4. Supply Section

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE PARAMETER						
V_{SW_START}	Drain-source start voltage				105	V
I_{DD_CH}	Start up charging current	V_{SW} = 105 V, V_{COMP}= GND, V_{DD} = 11.8V		-1.2		mA
V_{DD}	Operating voltage range	After turn-on	9		24	V
$V_{DDclamp}$	VDD clamp voltage		28	30	32	V
V_{DDovp}	VDD ovp Voltage		24		29	V
V_{DDon}	VDD start up threshold		11.5	12.5	13.5	V
V_{DDoff}	VDD under voltage shutdown threshold		7.5	8	8.5	V
$V_{DDrestart}$	VDD restart threshold		5		6.5	V
$V_{DD\text{-}REF}$	VDD feedback reference			12.3		V
CURRENT PARAMETER						
I_{DD}	Operating supply current, switching				2	mA
I_{DD_FAULT}	Operating supply current, with protection tripping		100		550	uA
I_{DD_OFF}	Operating supply current with VDD < VDD_OFF	V_{DD} = 6 V	100		450	uA

Table 5. Control Section (T_A=25°C, V_{DD} = 15V; unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE PARAMETER						
I_{dlimit}	Max drain current limitation DIP-7		0.48	0.57	0.66	A
	Max drain current limitation SOP-7		0.39	0.49	0.59	A
T_{ON_MIN}	Minimum turn ON time			500		ns
t_d	Propagation delay			100		ns
t_{LEB}	Leading edge blanking			400		ns
OSCILLATOR PARAMETER						
F_{OSC_MAX}	Maximum Switching Frequency	V_{COMP} = 3V		60		kHz
FD	Frequency Variation			±8		%
FM	Modulation frequency			250		Hz
D_{MAX}	Maximum duty cycle		55		74	%
ERROR AMPLIFIER PARAMETER						
Gain	DC Current Gain			65		dB
$I_{\_COMP1}$		V_{DD} =15V，V_{COMP} = 2.5V	10		20	uA
$I_{\_COMP2}$		V_{DD} =10V，V_{COMP} = 2.5V	-20		-10	uA
$I_{\_COMP3}$		V_{DD} =15V，V_{COMP} = 0.5V	5		20	uA
THERMAL PARAMETER						
T_{SD}	Thermal shutdown temperature		140	160		°C
T_{HYST}	Thermal shutdown hysteresis			30		°C

Typical Circuit



Operation Description

1. Start up

At start up, the internal high-voltage current source supplies the internal bias 1.2mA and charges the external V_{DD} capacitor. When V_{DD} reaches 12.5V, the device starts switching and the internal high-voltage current source stops charging the capacitor. The device is in normal operation provided V_{DD} does not drop below 8V. After start up, the bias is supplied from the auxiliary transformer winding.

2. Gate driver

The internal power MOSFET in PN8024R is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate drive results in worse EMI.

A good tradeoff is achieved through the built-in totem pole gate design with proper output strength and dead time. The good EMI system design and low idle loss is easier to achieve with this dedicated control scheme.

3. Oscillator

The switching frequency of PN8024R is internally fixed at 60 kHz. No external frequency setting components are required for PCB design.

The frequency modulation is implemented in PN8024R, So that, it minimizes the conduction band EMI and therefore eases the system design because the tone energy could be spread out.

4. Internal error amplifier

The output voltage modulation could be realized by the error amplifier built –in PN8024R. Through the internal resistor voltage divider, output voltage could be modulated via using the error amplifier detection VDD potential.

5. PFM -mode operation

PN8024R work in PFM-mode to decrease light load power consumption. When load mitigated，and frequency reduced. Lower switching frequency is helpful to reduce the switching loss.

6. Output constant voltage modulation

PN8024R provide the load compensation function，that can make good load modulation。

7. Over temperature protection (OTP)

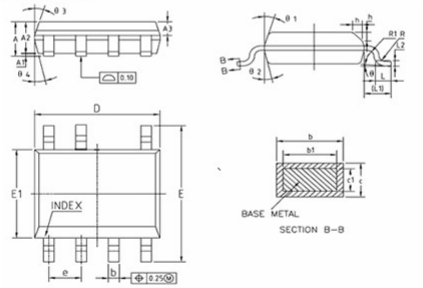
The power MOSFET and control chip are integrated, making it easier for control chip to detect the temperature of MOSFET. If the temperature exceeds about 160℃，OTP fault is activated.

Package Dimensions

Table 6. SOP-7 mechanical data

Size / symbol	Min.(mm)	Nom.(mm)	Max.(mm)	Size / symbol	Min.(mm)	Nom.(mm)	Max.(mm)
A	1.35	1.55	1.75	L	0.45	0.60	0.80
A1	0.10	0.15	0.25	L1	1.04REF		
A2	1.25	1.40	1.65	L2	0.25BSC		
A3	0.50	0.60	0.70	R	0.07	—	—
b	0.38	—	0.51	R1	0.07	—	—
b1	0.37	0.42	0.47	h	0.30	0.40	0.50
c	0.17	—	0.25	θ	0°	—	8°
c1	0.17	0.20	0.23	θ1	15°	17°	19°
D	4.80	4.90	5.00	θ2	11°	13°	15°
E	5.80	6.00	6.20	θ3	15°	17°	19°
E1	3.80	3.90	4.00	θ4	11°	13°	15°
e	1.270 (BSC)						

Figure 1. Package dimensions



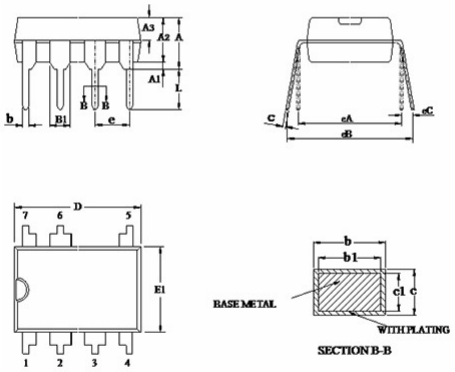
TOP MARK	Package
PN8024R YWWXXXXX	SOP-7

Note: Y: Year Code; W: Week Code; XXXXX: Internal Code

Table 7. DIP-7 mechanical data

Size / symbol	Min.(mm)	Nom.(mm)	Max.(mm)	Size / symbol	Min.(mm)	Nom.(mm)	Max.(mm)
A	3.60	3.80	4.00	c1	0.24	0.25	0.26
A1	0.51	-	-	D	9.05	9.25	9.45
A2	3.00	3.30	3.40	E1	6.15	6.35	6.55
A3	1.55	1.60	1.65	e	2.54BSC		
b	0.44	-	0.53	eA	7.62BSC		
b1	0.43	0.46	0.48	eB	7.62	-	9.30
B1	1.52BSC			eC	0	-	0.84
c	0.25	-	0.31	L	3.00	-	-

Figure 2. Package dimensions



TOP MARK	Package
PN8024R YWWXXXXX	DIP-7

Note: Y: Year Code; W: Week Code; XXXXX: Internal Code

Note: If you need product datasheet or design reference report,please click here.>>

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